Modeling Techniques of Submicron GaAs MESFETs and HEMTs

by

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Dedication

This work is dedicated to my loved Father (*late*),
Praiseworthy Mother and
Dr Muhammad Mansoor Ahmed for guiding me with love and patience.

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I humbly praise and grateful to ALMIGHTY ALLAH, Who permits me to live and accomplish tasks including the research work being presented in this thesis.

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May ALLAH bless all these wonderful people.

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Abstract

This thesis discusses the electrical response of submicron GaAs MESFETs and HEMTs to develop a physical model. Nine different FET models have been presented and their ability to simulate submicron GaAs MESFET characteristics are checked. To demonstrate the validity of a model, I-V characteristics of short channel MESFETs are simulated and compared with experimental data. The accuracy of a model is reported by evaluating its RMS error values.

A comprehensive new model is developed to simulate I-V characteristics of short channel GaAa FETs. It has been demonstrated that the proposed model is a comprehensive one, capable of simulating DC characteristics of GaAs MESFETs including those having significant non-ideal Schottky barrier response. The model has also been applied successfully to I-V characteristics of GaAs HEMTs.

The Schottky barrier interfacial layer dependent performance of submicron GaAs MESFETs has been discussed by using their output and transfer characteristics. The mobility of carriers, scattering from the channel into the Schottky barrier gate, increases significantly for the devices which have a relatively thicker interfacial layer. The negative effects of increased carriers' mobility from MESFET Schottky barrier gate are discussed and a plausible explanation is given for reduced barrier lowering in the presence of interfacial layer. Based on the proposed explanation the definition of threshold voltage has been redefined involving the concept of interfacial layer thickness.

A technique is developed to estimate intrinsic small signal parameters of GaAs MESFETs and HEMTs. In the proposed technique DC characteristics are first evaluated. Once a good DC match is attained then small signal parameters are evaluated. To check the validity of the proposed technique submicron GaAs MESFETs and HEMTs of varying gate length have been simulated. It has been shown that the proposed method is accurate as well as efficient in estimating AC parameters of GaAs FETs by using their DC characteristics, and could be employed as a useful tool in device simulation software.

List of Publications

1. **N. M. Memon**, M. M. Ahmed and F. Rehman "Comparison of Nonlinear *I-V* Models for Submicron GaAs MESFET's Characteristics," IEEE-ICSICT-2006, Shanghai China, Oct 2006.

2. **N. M. Memon**, M. M. Ahmed and F. Rehman "A Comprehensive Four Parameters *I-V* Model for GaAs MESFET Output Characteristics," Journal of Solid State Electronics, Vol. 51, pp 511-516 (2007).

3. U. Iqbal, M. M. Ahmed and **N. M. Memon** "An Efficient Small Signal Parameters Estimation Techniques for Submicron GaAs MESFET's," IEEE-ICET- 2005, Islamabad, September 2005.

4. **N. M. Memon**, M. M. Ahmed and S. A. Moiz "Extraction of AC Parameters of *mm* Wavelength GaAs MESFETs and HEMTs from measured DC Characteristics," Submitted in Journal of Microelectronics.

5. M. M. Ahmed, **N. M. Memon** and S. A. Moiz "Effects of Schottky Barrier Interfacial Layer on Submicron GaAs MESFET's Characteristics," Submitted in IEEE Transactions on Electron Devices.

Contents

List of Figures

List of Tables

Abbreviations

a	Epi-layer thickness
AC	Alternating Current
$A(x)$	Available channel height
C_{gs}	Gate-source capacitance
C_{gd}	Gate-drain capacitance
C_{ds}	Drain-source capacitance
C_p	Pad capacitance
C_{pg}	Gate pad capacitance
C_{pd}	Drain pad capacitance
DC	Direct Current
d	Interfacial layer thickness
E_x	Electric field in x-direction
E_y	Electric field in y-direction
E_s	Electric field at saturation velocity
E_{max}	Maximum electric field
E_c	Energy of conduction band
E_v	Energy of valance band
E_g	Band gap
E_F	Fermi level
E_{Fn}	Fermi level in n-type semiconductor
E_{Fm}	Fermi level in metal
FET	Field Effect Transistor

f_T	Unity gain frequency
GaAs	Gallium Arsenide
g_d	Output conductance
g_m	Transconductance
$g_{m(ac)}$	AC Transconductance
h	Depletion width
HEMT	High Electron Mobility Transistor
I-V	Current-Voltage
I_{ch}	Channel current
I_{ds}	Drain-to-Source current
I_{gs}	Gate-to-Source current
I_p	Pinch-off current
$I_{ds(sat)}$	Drain saturation current
I_{dss}	Saturation current at $V_{gs} = 0$
J	Current density
JFET	Junction Field Effect Transistor
L_G	Gate length
L_g	Gate inductance
L_s	Source inductance
L_d	Drain inductance
L_{sg}	Source-gate distance
L_{gd}	Gate-drain distance
m	Number of parallel strips
MESFET	Metal Semiconductor Field Effect Transistor
n	Integer

N_d	Doping density of the channel
q	Electronic charge
Q_m	Negative charges in semiconductor
Q_d	Positive charges in semiconductor
Q_{ss}	Charges in the interface states
R_s	Source resistance
R_g	Gate resistance
R_d	Drain resistance
R_{dc}	DC resistance
R_c	Contact resistance
R_i	Channel resistance
R_{ox}	Resistance of the oxide layer
SCLC	Space charge limited current
Si	Silicon
v_s	Saturation velocity
V_{gs}	Gate-to-source voltage
V_{gd}	Gate-to-drain voltage
V_{eff}	Effective gate-to-source voltage
V_{ds}	Drain-to-source voltage
V_{bi}	Barrier height
V_i	Potential drop across interfacial layer
V_T	Threshold voltage
$V_{Breakdown}$	Breakdown voltage
ΔV_T	Shift in threshold voltage
ΔV_{Td}	Shift in threshold voltage due to oxide layer

W_d	Width of the depletion at drain
W_s	Width of the depletion at Source
x_d	Depletion layer thickness
Z	Gate Width
α	Simulates the dependence of linear region on V_{ds}
β	Transconductance parameter
γ	Simulates the dependence of threshold voltage on V_{ds}
λ	Simulates the dependence of I_{ds} on V_{ds}
δ	Voltage range transition
η	Simulates Schottky barrier interface
ε_{ox}	Permittivity of oxide layer
ε_s	Permittivity of Semiconductor (GaAs)
ε_o	Permittivity of free space
μ_{ox}	Mobility of oxide layer
μ_e	Mobility
μ_o	Permeability of free space
τ	Transit time delay
ω	Angular velocity
Φ_b	Schottky barrier height
Φ_m	Metal work function
Φ_0	Continuous distribution of surface states at interface

Chapter 1

Introduction

1.1. MESFET's Overview

In the innovative years of electronics i.e., before the 1940s, electron tubes were commonly used in the electronic systems, such as radio and television, but they had some serious limitations pertaining to their performance. Then a better discovery was made in 1947, when Bardeen and Brattain invented the transistor by using a slice of germanium with a few carefully placed wires [Brattain-1947]. Since its inception, the transistor brought a revolution to the industry and in day to day life through its use in automation, control and communication equipment. The diverse industrial demand eventually led to different types of transistors currently available in the market.

The concept of Schottky barrier FET was introduced by Schottky [Schottky-1938]. He gave the idea of formation of a potential barrier due to the difference of work function between the metal and the semiconductor contacts. Afterwards, a

researcher from Bell Laboratories William Shockley [Schockley-1948] invented the junction transistor and Bell Laboratories announced this invention in 1951.

Schottky's idea was utilized by Mead in 1966 for the fabrication of Metal Semiconductor Field Effect Transistor (MESFET) [Mead-1966] and subsequently it was fabricated by Hooper in 1967 using a Gallium Arsenide (GaAs) epitaxial layer on semi-insulating GaAs substrate [Hooper-1967].

A MESFET is a three-terminal device like any other transistor [Sze-1985, Soares-1988]. These terminals are named as Source, Drain and Gate as shown in Figure (1.1) Charge carriers (electrons) flow from the source to the drain via a channel. The channel is defined by doping the epitaxial layer grown on semiconductor and offers good conduction. The flow of charge carriers in the channel is controlled by a Schottky barrier gate. The main advantages of a MESFET compared to its counter parts are:

(a) high electron velocity inside the channel;
(b) smaller transit time leading to faster response and
(c) fabrication of active layer on semi-insulating GaAs substrates to decrease the parasitic capacitances.

In 1970, for microwave applications, Middlehoek realizes that Silicon based MESFETs with 1 μm gate length had maximum oscillation frequency up to 12 GHz [Middlehoek-1970]. In 1971, Turner took a step, when 1 μm gate length FETs were made on GaAs with maximum frequency upto 50 GHz [Turner-1971]. Such a high performance is attributed to GaAs which offers superior electrical properties compared to the Silicon. Beside high frequency of oscillation GaAs MESFETs also provide high output power with low noise figure. Owing to these attributes GaAs

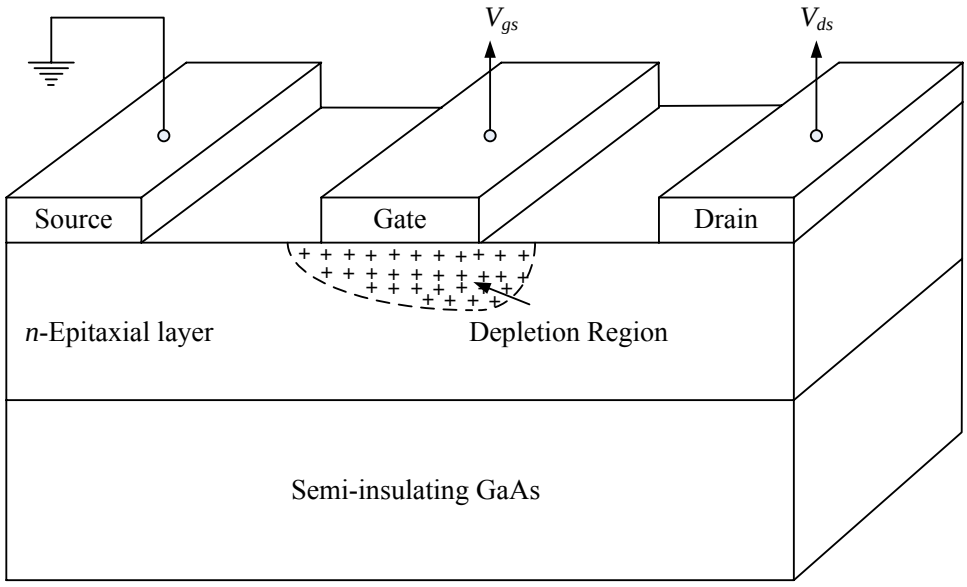


Figure (1.1): A cross-sectional view of a GaAs MESFET fabricated on a semi-insulating GaAs substrate.

MESFETs are overwhelmingly used in microwave integrated circuits [Ladbrooke-1991, Golio-1991, Bose-2001 and Khalaf-2000].

GaAs MESFETs have demonstrated excellent noise and gain performance at microwave frequency and they are used quite often in pre-amplifiers of communication devices. In today's world, high frequency communication is possible because of the superior electrical properties offered by GaAs MESFETs both in analog as well as in digital applications. A properly designed GaAs MESFET can operate comfortably at a frequency higher than 100 GHz [Ahmed-2003]. Whereas, a High Electron Mobility Transistor (HEMT) of submicron gate length can operate higher than 900 GHz [Das-1987 and Cidronali-2003]. An excellent microwave performance of a GaAs MESFET is certainly related to its channel properties [Golio-1991]. For low noise applications, there are special constraints on the design of a MESFET to achieve target performance [Fukui-1979, Feng-1992 and Hung-1988].

1.2. GaAs MESFET Construction

A microwave GaAs MESFET device is fabricated using semi-insulating GaAs substrate. GaAs has attractive features at high frequencies compared to Silicon. The substantial improvement in FET performance by using GaAs substrate over the Silicon is mainly attributed to the fact that:

(i) The conduction band electrons in GaAs have approximately six times higher mobility and twice the peak drift velocity as that of Silicon. This leads to low parasitic resistances, large transconductance and shorter transit time.

(ii) The larger band gap in GaAs devices allows higher working temperature. This is particularly important in the small geometry of power devices which are used at microwave frequencies and dissipates a lot of heat. Furthermore, due to the relatively large band gap, GaAs devices operating at room temperature offer low thermal leakage current and thus provide a low noise figure.

In MESFET fabrication, a thin epitaxial layer of *n*-type GaAs is deposited on a semi-insulating GaAs substrate. The optimum value of doping concentration in the epi-layer depends on the maximum allowed gate leakage current. For a given doping concentration optimum value of active channel thickness, a is a function of gate length, L_G. It has been shown that optimum doping level for low noise *mm*-wave length device is ~ 5 x 10^{17} cm^{-3} [Ohata-1980]. Ladbrooke has reported that for a good L_G / a ratio which is commonly known as the aspect ratio, should be in the range of 3-5 [Ladbrooke-1991]. Dambkes have reported the smallest acceptable value of L_G / a for a low-noise MESFET is 3 [Dambkes-1983]. According to a review by Golio, most reported devices have been fabricated with L_G / a ratio that lies between 2-10 [Golio-1988].

In *mm*-wave GaAs MESFETs where transconductance is of prime importance and the devices are operated at comparatively low current and biasing voltage, gate recesses are usual as shown in Figure (1.2). For good high frequency and noise performance, depth and shape of recess are both important. Increasing the value of gate recess-depth reduces the residual channel thickness which leads to increased output conductance [Mishra-1986].

A *mm*-wave length low noise GaAs MESFET has drain-source separation $\leq$ 1μm, with $L_G \leq 0.5$ μm. Drain and Source ohmic contacts are fabricated by using

AuGeNi alloy which is annealed to reduce ohmic resistance. After the gate lithography, Schottky barrier gate is usually fabricated by employing Ti/Au metals,

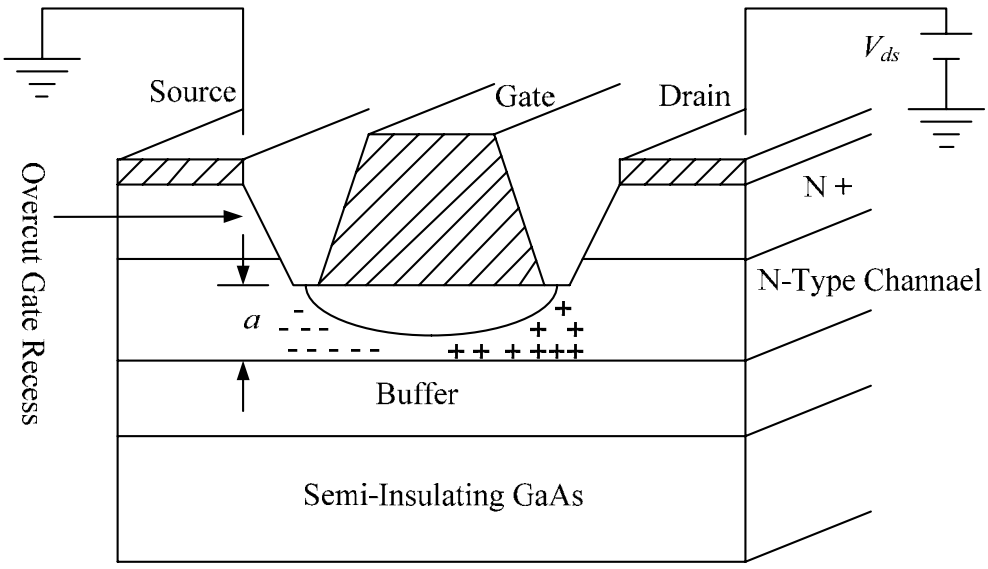


Figure (1.2): A cross-sectional view of a GaAs MESFET illustrating the recess gate technology.

where Ti is used to provide adhesiveness to Au.

Since the noise figure, N_f of a GaAs MESFET is given by [Fuki 1979]

$$N_f = 1 + k_f C_{gs} \sqrt{\frac{R_g + R_s}{g_m}} \qquad (1.2.1)$$

where k_f is constant, R_g is gate resistance, R_s is source resistance, g_m is transconductance and C_{gs} is gate-to-source capacitance. As per Equation (1.2.1), in order to reduce noise figure R_g is reduced by adopting interdigitated technology, which leads to different types of MESFET topologies as shown in Figure (1.3). Furthermore, R_g is reduced by increasing the metal cross-section of a Schottky barrier gate, while maintaining L_G small. This leads to T-gate GaAs MESFET technology as shown in Figure (1.4).

A further reduction in N_f is made by decreasing R_s through recess gate technology in MESFET fabrication in which gate metal is placed after etching the epilayer to a pre-determined value.

1.3. Types of MESFETs

The type of a MESFET device depends upon the thickness of an epitaxial layer. It can be designed to operate either as a depletion type (normally ON) or an enhancement type (normally OFF) [Grebene-1969]. In a depletion type device the thickness of the epitaxial layer is more than the zero-bias depletion region width of the Schottky barrier gate, and the transistor has a conducting channel at V_{gs} = 0 V. Thus, the gate is biased in the negative to deplete the channel, as shown in Figure (1.5-a).

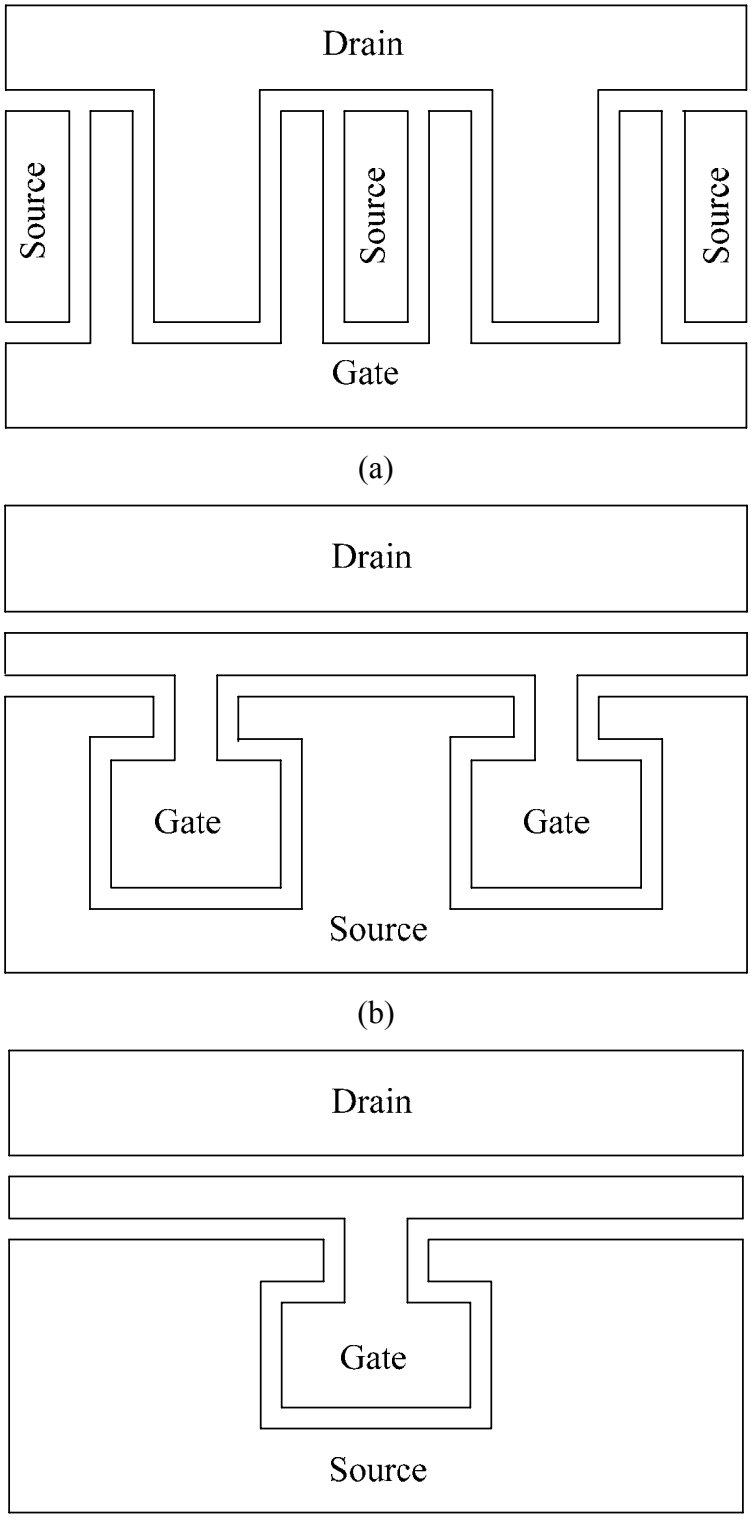


Figure (1.3): Different layouts of a GaAs MESFET.

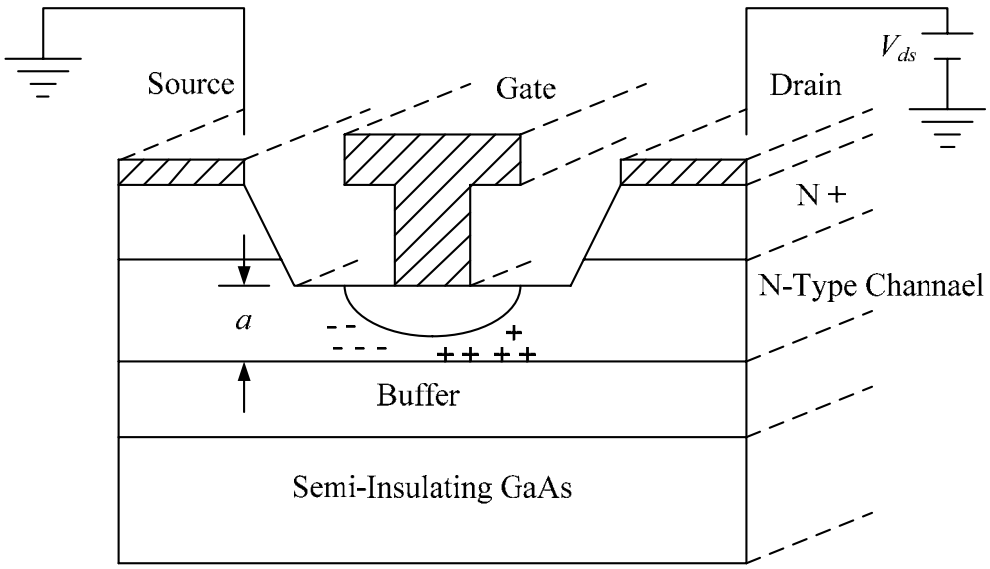


Figure (1.4): A cross-sectional view of a T-gate GaAs MESFET.

In an enhancement-type device, as shown in Figure (1.5-b), the epitaxial layer is kept thin, and the built-in voltage of the metal gate Schottky barrier junction is sufficient to deplete the channel completely at V_{gs} = 0 V [Sze-1985]. Conduction in the channel occurs only for small positive values of V_{gs}. Enhancement type devices are useful for high-speed and low power applications, but majority of the MESFET's are the depletion type devices.

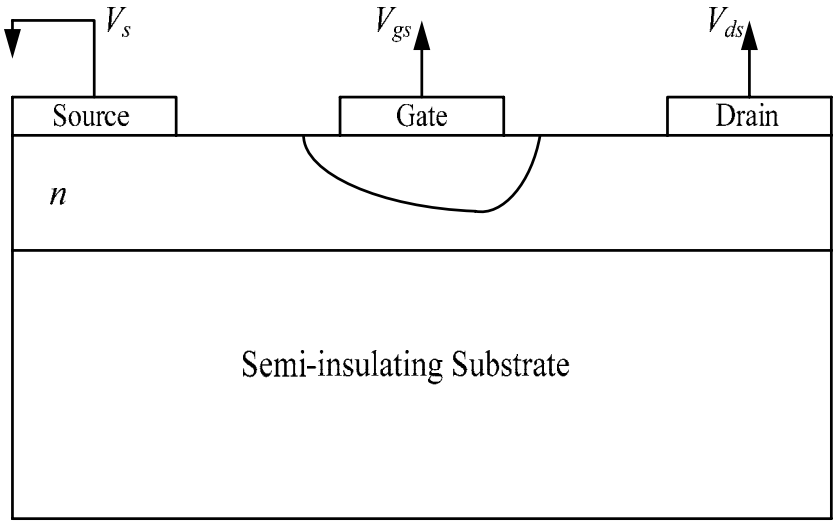
1.4. MESFET Characteristics

A MESFET offers two types of characteristics: (a) output and (b) transfer characteristics. Output characteristics are defined by drain to source current, I_{ds} as function of drain to source, V_{ds} and gate to source voltage, V_{gs} i.e., I_{ds} (V_{ds}, V_{gs}).

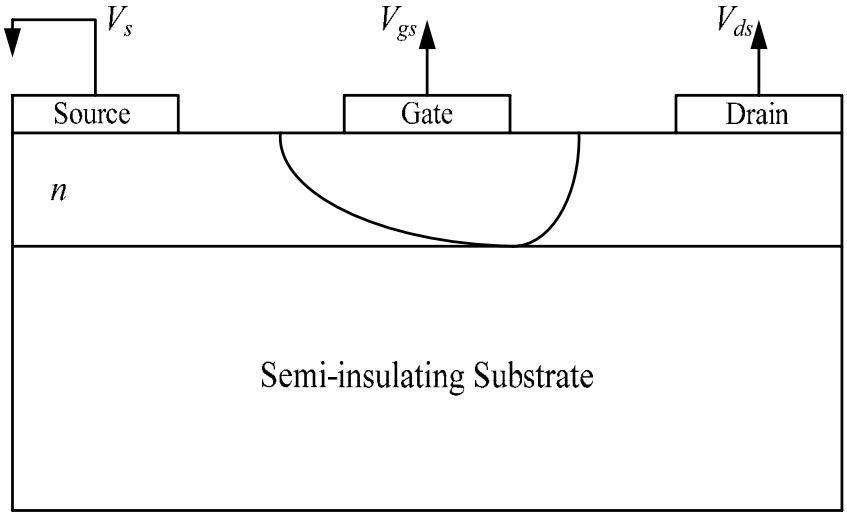
In short channel MESFET, increasing V_{ds} beyond a certain value, a condition called velocity saturation conditions, reaches in the channel, where I_{ds} becomes independent of V_{ds} and stay at a constant level. At this condition $I_{ds} = I_{ds(sat)}$ and $V_{ds} = V_{ds(sat)}$ and the device under this condition essentially behaves as a current source.

For an *n*–channel device if applied V_{gs} is positive, this enhances the channel cross-section by reducing the gate depletion and the operation of the device is known as enhancement mode operation. The same operation may be reciprocated by reversing the sign of the applied V_{gs} which is called depletion mode operation. The depletion mode operation is possible only in those devices which have $V_{gs} = 0$, $I_{ds} \neq 0$, i.e., normally ON devices.

The transfer characteristics of a GaAs MESFET are observed as:



(a)



(b)

Figure (1.5): GaAs MESFET types (a) depletion type device
(b) enhancement type device.

$$I_{ds}(V_{gs}) \quad \text{for} \quad V_{ds} = V_{ds(sat)} \tag{1.4.1}$$

For a depletion type device, the transfer characteristics comply with the conditions:

$$\begin{aligned} I_{ds}(V_{gs}) &= I_{dss} \quad \text{when} \quad V_{gs} = 0\,V \\ I_{ds}(V_{gs}) &= 0 \qquad \text{when} \quad V_{gs} = V_T \end{aligned} \tag{1.4.2}$$

Flow of current through Schottky barrier gate is called leakage current (I_{gs}) and for a good device its value is less than 1 μm. It is dependent on biasing voltage V_{gs} and V_{ds}. The characteristics, $I_{gs}(V_{gs}, V_{ds})$ are also known as Schottky characteristics. For a good quality MESFET Schottky characteristics should have an ideality factor equal to unity [Ahmed-1995].

The AC capability of a MESFET is evaluated by using standard AC probers, which involves the measurements of scattering parameters as a function of frequency. The measured scattering parameters are then used to evaluate MESFET AC equivalent circuit. The developed AC circuit is employed to determine unity gain frequency, maximum frequency of oscillation and other such parameters for a given MESFET.

1.5.MESFET Models

The trend of higher integration and higher transmission speed, challenges modeling engineers to develop accurate models for MESFETs DC and AC simulation (Ladbrooke-1991). An important relationship exists among device models, parameter extraction techniques, and device measurements (Neamen-1992). The accuracy of a model is determined not only by the form and features of the model, but also by the

validity of the parameters used within the model (Golio-1991). Reliable determination of these parameters is required for device characterization. There are two types of modeling techniques normally employed by the design engineers; (a) Numerical technique and (b) Physical technique [Ahmed-1996].

In the numerical modeling technique, the field distribution inside the channel is evaluated under changing conditions and the flow of caries as a function of applied biasing is evaluated. Since, the parameters which influence the field distribution are numerous, thus, it is very hard to predict the field efficiently. Furthermore, it involves rigorous mathematical treatment and quite often is difficult for a design engineer to handle.

On the other hand, a physical modeling technique requires information regarding device dimensions and material parameters. In these models mathematical expressions are simpler and involve fewer variables to handle with. Thus a design engineer prefers a physical model in which the changed device characteristics can be envisaged quickly by changing physical variables of the device.

1.6. Thesis Layout

This thesis comprises of seven chapters. Chapter # 2 deals with the fundamental concept of a GaAs MESFET. The basic equations which involve its operation have been described in this chapter. Chapter # 3 reviews nine different physical models presented from 1980-2004. The ability of these models to simulate DC response of submicron MESFETs and HEMTs is discussed. Chapter # 4 discusses the performance of GaAs MESFETs as a function of their Schottky barrier quality. The degradation caused by the native oxide layer, present on the surface of GaAs, is evaluated. Chapter # 5 presents a new model based on results obtained by comparing

nine different physical models presented in Chapter-3. The validity of the proposed model is checked by simulating *I-V* characteristics for a range of FET devices. Chapter # 6 predicts the small signal equivalent circuit of GaAs MESFETs and HEMTs by using their DC characteristics. The developed technique gives a straightforward mechanism for the estimation of device small signal parameters. A comprehensive summary of research work along with possible future extension is presented in Chapter # 7.

Chapter 2

MESFET's Operation

2.1. Introduction

The operation of a GaAs MESFET is similar to Si JFET, but the only difference is, in GaAs MESFET a metal semiconductor rectifying contact is used at the gate instead of a *pn* junction of a JFET [Sze-1981, Shur-1990]. A MESFET device is biased by applying two voltages, V_{gs} and V_{ds} [Mass-1988]. These voltages are used to control I_{ds}, which is present between the drain and the source of the device, by varying the electric field inside the channel. The field changes by changing the applied potential, giving rise to three distinct regions in the *I-V* characteristics of the device namely:

(a) Linear Region;

(b) Saturation Region and

(c) Pinch-off Region.

To simulate the dependence of I_{ds} on V_{gs} and V_{ds}, the field distribution inside the channel, which is dependent on device geometry, should be known [Rodriguez-1994, McCamant-1990 and Ahmed (a)-1997]. Microwave MESFETs are of submicron gate length; called short channel devices having $L_G < a$ and usually fabricated by employing the gate recess technology [Das-1987, Bernstein-1998, Golio-1991 and Ahmed-1995]. Whereas low frequency devices having $L_G > a$ are called long channel devices [Adams-1993, Jaeckel-1986, Watts-1989]. This chapter, primarily, deals with mathematical description of *I-V* characteristics of both long channel and short channel MESFETs. It also describes the origin of intrinsic and extrinsic device parameters, which influence the performance of the device and are also required for its accurate modeling.

2.2. Long Channel Model

MESFETs fabricated by employing the condition $L_G > a$ are called long channel devices and the model that describes the behavior of such devices is termed as long channel model. It was first presented by Shockley in 1951 [Shockley-1951]. To describe the basic mechanism involved in the Shockley model, consider a cross-sectional view of a GaAs MESFET shown in Figure (2.1). In this figure L_G is the channel length, h is the depletion width, $V(x)$ is the voltage drop underneath the gate, a is the epi-layer thickness, W_d and W_s represent width of the depletion at drain and source sides of the device respectively and $A(x)$ is the available channel height defined as

$$A(x) = a - h(x). \tag{2.2.1}$$

Here $A(x)$ is a function of x because the electrons are flowing from source to drain

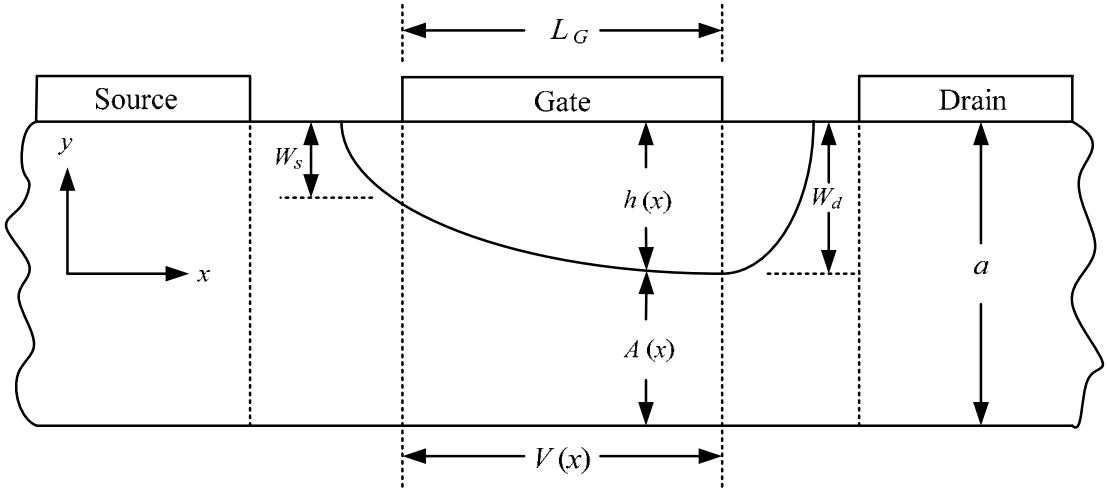


Figure (2.1): A cross-sectional view of a biased GaAs MESFET channel.

giving rise to a voltage drop $V(x)$ along the channel which varies from zero at the source end to V_{ds} at the drain side of the device. The potential difference between the gate and the channel at any point x is, therefore, given as

$$V_1 = \Phi_b - V_{gs} + V(x) \tag{2.2.2}$$

here Φ_b is the Schottky barrier height.

In order to calculate the width of the depletion layer formed by the Schottky barrier, it is assumed that the junction is abrupt and all the donor atoms (N_d) are ionized [Zeghbroeck-2004]. Under such conditions the two-dimensional Poisson's equation can be written as [Zeghbroeck-2004]

$$\frac{\partial^2 \Phi_b}{\partial x^2} + \frac{\partial^2 \Phi_b}{\partial y^2} = -\frac{q N_d}{\varepsilon_s} \tag{2.2.3}$$

If we also assume that the variation of the potential along the length of the channel is negligibly small compared to y-directed field then Equation (2.2.3) can be modified as

$$\frac{\partial^2 \Phi_b}{\partial y^2} = -\frac{dE_y}{dy} = -\frac{q N_d}{\varepsilon_s} \tag{2.2.4}$$

By solving Equation (2.2.4) one can evaluate the potential associated with the depletion region under the device boundary conditions as [Sze-1981]

$$\Phi_b = \frac{q N_d h^2(x)}{2 \varepsilon_s} \tag{2.2.5}$$

When V_{gs} and V_{ds} both are non zero then d is not uniform and it is function of x and can be written by using Equation (2.2.2) and (2.2.5)

$$h(x) = \sqrt{\frac{2\varepsilon_s}{q N_d}\left[\Phi_b - V_{gs} + V(x)\right]} \tag{2.2.6}$$

The depletion width W_d and W_s can be determined by letting $V(x) = V_{ds}$ at drain side and $V(x) = 0$ at source side of the device respectively. Thus,

$$W_d = \sqrt{\frac{2\varepsilon_s(\Phi_b - V_{gs} + V_{ds})}{q N_d}} \tag{2.2.7}$$

and

$$W_s = \sqrt{\frac{2\varepsilon_s(\Phi_b - V_{gs})}{q N_d}}\,. \tag{2.2.8}$$

By increasing the magnitude of the applied potential, the value of $A(x)$ decreases to an extent that it effectively goes to zero. The voltage at which $A(x) = 0$ is called pinch-off voltage or threshold voltage, V_T and represented as

$$V_T = \frac{q N_d a^2}{2\varepsilon_s} - \Phi_b \tag{2.2.9}$$

If x-directed mobility of the free carriers is given by μ and assuming the device width Z, then one can write the incremental channel current as

$$I_{ds}\, dx = q N_d \mu A(x) Z\, dV \tag{2.2.10}$$

After integrating Equation (2.2.10) over the channel length we get

$$I_{ds} = I_p \left[\frac{V_{ds}}{V_T} - \frac{2}{3}\left(\frac{\Phi_b - V_{gs} + V_{ds}}{V_T}\right)^{3/2} + \frac{2}{3}\left(\frac{\Phi_b - V_{gs}}{V_T}\right)^{3/2}\right] \tag{2.2.11}$$

where I_P is the saturation current given by

$$I_P = \frac{q^2 N_d^2 \mu Z h^3}{2 \varepsilon_s L_G} \quad . \tag{2.2.12}$$

When the current saturates $V_{ds} \geq V_{sat}$, and $V_{gs} \neq V_T$ its value is constant but non zero, whereas at $V_{ds} \geq V_{sat}$, and $V_{gs} = V_T$ its magnitude goes to zero.

Equation (2.2.11) represents the long channel model which is also known as the Shockley Model. The equation represents the linear *I-V* characteristics of a MESFET as shown in Figure (2.2). In this region $V_{ds} << V_{gs}$, therefore by applying the Binomial approximation, Equation (2.2.11) reduces to

$$I_{ds} = \frac{I_p}{V_T}\left[1 - \sqrt{\frac{\Phi_b - V_{gs}}{V_T}}\right] V_{ds} \tag{2.2.13}$$

The above expression demonstrates the linear variation of I_{ds} as a function of V_{ds}

In a long channel device, the saturation occurs when the channel pinches-off due to the applied V_{ds}, and at this point the current becomes independent of V_{ds} under ideal conditions [Ladbooke-1989 and Ahmed-1998]. Thus,

$$V_T = \Phi_b - V_{gs} + V_{ds} \tag{2.2.14}$$

Substituting this condition in Equation (2.2.11), the corresponding I_{ds} value is

$$I_{ds(sat)} = I_p \left[\frac{1}{3} - \left(\frac{\Phi_b - V_{gs}}{V_T}\right) + \frac{2}{3}\left(\frac{\Phi_b - V_{gs}}{V_T}\right)^{3/2}\right] \tag{2.2.15}$$

This represents long channel characteristics of a MESFET in the saturation

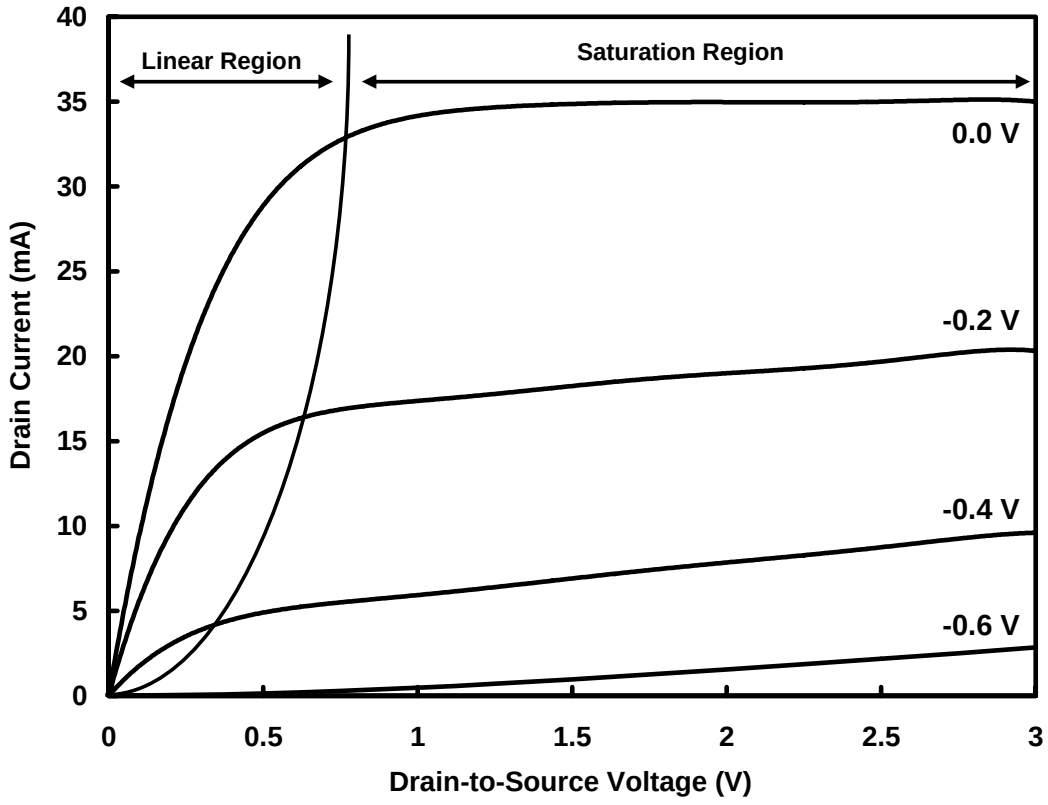


Figure (2.2): Typical *I-V* characteristics of a GaAs MESFET showing linear and saturation regions.

Region of operation. The combination of Equation (2.2.11) and (2.2.15) under the respective condition generates a family of characteristics both in the linear as well as saturation region of operation as shown in Figure (2.2). This model is collectively known as long channel model.

Shockley also proposed an approximate form of Equation (2.2.15), which is called MESFET square law for the drain current as [Yang-1978]

$$I_{ds} = I_{dss}\left(1 - \frac{V_{gs}}{V_T}\right)^2 \tag{2.2.16}$$

where $I_{dss} = I_{ds}$ at $V_{gs} = 0$.

Transconductance, g_m of a device after the onset of saturation is given by

$$g_m = \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{V_{ds}=Const} = \frac{I_p}{V_T}\left[\sqrt{\frac{\Phi_b - V_{gs}}{V_T}} - 1\right]. \tag{2.2.17}$$

Output conductance, g_d, also in the saturation region is defined as

$$g_d = \left.\frac{\partial I_{ds}}{\partial V_{ds}}\right|_{V_{gs}=Const} = \frac{I_p}{V_T} \tag{2.2.18}$$

This shows that the magnitude of g_d is higher when the channel current is higher. Since a high value of g_d is an undesirable feature, the expression represents that its value could be controlled by controlling V_T of a device.

Figure (2.2) illustrates linear and saturation regions of *I-V* characteristics of a MESFET. After the onset of saturation, the drain current remains constant until a phenomenon occurs, called avalanche breakdown [Shur-1978 and Bose-2001]. Due to

the increase in drain voltage the energy of the electrons increases. These energetic electrons collide with semiconductor atoms and create electron-hole pairs in the device. As a result, the drain current increases very rapidly with the drain voltage and the device's characteristics are no more controlled characteristics [Ladbrooke-1991].

2.3. Short Channel Model

Devices having length $L_G < a$ are called short channel devices and the model describing the *I-V* characteristics of such devices is called short channel model [Liechti-1976 and Ladbrooke-1991]. According to the Shockley model, the current saturation in long channel FETs occurs when the channel is pinched-off at the drain-side of the gate, whereas in microwave MESFETs it is due to the velocity saturation [Shur-1987]. The importance of the field dependence of electron mobility for understanding the current saturation in FETs was first mentioned by Das and Ross [Das-1955]. This concept was developed for many theoretical models which are used to describe FET's characteristics and to interpret experimental results [Wada-1979, Bonjour-1980, Shur-1982, and Ladbrooke-1989].

As shown in Figure (2.1), the width of the active channel available for the flow of current is given by

$$A(x) = a\left[1 - \sqrt{\frac{\Phi_b - V_{gs} + V(x)}{V_T}}\right] \qquad (2.3.1)$$

Assuming that the *x*-directed electric field, E_x is uniform along the channel and as V_{ds} increases from zero the value of E_x also increases until the saturation velocity electric field, E_s is obtained prior to the pinch-off. After this, the carriers will drift

with saturation velocity, v_s, and as a result I_{ds} will saturate. Thus, the saturation current for GaAs MESFETs is given by

$$I_{ds(sat)} = q\,N_d\,v_s\,(a-d)\,Z = q\,N_d\,v_s\,A(x)\,Z \qquad (2.3.2)$$

By combining Equations (2.3.1) and (2.3.2), we get

$$I_{ds(sat)} = q\,N_d\,v_s\,Z\,a\left[1-\sqrt{\frac{\Phi_b - V_{gs} + V(x)}{V_T}}\right] \qquad (2.3.3)$$

where

$$V(x) \approx E_s\,L_G \qquad (2.3.4)$$

A typical value of $V(x)$ where the saturation will occur is about 0.4 V [Ladbrooke-1989]. Thus, indicating current saturation due to the velocity saturation mechanism in microwave FETs.

In the saturation region g_m of short channel device is, therefore, given by

$$g_m = \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{V_{ds}=Const} = \frac{\varepsilon_s\,v_s\,Z}{h} \qquad (2.3.5)$$

and in saturation region g_d is also defined as

$$g_d = \left.\frac{\partial I_{ds}}{\partial V_{ds}}\right|_{V_{gs}=Const} = -\frac{\varepsilon_s\,v_s\,Z}{h} \qquad (2.3.6)$$

Plotting the $I_{ds(sat)}$ against V_{ds} with V_{gs} as a parameter, one gets a set of straight lines parallel to x-axis. Extending the lines to the origin, keeping in view the smooth transition, generates characteristics as shown in Figure (2.2).

It is an experimental fact that the magnitudes of I_{ds} after the onset of current saturation does not remain constant but it grows slowly with V_{ds}. According to Eastman [Eastman-1979] the channel electrons are heated by the intense electric field and have adequate energy to scatter into the substrate or into the buffer layers as shown in Figure (2.3). Therefore, the channel of the current carrying electrons tends to widen into the substrate, gives rise to a component of current I_{sub} in the substrate. Thus, I_{ds} will be divided into two currents I_{ch} and I_{sub}, i.e., $I_{ds} = I_{ch} + I_{sub}$. There is a sharp rise in the electric field in Region II and the peak field is observed near the drain end as shown in Figure (2.3). Because of this, the output characteristics of a MESFET will have a slight positive slope indicating a positive output conductance.

According to Ahmed [Ahmed-1998], the uncompensated charge accumulation towards the drain side of the depletion causes a transverse electric field which opposes gate biasing, as shown in Figure (2.4), thus widening the channel and generating positive slope of I_{ds} after onset of saturation. In this figure, the solid curve shows the depletion layer in the absence of transverse electric fields, whereas the broken curve shows the modification in the depletion layer due to the transverse electric fields.

2.4.Microwave MESFET's Equivalent Circuit

The equivalent circuit of a submicron GaAs MESFET is dependent upon the physical construction of the device [Sze-1985 and Ladbrooke-1989]. The origin of the device equivalent circuit elements is shown in Figure (2.5). In this figure the circuit elements are: source resistance, R_s; gate resistance, R_g; drain resistance, R_d; channel resistance, Ri; contact resistance, Rc; source inductance, Ls; gate inductance, Lg; drain inductance, L_d; gate-source capacitance, C_{gs}; gate-drain capacitance, C_{gd}; drain-

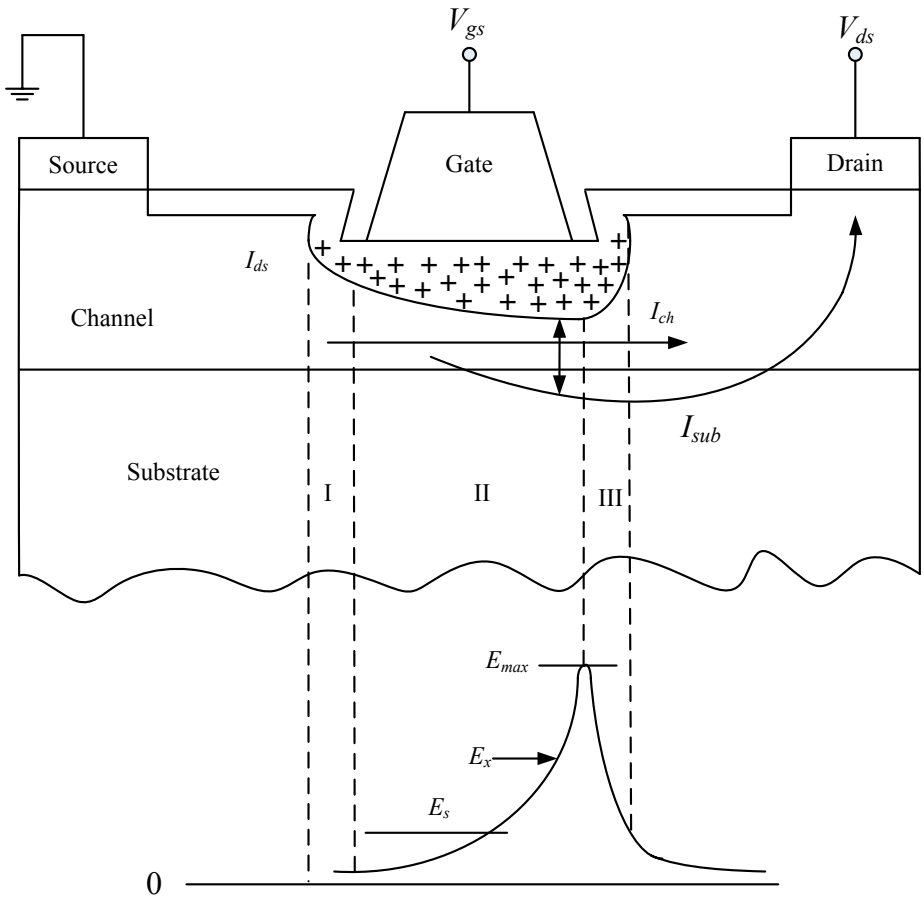


Figure (2.3): A Cross-sectional view of an operating MESFET showing the scattering of carriers under intense electric field into the substrate and subsequently collected by the drain electrode.

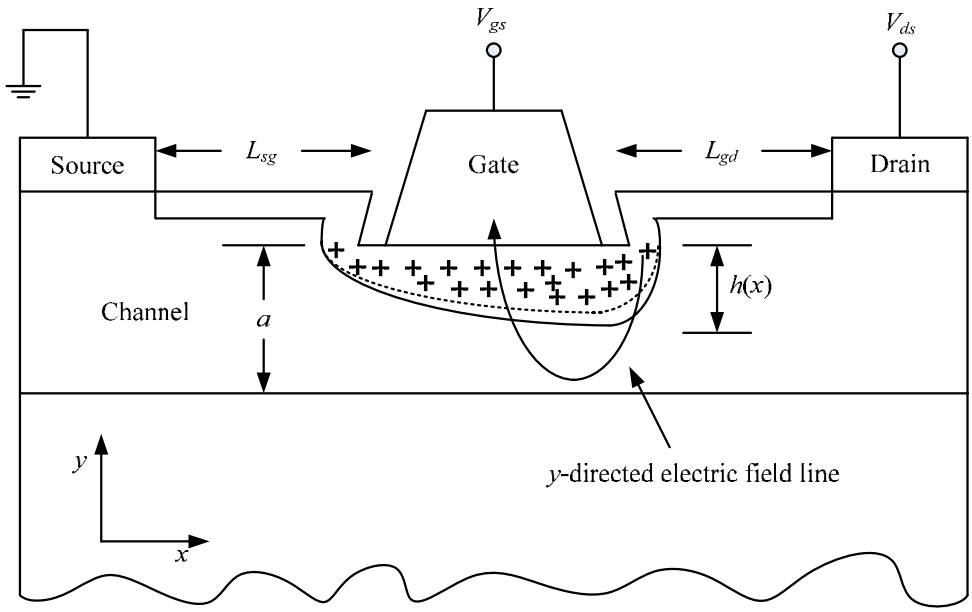


Figure (2.4): A Cross-sectional view of an operating GaAs MESFET indicating the depletion modification due to transverse electric field.

source capacitance, C_{ds}; gate-pad capacitance, C_{pg}; and drain-pad capacitance, C_{pd}. The values of C_{pg} and C_{pd} are topology dependent and circuit topologies involving additional elements have been described in [Backus-1976, Pulfrey-1978, Grebene-1969, Shockley-1962, and Golio-1991]. A complete common source AC equivalent circuit of a GaAs MESFET in the saturation region is shown in Figure (2.6). In Figure (2.6), circuit elements inside the box represent intrinsic elements of the device, whereas the other components are called extrinsic device components. The device equivalent circuit components are calculated by employing a set of equations given in following sections.

2.4.1. Parasitic Inductances

The parasitic inductances arise, primarily, from metal contact pads of the device [Golio-1991]. The values of these inductors are dependent upon the surface features of the device [Khalaf-2000 and Ladbrooke-1991]. For modern short gate length devices, L_g is usually the largest and a function of particular topology employed. The value of L_g is given as [Ladbrooke-1989]

the device [Khalaf-2000 and Ladbrooke-1991]. For modern short gate length devices, L_g is usually the largest and a function of particular topology employed. The value of L_g is given as [Ladbrooke-1989]

$$L_g \approx \frac{\mu_0 h Z}{m^2 L_G} \qquad (2.4.1)$$

where m is the number of parallel strips into which the total gate-width is divided, μ_0 is permeability of free space. The other inductances are L_d and L_s. Typically L_g and L_d are about 5 - 10 pH, whereas the magnitude of L_s is often small and about 1 pH. It is

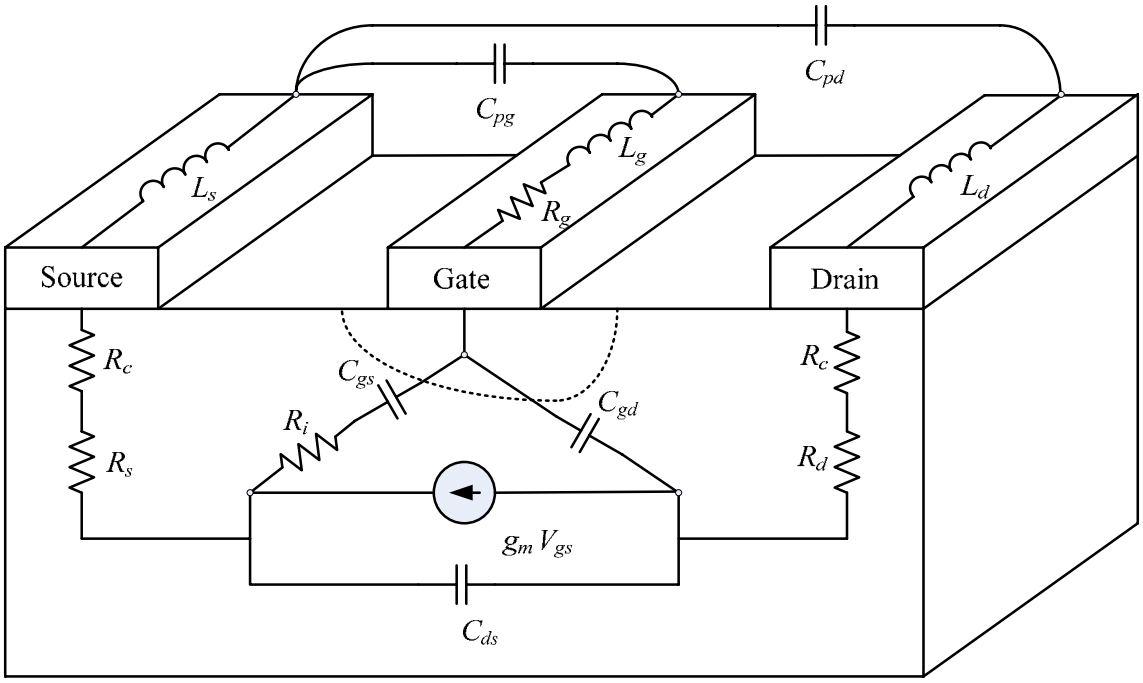


Figure (2.5): A cross-sectional view of a GaAs MESFET showing the origin of device electrical components.

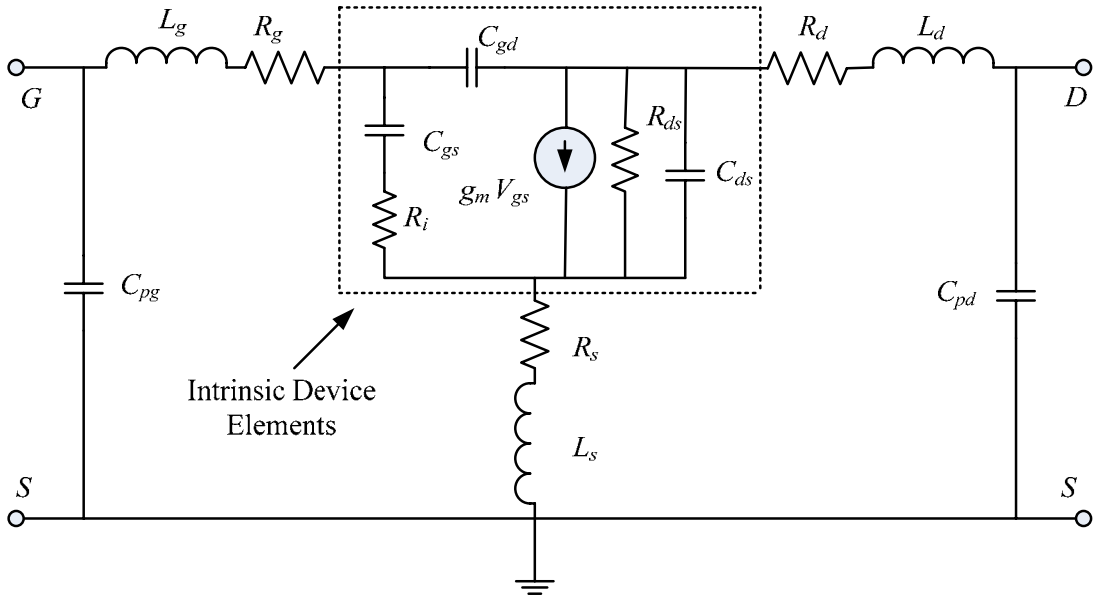


Figure (2.6): MESFET's small signal equivalent circuit in the saturation region of operation.

pertinent to mention that these inductances exist in addition to any parasitic bond wire inductance or parasitic package inductance, which must also be accounted for in the circuit model [Golio-1991]. In many cases, bond inductances are of the range of 100 - 300 pH and dominate in the device parasitic components.

2.4.2. Parasitic Resistances

Parasitic resistances are those which are closer to the terminals of a MESFET, i.e., along source, drain and the gate. The respective resistances are R_s, R_d and R_g. The R_s and R_d included R_c of the ohmic contacts as well as the bulk resistance of the device. These resistances are given as

$$R_s = R_c + \frac{L_{sg}}{q N_d \mu_0 a Z} \tag{2.4.2}$$

$$R_d = R_c + \frac{L_{gd}}{q N_d \mu_0 a Z} \tag{2.4.3}$$

where L_{sg} is source-to-gate length, L_{gd} is gate-to-drain length. R_g results from the metallization resistance of the gate Schottky contact and is given by

$$R_g = \frac{\rho Z}{3 m^2 H L_G} \tag{2.4.4}$$

where ρ is resistivity and H is the height of the gate strip. All three resistances reported in Equations (2.4.2) to (2.4.4) vary from 1-10 Ω for a modern microwave device [Tuzun-2006].

2.4.3. Intrinsic Capacitances

Referring the virtual source and drain electrodes as $s^{/}$ and $d^{/}$ as shown in Figure (2.7) then the symbols $V_{gs}^{/}$ will refer to the potentials between gate and $s^{/}$. The importance of these virtual electrodes is that their potential differs from the applied potentials due to voltage drops across L_{sg} and L_{gd} involved. It is, primarily, the potential between these virtual electrodes which govern the equivalent circuit elements of the intrinsic FET, and for that reason it is important that they be distinguished from the applied voltages at the contacts, i.e., V_{gs} and V_{gd}.

In Figure (2.7), there are three different regions. In Region I and II, the motion of electrons is governed by the part of the velocity- field characteristic, for which $0 < E < E_s$. Over this region, an increase in electric field strength results in an increase in electron drift velocity. At the end of Regions II, the electric field has reached the value E_s at which the electron drift velocity saturates and becomes independent of E. This condition persists until the end of Region III, at that point the x-directed channel field has dropped to values below E_s once more as shown in Figure (2.3).

Consider Region II, the total charge in this region is given by the expression [Ladbrooke-1991 and Ahmed (b)-1995]

$$Q_{II} \approx q\, N_d\, h\, L_G\, Z \tag{2.4.5}$$

If we take $V_{sg}^{/} = - V_{gs}^{/}$, then by definition the capacitance is

$$C_{II} \equiv C = \frac{\partial Q}{\partial V_{sg}^{/}} \approx q\, N_d L_G\, Z \frac{\partial h}{\partial V_{sg}^{/}} \tag{2.4.6}$$

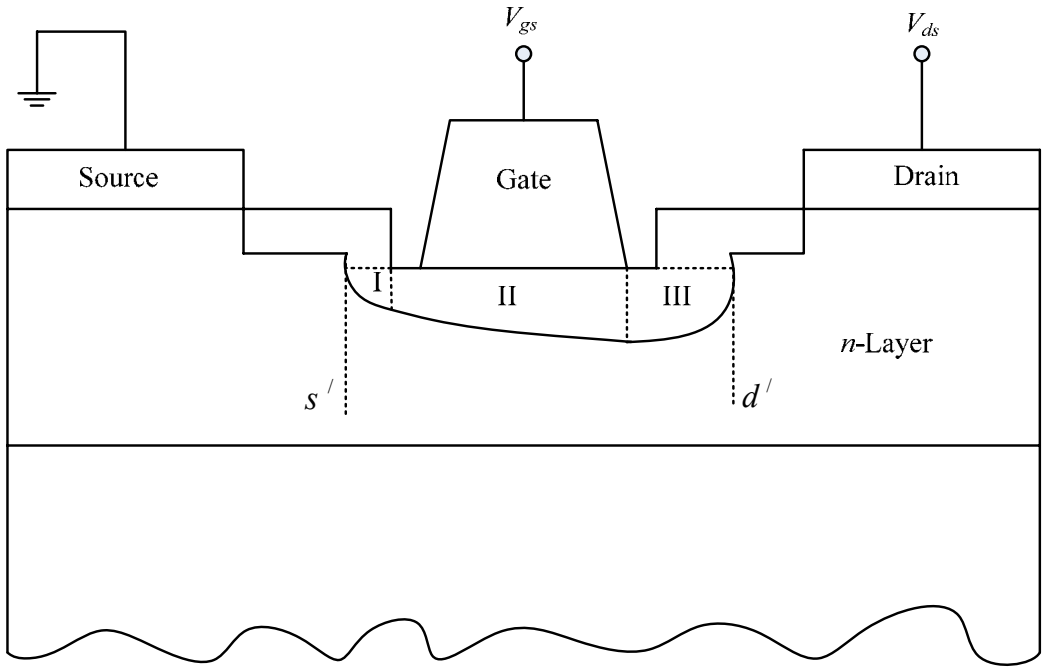


Figure (2.7): Depletion layer in an operating GaAs MESFET.

Since

$$\Phi_b + V'_{sg} \approx \frac{q N_d h^2}{2 \varepsilon_s} \tag{2.4.7}$$

By differentiating Equation (2.4.7) we get

$$\frac{\partial h}{\partial V'_{sg}} = \frac{\varepsilon_s}{q N_d h} \tag{2.4.8}$$

Therefore

$$C_{II} \approx \frac{\varepsilon_s L_G Z}{h} \tag{2.4.9}$$

This is a well known result which shows that the depletion layer capacitance below a Schottky contact behaves as a parallel-plate capacitor. Now consider Region I and III, the excess surface charges in these two regions are [Enoki-1990].

$$Q_I + Q_{III} \approx \frac{q N_d h^2 Z \pi}{2} \tag{2.4.10}$$

yields

$$C_I = C_{III} \approx \frac{\pi \varepsilon_s Z}{2} \ . \tag{2.4.11}$$

From the geometry of the channel shown in Figure (2.7) we can write

$$C_{gs} = C_I + C_{II} \tag{2.4.12}$$

and

$$C_{gd} = C_{III} \tag{2.4.13}$$

2.4.4. Channel Resistance

As a reasonable approximation for Region II shown in Figure (2.7), it is obvious that this region occupies most of the gate, so the length of Region II is equal to L_G. The potential drop in the channel is approximately $E_s L_G$, and the current flowing through this region is just the channel current, I_{ch}, therefore the DC resistance of the Region II is given as [Ahmed (b)-1995]

$$R_{dc} \approx \frac{E_s L_G}{I_{ch}} \tag{2.4.14}$$

It is convenient to eliminate E_s from the above expression in favor of more readily determined factors. Neglecting the effects of transverse fields for a moment, one can write

$$E_s \approx \frac{v_s}{\mu_e} \tag{2.4.15}$$

Taking into account the mobility degradation due to the transverse fields, μ_e is reduced by E_y, to about one third of its value [Ladbrooke-1989]. Therefore

$$E_s \approx \frac{3 v_s}{\mu_e} \tag{2.4.16}$$

so that

$$R_{dc} \approx \frac{3 v_s L_G}{\mu_e I_{ch}} \tag{2.4.17}$$

Since the AC resistance is one third of the DC resistance [Ladbrooke-1991], thus we obtain the equivalent value of channel resistance, R_i as

$$R_i \approx \frac{v_s L_G}{\mu_e I_{ch}} \tag{2.4.18}$$

2.4.5. Pad Capacitances

These capacitances are also included in the extrinsic part of the circuit model. The pad capacitances come from the stray capacitance between the metal pads. The pad capacitance consists of crossover capacitance of the metal lines and the capacitance between the pad and the back face of the semi-insulating substrate, which is usually connected to the source terminal. However, the crossover capacitance is usually much smaller than the substrate capacitance [Dilorenzo-1982].

Two pad capacitances are often included in the circuit model: C_{pg} and C_{pd}. Although the pad capacitance between gate and drain pads can be included in the circuit model, it is usually neglected for its small value compared to other capacitance values in the model. C_{pg} and C_{pd} are typically on the order of a few tens of fF.

2.4.6. Cut-Off Frequency

The cut-off frequency, f_T is defined as the frequency at which $\left| i_d / i_g \right|$ falls to unity under short circuit output conditions as shown in Figure (2.8). We have

$$i_d = g_m^{/} V_{gs}^{/} \tag{2.4.19}$$

where $g_m^{/}$ is called extrinsic transconductance given as

$$g_m^{/} = \frac{g_m}{1 + g_m R_s} \tag{2.4.20}$$

By applying Krichoff's law, we get

$$i_g = j\,\omega (C_{gs} + C_{gd}) V_{gs}^{/} \tag{2.4.21}$$

Equations (2.4.19) and (2.4.21) yields under unity gain condition

$$\left| \frac{i_d}{i_g} \right| = \frac{g_m^{/}}{\omega (C_{gs} + C_{gd})} \tag{2.4.22}$$

therefore

$$f_T = \frac{g_m^{/}}{2\pi (C_{gs} + C_{gd})} \ . \tag{2.4.23}$$

A full expression involving pad capacitances ($C_p = C_{pg} + C_{pd}$) for f_T is therefore given as

$$f_T = \frac{g_m^{/}}{2\pi (C_{gs} + C_{gd} + C_p)} \tag{2.4.24}$$

2.4.7. Transconductance Delay

Due to instantaneous changes in gate voltage the g_m cannot respond quickly. The delay inherent to this process is described by the transit time or transconductance delay, τ. Physically, the τ represents the time it takes for the charge to redistribute itself after the fluctuation of gate voltage [Golio-1991]. Typical value of τ is 1 p-sec for microwave MESFETs. τ tends to decrease when L_G decreases [Diamond-1982]. It is given by

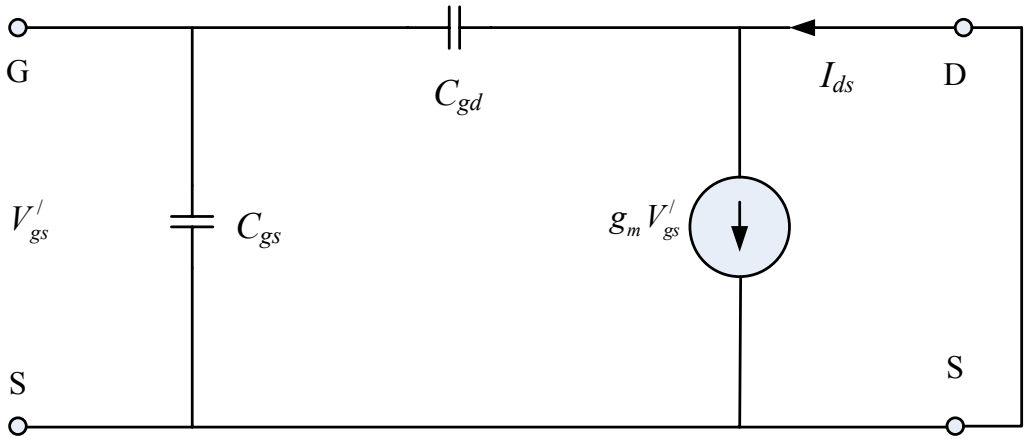


Figure (2.8): The equivalent circuit of a GaAs MESFET with short drain-source terminals.

$$\tau \approx \frac{C_{gs} + C_{gd}}{g_m^{/}} \qquad (2.4.25)$$

2.5. Summary

This chapter discusses the electrical response of submicron GaAs MESFETs. The output and transfer characteristics have been described as a function of device physical size. Long channel devices, i.e, $L_G > a$ have been explained with long channel MESFET model in which the channel pinches-off before attaining the saturation velocity. Whereas characteristics of microwave MESFETs ($L_g < a$) are discussed with velocity saturation model commonly known as short channel model.

The electrical response of the device has been explained by using its common source equivalent circuit. The parasitic and the intrinsic components of the circuit have been discussed in detail. Mathematical expressions linking the device equivalent circuit with its physics have been discussed to improve its modeling and understanding.

Chapter 3

Nonlinear GaAs MESFET's Models

3.1. Introduction

From applications and the fundamental research point of view, submicron GaAs MESFET's have been focus of interest. In high-tech analog and digital circuitry these devices are used due to their superior noise and gain properties. A number of different MESFET's models exist to predict their characteristics [Golio-1991 and Rodriguez-1992]. Usually these models are categorized based on the technique employed in their development. Broadly speaking, they may be classified as:

(a) Numerical models,

(b) Physical models.

Numerical models with rigorous field-dependent characteristics of carrier velocity in the channel, although more accurate, not suitable for use in circuit design programs due to their complexity and numerous parameters. A generally accepted DC model based on device fabrication parameters, called physical model, is preferred by the

design engineers provided it can predict the device characteristics to a reasonable accuracy [Golio-1991].

There are several physical models which are used in device simulators to predict MESFET characteristics [Curtice-1980, Kacprzak-1983, Statz-1987, McCamant-1990, Rodriguiz-1992, Ahmed (a)-1997, McNally-2001, Islam-2004 and Dobes-2004]. All these models assume an ideal Schottky barrier junction of the device having no interface states.

A direct way to enhance the high frequency capabilities of a MESFET is the reduction of its L_G [Enoki-1990] which inevitably causes a finite density of interface states at Schottky barrier [Ahmed-1995]. Furthermore, the reduction in L_G resulted into high g_d, compression in g_m and a shift in V_T of the device, called short channel effects [Ahmed (a)-1995]. The presence of short channel effects along with interface states makes the modeling more difficult and challenging. A model which accommodates all of these effects with minimum number of variables, but predicts *I-V* characteristics to a reasonable accuracy, will be a preferred model [Ahmed-1998]. In this chapter a comparative study of nine different nonlinear *I-V* FET models is presented. Accuracy of these models for submicron GaAs MESFETs is checked by simulating *I-V* characteristics and their comparison with experimental data. The simulation was carried out by developing a MATLAB tool whose operation is explained by a flow chart shown in Figure (3.1). Once a possible best fit for *I-V* characteristics is attained the values of g_m and g_d are then simulated by using their respective expressions.

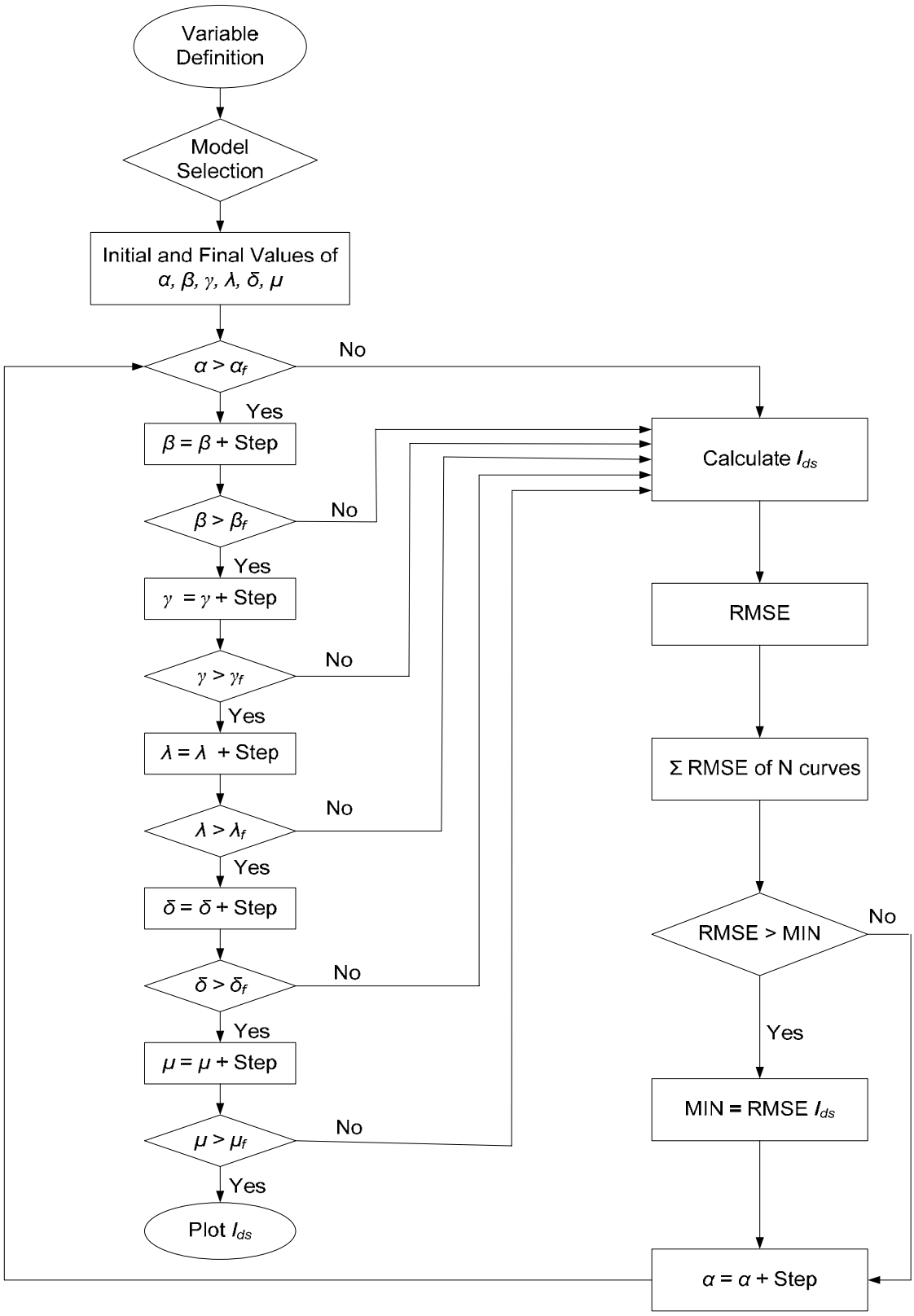


Figure (3.1): Optimization strategy to simulate output characteristics of GaAs MESFETs by using non-linear models.

3.2. Curtice Model

V. Tuyl *et al*. in 1974, proposed a FET model for circuit simulator [Van-1974]. The model was later modified by Curtice in 1980, which is now commonly known as Curtice FET model [Curtice-1980]. The Curtice model describes I_{ds} as a function of V_{ds} and V_{gs} as

$$I_{ds} = \beta (V_{gs} - V_T)^2 \times \tanh(\alpha V_{ds})(1 + \lambda V_{ds}) \qquad (3.2.1)$$

The variable α is used to simulate the linear region *I-V* characteristics, β is the transconductance parameter and λ predicts the dependence of I_{ds} on V_{ds} after the onset of the current saturation. Hyperbolic tangent function is used to simulate I_{ds} for $0 \leq V_{ds} \leq V_{breakdown}$ contrary to the Shockley model which simulates I_{ds} only for $V_{sat} \leq V_{ds} \leq V_{breakdown}$. The values of g_m and g_d based on Equation (3.2.1) are given, respectively, by

$$g_m = \frac{2I_{ds}}{V_{gs} - V_T}, \qquad (3.2.2)$$

and

$$g_d = I_{ds}\left[\frac{\lambda}{1 + \lambda V_{ds}} + \frac{2\alpha}{\sinh(2\alpha V_{ds})}\right]. \qquad (3.2.3)$$

Figure (3.2-a) shows the observed and the simulated *I-V* characteristics of a submicron GaAs MESFET. Examination of the figure reveals that Curtice model performance is relatively better in the linear region whereas it deteriorates significantly in the saturation region of operation. Thus, for submicron GaAs MESFETs the model performance is not within acceptable margin. The variations of

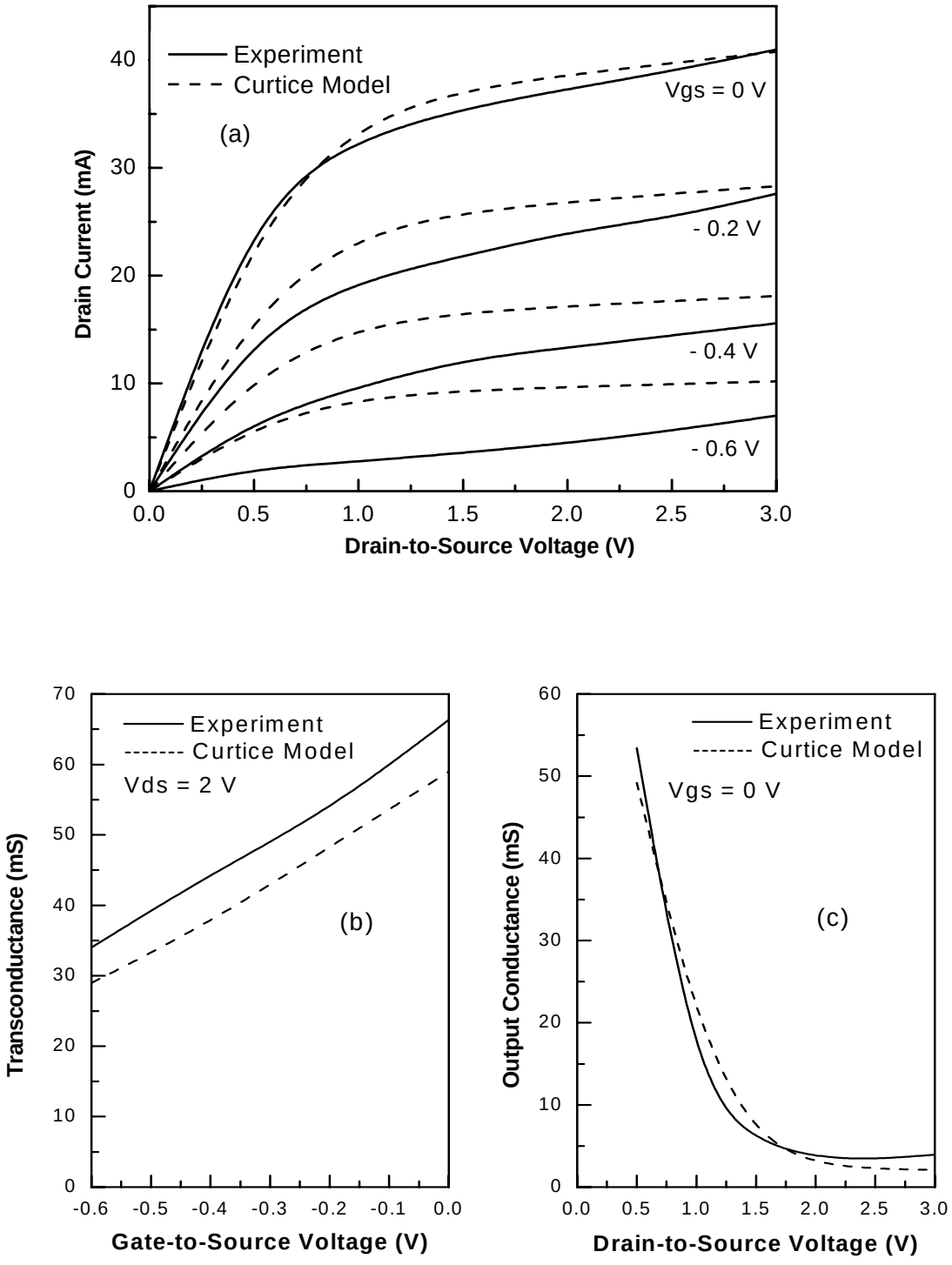


Figure (3.2): Observed and simulated characteristics of a 0.28 x 150 μm^2 GaAs MESFET by using Curtice nonlinear DC model (a) output *I-V* characteristics, (b) transconductance and (c) output conductance.

g_m and g_d by using Equations (3.2.2) and (3.2.3), in comparison with experimental data, are shown in Figures (3.2-b) & (3.2-c) respectively. Figure (3.2-c) shows a good agreement between the simulated and the observed characteristics, because at $V_{gs} = 0$, device *I-V* characteristics represent a good fit so does the value of g_d. On the other hand, the model does not predict good g_m (V_{gs}) values, for the device under consideration, as evident from the plot of Figure (3.2-b). Hence, one can conclude that Curtice model is not suitable to predict DC characteristics of a submicron GaAs MESFET.

3.3. Materka Model

The Materka model is based on the work proposed by Taki [Taki-1981]. However, V_T definition of Taki model is modified by Materka for its V_{ds} dependence and he proposed the following expression for I_{ds} (V_{gs}, V_{ds}) characteristics [Kacprzak-1983]

$$I_{ds} = I_{dss}\left[1 - \frac{V_{gs}}{V_T + \gamma V_{ds}}\right]^2 \times \tanh\left(\frac{\alpha V_{ds}}{V_{gs} - V_T - \gamma V_{ds}}\right). \qquad (3.3.1)$$

Whereas g_m and g_d of a FET device based on Equation (3.3.1) are given, respectively, by

$$g_m = 2 I_{ds}\left[\frac{\sinh\left(\frac{2\alpha V_{ds}}{V_{gs} - V_T - \gamma V_{ds}}\right) - 1}{\left(V_{gs} - V_T - \gamma V_{ds}\right)\sinh\left(\frac{2\alpha V_{ds}}{V_{gs} - V_T - \gamma V_{ds}}\right)}\right] \qquad (3.3.2)$$

and

$$g_d = 2I_{ds}\left[\left(1+\frac{1}{V_{gs}-V_T-\gamma V_{ds}}\right)+\frac{\gamma V_{gs}}{(V_T+\gamma V_{ds})\,(V_{gs}-V_T-\gamma V_{ds})}\right] \quad (3.3.3)$$

In Equation (3.3.1) the hyperbolic tangent function goes to unity for higher values of V_{ds} which is the case when $V_{ds} \geq V_{sat}$, then Equation (3.3.1) for $\gamma = 0$ is reduced to Shockley Equation (2.2.16). Hence, after the onset of current saturation Materka model expression is the same as that of Shockley square law expression.

In submicron GaAs MESFETs the value of g_d in saturation region is usually positive which eventually increases the value of V_T. Thus, in Materka model, $V_T + \gamma V_{ds}$ term is used to simulate the change in V_T as a function of V_{ds}.

Figure (3.3-a) represents *I-V* characteristics of a submicron GaAs MESFET. A poor match between the observed and the simulated characteristics demonstrates the failure of Materka model for submicron devices. This is, mainly, due to the inability of the model to simulate finite value of g_d in the saturation region which is usually observed in short channel MESFETs. The variation of g_m and g_d by using Equations (3.3.2) & (3.3.3), in comparison with experimental data, are shown in Figures (3.3-b) & (3.3-c) respectively. The plots of Figures (3.3-b) & (3.3-c) once again demonstrate the failure of the model especially in the saturation region.

3.4. Statz Model

In 1987, Statz *et al*. proposed a FET model to simulate I_{ds} (V_{ds}, V_{gs}) characteristics by using the following expression called Statz model [Statz-1987]

$$I_{ds} = (1+\lambda V_{ds})\left[\frac{\beta(V_{gs}-V_T)^2}{1+\delta\,(V_{gs}-V_T)}\right]\times\left[1-\left(1-\frac{\alpha V_{ds}}{3}\right)^3\right] \quad for \quad 0<V_{ds}<\frac{3}{\alpha} \quad (3.4.1)$$

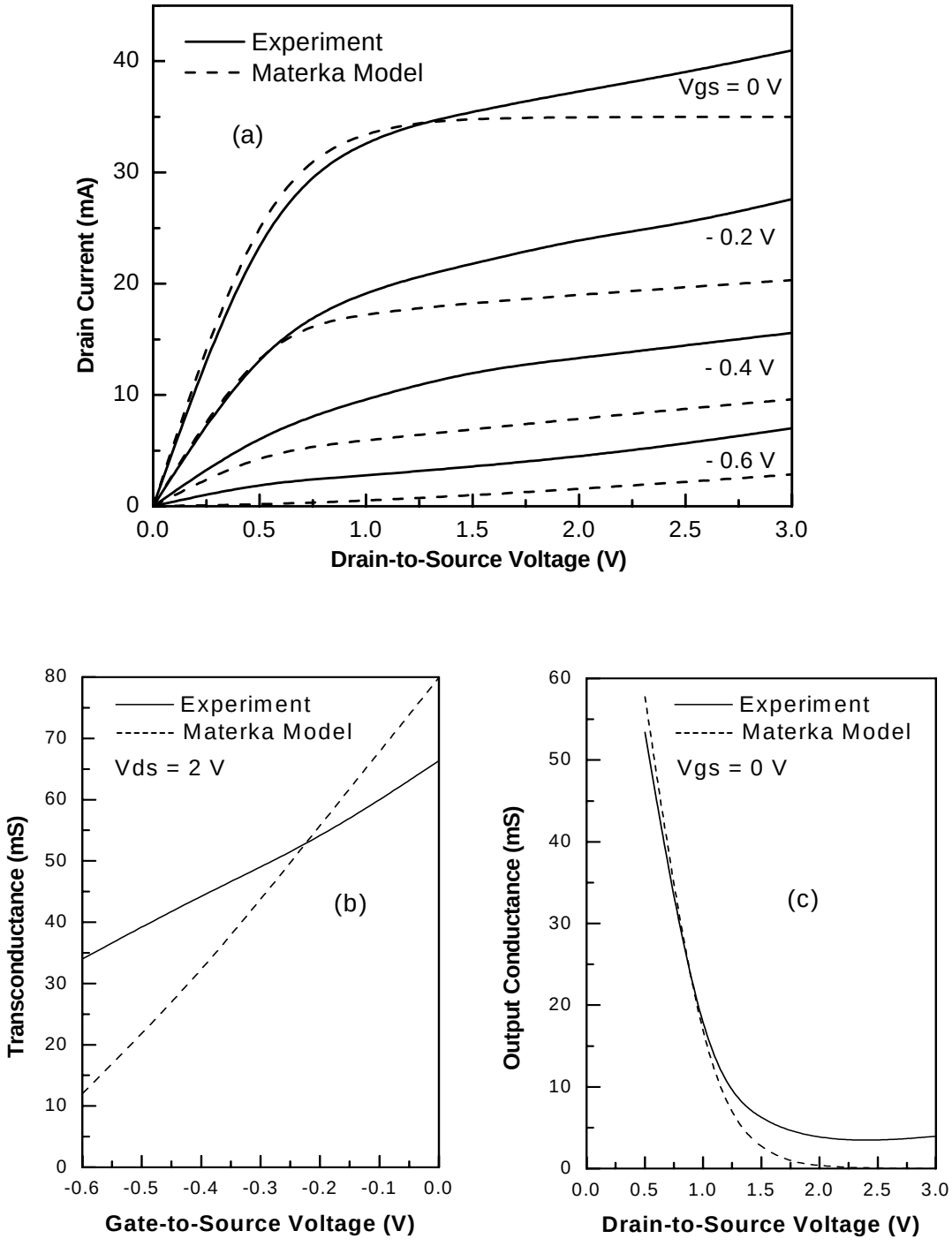


Figure (3.3): Observed and simulated characteristics of a 0.28 x 150 μm^2 GaAs MESFET by using Materka nonlinear DC model (a) output *I-V* characteristics, (b) transconductance and (c) output conductance.

$$I_{ds} = (1+\lambda V_{ds})\left[\frac{\beta(V_{gs}-V_T)^2}{1+\delta\,(V_{gs}-V_T)}\right] \qquad for \qquad V_{ds} \geq \frac{3}{\alpha} \tag{3.4.2}$$

where δ defines voltage range transition and other variables have usual meanings. The magnitude of g_m based on Equation (3.4.1) can be expressed as

$$g_m = \begin{cases} \dfrac{I_d}{\beta^2(V_{gs}-V_T)^2} & for \quad 0 < V_{ds} < \dfrac{3}{\alpha} \\ \dfrac{I_d}{\beta^2(V_{gs}-V_T)^2} & for \qquad V_{ds} \geq \dfrac{3}{\alpha} \end{cases} . \tag{3.4.3}$$

Whereas the variation of g_d as a function of V_{ds} and V_{gs} is given by

$$g_d = \begin{cases} \dfrac{\lambda I_{ds}}{1+\lambda V_{ds}} + \alpha I_d\left(1-\dfrac{\alpha V_{ds}}{3}\right)^2 & for \quad 0 < V_{ds} < \dfrac{3}{\alpha} \\ \dfrac{\lambda I_{ds}}{1+\lambda V_{ds}} & for \qquad V_{ds} \geq \dfrac{3}{\alpha} \end{cases} \tag{3.4.4}$$

where

$$I_d = I_{ds0}(1+\lambda V_{ds}) \tag{3.4.5}$$

and

$$I_{ds0} = \frac{\beta\,(V_{gs}-V_T)^2}{1+\delta\,(V_{gs}-V_T)} \tag{3.4.6}$$

The Statz model represented by Equation (3.4.1) for the simulation of output characteristics of a FET is fairly complicated in comparison with two models discussed in Sections 3.2 & 3.3. It is polynomial in nature and difficult to handle with. The basic parameters of a physical model have been dealt with in a complicated manner and the square law rule given by the Shockley equation has been violated.

Furthermore, the model also requires very stringent conditions for its applicability thus, making it inefficient and less user friendly.

Figure (3.4) represents the simulated and the observed characteristics for a submicron GaAs MESFETs. A poor match between the observed and the simulated characteristics demonstrates the inability of Statz model to predict the response of a submicron device. Examination of the figure showed that Statz model exhibited poor gate control which could be a main reason that caused a significant discrepancy as seen in all three plots of the figure.

3.5. McCamant Model

In 1990, McCamant *et al.* proposed an improved FET model for the device simulator [McCamant-1990] in which the variation of I_{ds} is given by

$$I_{ds} = \frac{I_{ds0}}{1 + \delta V_{ds} I_{ds0}} \tag{3.5.1}$$

Where

$$I_{ds0} = \begin{cases} \beta (V_{gs} - V_T - \gamma V_{ds})^n \left[1 - \left(1 - \frac{\alpha V_{ds}}{3} \right)^3 \right] & for \quad 0 < V_{ds} < \frac{3}{\alpha} \\ \beta (V_{gs} - V_T - \gamma V_{ds})^n & for \quad V_{ds} \geq \frac{3}{\alpha} \end{cases} \tag{3.5.2}$$

here n is an integer. Whereas g_m and g_d of a FET device based on Equation (3.5.2) are given, respectively, as

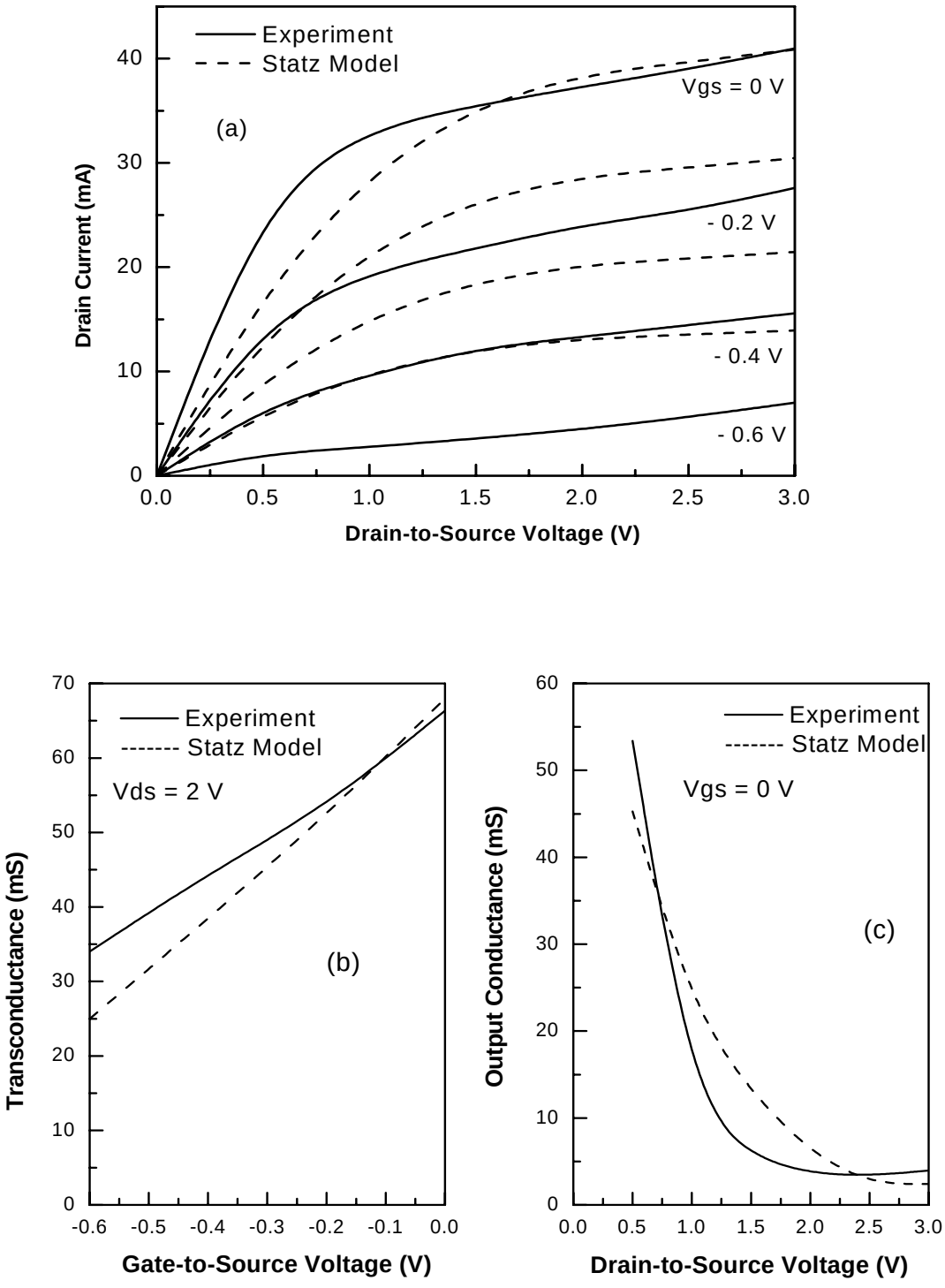


Figure (3.4): Observed and simulated characteristics of a 0.28 x 150 μm^2 GaAs MESFET by using Statz nonlinear DC model (a) output *I-V* characteristics, (b) transconductance and (c) output conductance.

$$g_m = \begin{cases} \dfrac{n I_{ds0}}{(1+\delta V_{ds} I_{ds0})(V_{gs} - V_T - \gamma V_{ds})} & for \quad 0 < V_{ds} < \dfrac{3}{\alpha} \\ \dfrac{n I_{ds0}}{(1+\delta V_{ds} I_{ds0})(V_{gs} - V_T - \gamma V_{ds})} & for \quad V_{ds} \geq \dfrac{3}{\alpha} \end{cases} \tag{3.5.3}$$

and

$$g_d = \begin{cases} \dfrac{I_{ds0}\left[\alpha\left(1 - \dfrac{\alpha V_{ds}}{3}\right)^2\right]}{(1+\delta V_{ds} I_{ds0})^2\left[1 - \left(1 - \dfrac{\alpha V_{ds}}{3}\right)^3\right]} - \dfrac{-\gamma n I_{ds0}}{(1+\delta V_{ds} I_{ds0})^2 (V_{gs} - V_T - \gamma V_{ds})} - \delta I_{ds}^2 & for \quad 0 < V_{ds} < \dfrac{3}{\alpha} \\ \dfrac{-\gamma n I_{ds0}}{(1+\delta V_{ds} I_{ds0})^2 (V_{gs} - V_T - \gamma V_{ds})} - \delta I_{ds}^2 & for \quad V_{ds} \geq \dfrac{3}{\alpha} \end{cases} \tag{3.5.4}$$

Figure (3.5) shows the simulation carried out by using McCamant model for a submicron MESFET. By examining the figure it is evident that the simulated output characteristics show a significant discrepancy relative to experimental data both in the linear as well as in the saturation region of operation. Furthermore, the simulated characteristics show a negative output conductance in the saturation region which is usually observed in long channel FETs. Based on the simulated results one can conclude that McCamant model is a poor choice for the prediction of DC characteristics of a microwave MESFET.

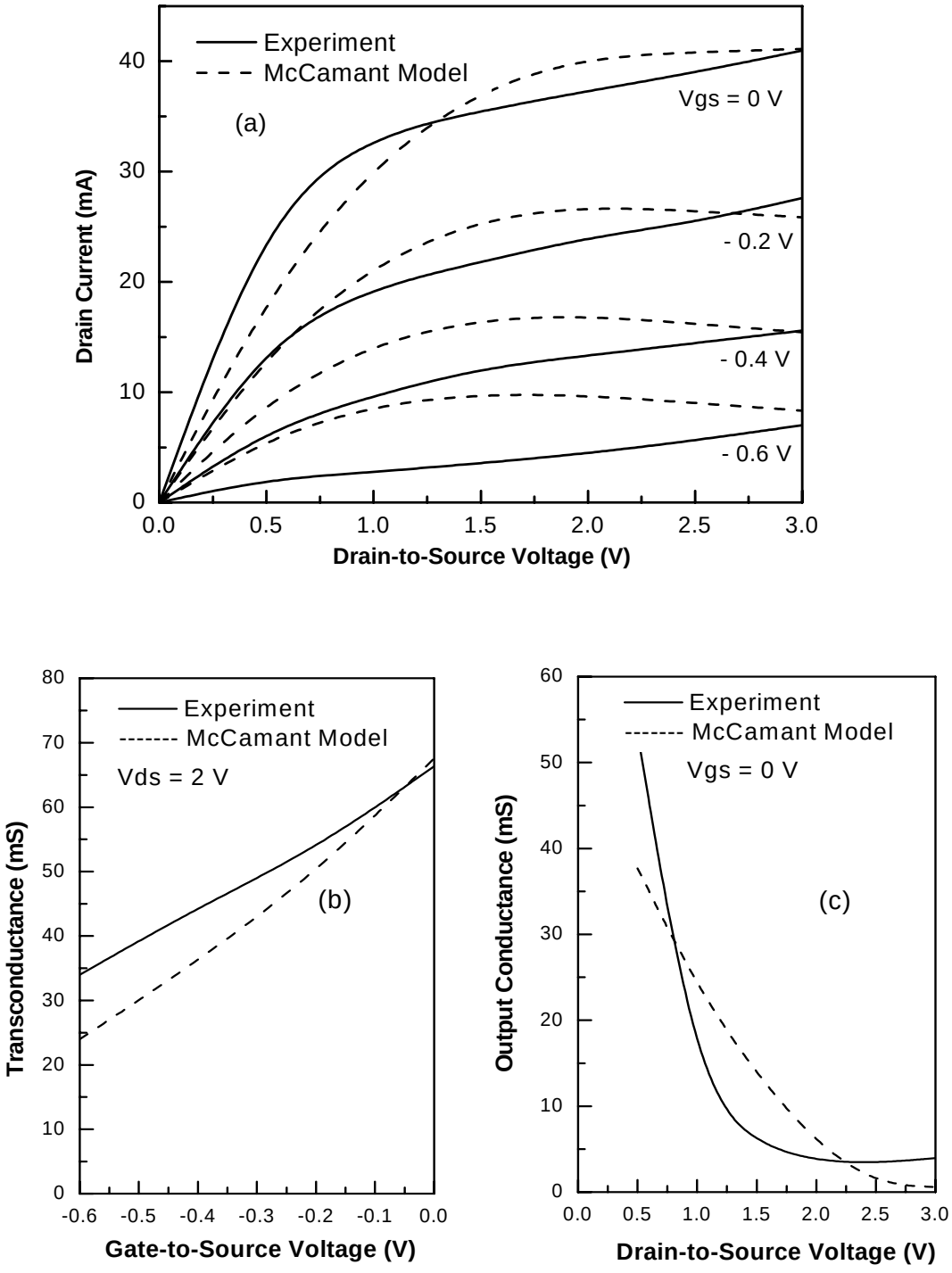


Figure (3.5): Observed and simulated characteristics of a 0.28 x 150 μm^2 GaAs MESFET by using McCamant nonlinear DC model (a) output *I-V* characteristics, (b) transconductance and (c) output conductance.

3.6. Rodriguiz Model

In 1992, Rodriguiz *et al*. proposed a model for the simulation of *I-V* characteristics of a MESFET defined by the expression [Rodriguiz-1992]

$$I_{ds} = \beta (V_{gs} - V_T - \gamma V_{ds})^2 \tanh(\alpha V_{ds}) (1 + \lambda V_{ds}) . \qquad (3.6.1)$$

Whereas g_m and g_d of a FET device based on Equation (3.6.1) are given, respectively, by

$$g_m = \frac{2 I_{ds}}{V_{gs} - V_T - \gamma V_{ds}} \qquad (3.6.2)$$

and

$$g_d = I_{ds} \left[- \frac{2\gamma}{V_{gs} - V_T - \gamma V_{ds}} + \frac{2\alpha}{\sinh(2\alpha V_{ds})} + \frac{\lambda}{1 + \lambda V_{ds}} \right] \qquad (3.6.3)$$

Equation (3.6.1) shows that it is an extended version of Curtice model in which only γV_{ds} term is added to improve the definition of V_T and to simulate its dependence on V_{ds}. Figure (3.6) shows the simulated and the observed characteristics for a submicron GaAs MESFETs by using Rodriguiz model. In this figure the characteristics show that Rodriguiz model performance is relatively better than those reported in subsequent sections. However, the model performance is still not within acceptable error limits usually permitted by the design softwares.

3.7. Ahmed Model

To simulate *I-V* characteristics for short channel GaAs MESFETs Ahmed *et al*. have proposed a model defined by the expression [Ahmed (a)-1997]

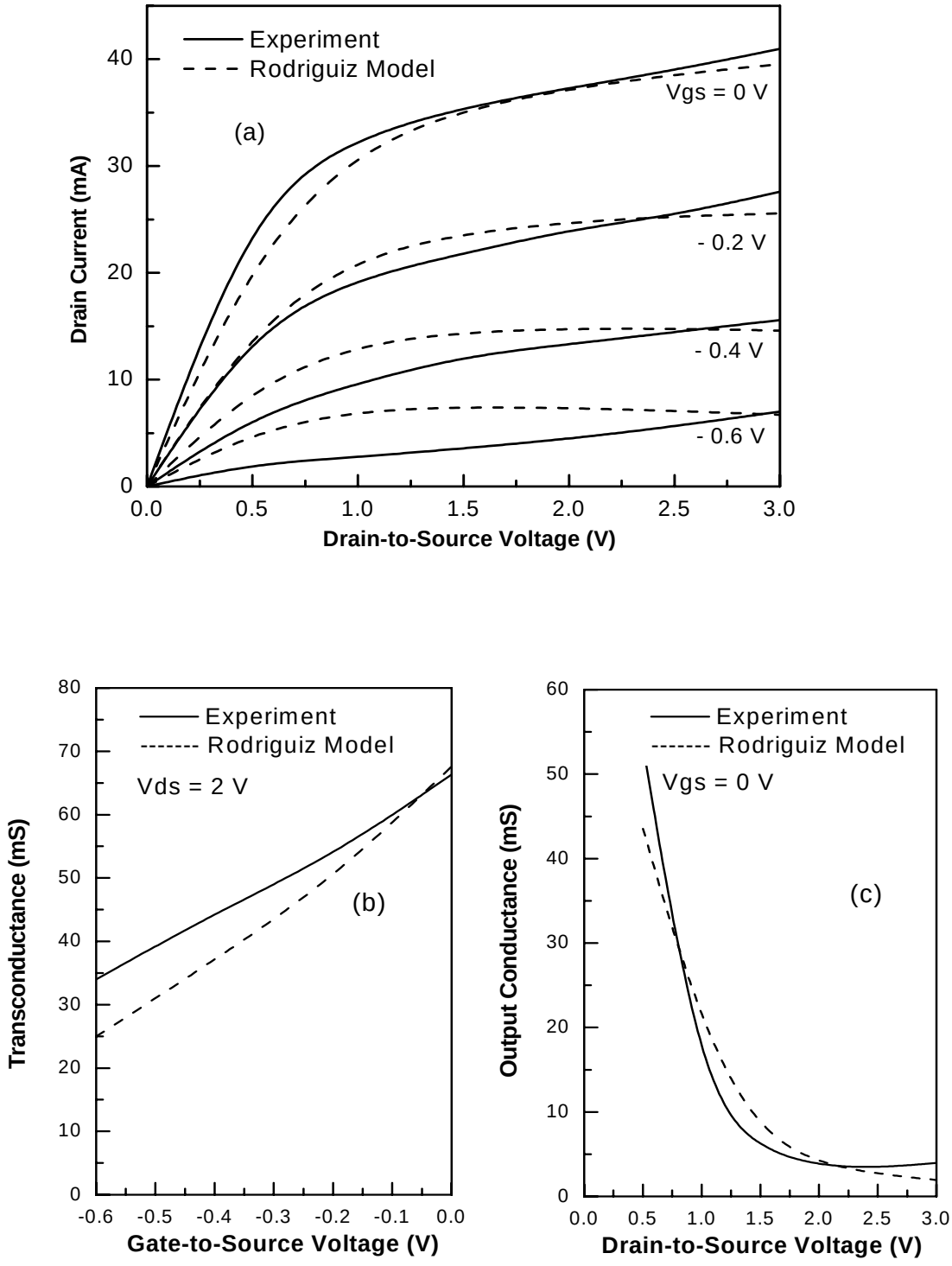


Figure (3.6): Observed and simulated characteristics of a 0.28 x 150 μm^2 GaAs MESFET by using Rodriguiz nonlinear DC model (a) output *I-V* characteristics, (b) transconductance and (c) output conductance.

$$I_{ds} = I_{dss}\left(1 - \frac{V_{gs}}{V_T + \Delta V_T + \gamma V_{ds}}\right)^2 \times \tanh(\alpha V_{ds})\,(1 + \lambda V_{ds})\,. \qquad (3.7.1)$$

According to simple one-dimensional device models, the value of V_T is independent of L_G [Ladbrooke-1989]. But in fact V_T is a function of L_G in short channel devices [Enoki-1990]. The main contribution of Ahmed model is that it has introduced a shift in V_T caused by the submicron geometry of the device into the model expression with a term ΔV_T defined by

$$\Delta V_T = \frac{4a}{3L_g} V_T\,. \qquad (3.7.2)$$

The variation in g_m and g_d of a FET device based on Equation (3.7.1), as a function of applied voltages are given, respectively, as

$$g_m = \frac{2\,I_{ds}}{V_{gs} - V_T - \Delta V_T - \gamma V_{ds}} = \frac{2(A-1)\,I_{ds}}{AV_{gs}}, \qquad (3.7.3)$$

and

$$g_d = \frac{\lambda I_{ds}}{1 + \lambda V_{ds}} + 2I_{ds}\left[\frac{\gamma V_{gs}}{(V_T + \Delta V_T + \gamma V_{ds})\,(V_{gs} - V_T - \Delta V_T - \gamma V_{ds})} + \frac{\alpha}{\sinh(2\alpha V_{ds})}\right]$$

$$= \frac{\lambda I_{ds}}{1 + \lambda V_{ds}} + 2I_{ds}\left[\frac{\gamma\,(A-1)^2}{AV_{gs}} + \frac{\alpha}{\sinh(2\alpha V_{ds})}\right] \qquad (3.7.4)$$

where

$$A = 1 - \frac{V_{gs}}{V_T + \Delta V_T + \gamma V_{ds}}\,. \qquad (3.7.5)$$

Figure (3.7) shows the simulated DC characteristics for a submicron GaAs MESFET by using Ahmed model. Comparing it with the earlier reported models, it is obvious that the performance of Ahmed model is significantly better than those models.

This may be attributed to the fact that this model is especially conceived keeping in view the device behavior at submicron level. The variation in g_m and g_d calculated by using Equations (3.7.3) & (3.7.4) are shown in Figures (3.7-b) & (3.7-c) respectively. Both the plots are self explanatory by showing that Ahmed model is accurate enough to be used in circuit simulation softwares.

3.8. McNally Model

In 2001, McNally *et al.* also proposed a DC model to simulate submicron GaAs MESFET characteristics [McNally-2001]. Its *I-V* characteristics expression is given as

$$I_{ds} = \left(\frac{\beta}{1+\mu(V_{gs} - V_T - V_{ds} - \Delta V_T)} \right) \times \left(1 - \frac{V_{gs}}{V_T + \gamma V_{ds} + \Delta V_T} \right)^2 \times \tanh(\alpha V_{ds})(1+\lambda V_{ds}) \tag{3.8.1}$$

where μ is another fitting variable having dimension as V^{-1}.

This model is an extension of Ahmed model in which I_{dss} term of Ahmed model has been replaced as

$$I_{dss} = \left(\frac{\beta}{1+\mu(V_{gs} - V_T - V_{ds} - \Delta V_T)} \right). \tag{3.8.2}$$

It is worth mentioning that this model has five fitting variables. This number is highest thus for reported by any model. This is considered a negative aspect of

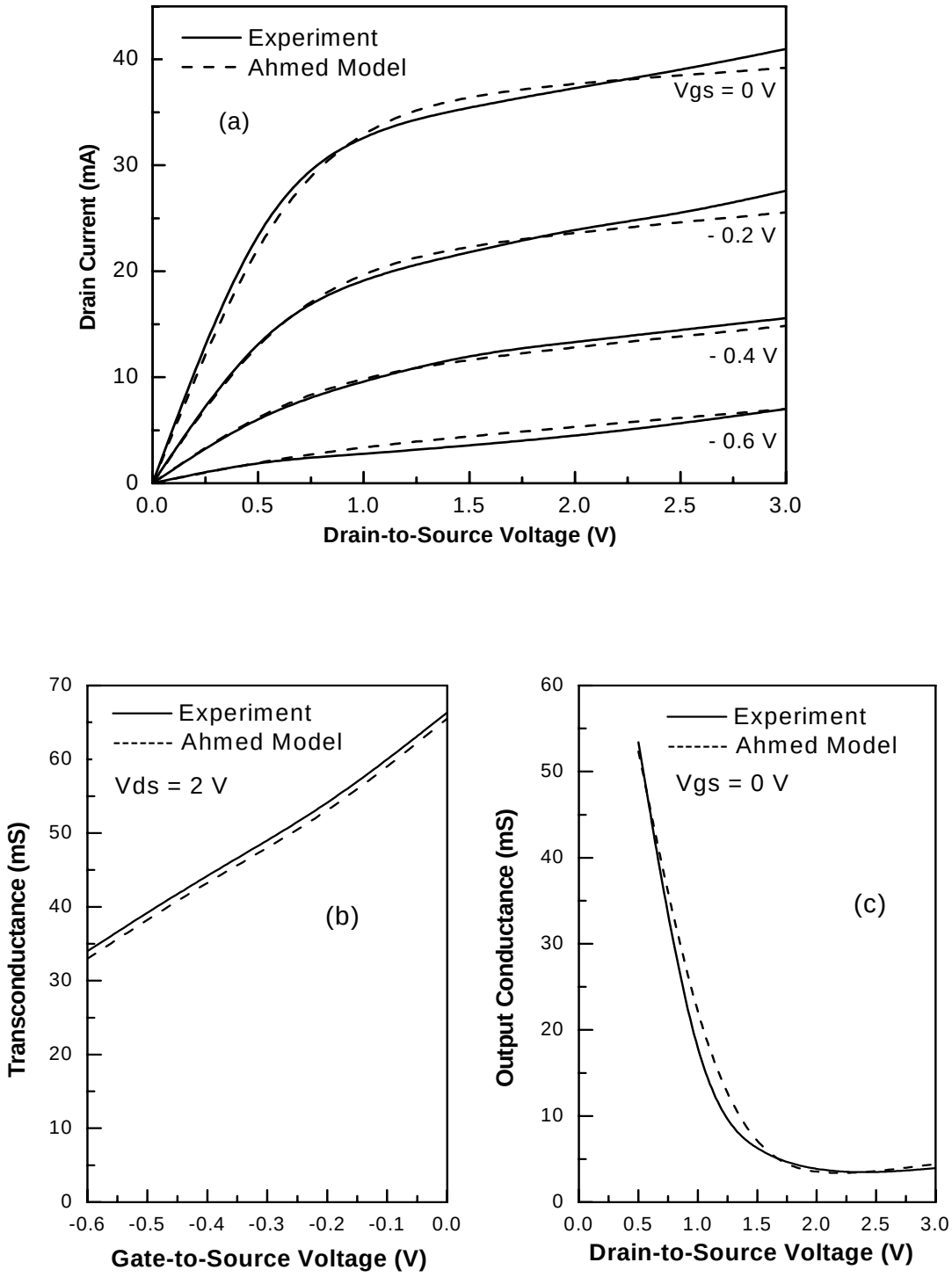


Figure (3.7): Observed and simulated characteristics of a 0.28 x 150 μm^2 GaAs MESFET by using Ahmed nonlinear DC model (a) output *I-V* characteristics, (b) transconductance and (c) output conductance.

modeling, because increasing the number of fitting variables would mean decreasing the dependence on the physical parameters of the device. And hence such model speaks minimum about the physical origin of different terms used in the model. So, it is highly difficult to predict device characteristics before its fabrication by employing its physical parameters.

The expressions for g_m and g_d of a GaAs MESFET device based on Equation (3.8.1) are thus given, respectively, by

$$g_m = I_{ds}\left[\frac{2(A-1)}{AV_{gs}} - \frac{\mu (AB)^2}{\beta}\right] \tag{3.8.3}$$

and

$$g_d = I_{ds}\left[\frac{2\gamma (A-1)^2}{AV_{gs}} + \frac{2\alpha}{\sinh(2\alpha V_{ds})} + \frac{\mu B}{\beta} + \frac{\lambda}{1+\lambda V_{ds}}\right] \tag{3.8.4}$$

where

$$B = \frac{\beta}{1+\mu (V_{gs} - V_T)}. \tag{3.8.5}$$

Figure (3.8-a) clearly shows that McNally model can be employed to simulate *I-V* characteristics of a submicron MESFETs to a reasonable accuracy but on expense of high number of fitting variables. Furthermore, Figures (3.8-b) & (3.8-c) also confirm the model ability to simulate g_m and g_d of a short channel device with good conformity to experimental data.

3.9. Islam Model

In 2004, Islam *et al.* proposed a model, to simulate DC characteristics of

Submicron GaAs MESFETs, whose expression for *I-V* response is given as [Islam-2004]

$$I_{ds} = I_{dss}\left(1 - \frac{V_{gs}}{V_T + \Delta V_T + \gamma V_{ds}}\right)^2 (1 + \lambda V_{ds} + \mu V_{gs}) \tanh(\alpha V_{ds}) \ . \quad (3.9.1)$$

This model is once again an extension of Ahmed model, where $(1 + \lambda V_{ds})$ term of Ahmed model has been modified as $(1 + \lambda V_{ds} + \mu V_{gs})$. The introduction of an extra variable in Islam model made it more complex than Ahmed model.

The expressions for g_m and g_d of a GaAs MESFET device based on Equation (3.9.1) are given, respectively, as

$$g_m = I_{ds}\left[\frac{2(A-1)}{AV_{gs}} + \frac{\mu}{C}\right] \quad (3.9.2)$$

and

$$g_d = I_{ds}\left[\frac{2\gamma(A-1)^2}{AV_{gs}} + \frac{2\alpha}{\sinh(2\alpha V_{ds})} + \frac{\lambda}{C}\right] \quad (3.9.3)$$

Where

$$C = 1 + \lambda V_{ds} + \mu V_{gs} . \quad (3.9.4)$$

To see the validity of Equation (3.9.1), *I-V* characteristics of a submicron GaAs MESFETs have been simulated and the result is shown in Figure (3.9).

Comparing Figures (3.7), (3.8) & (3.9), one can clearly see that there is not much apparent difference in the performance of these three models i.e., Ahmed,

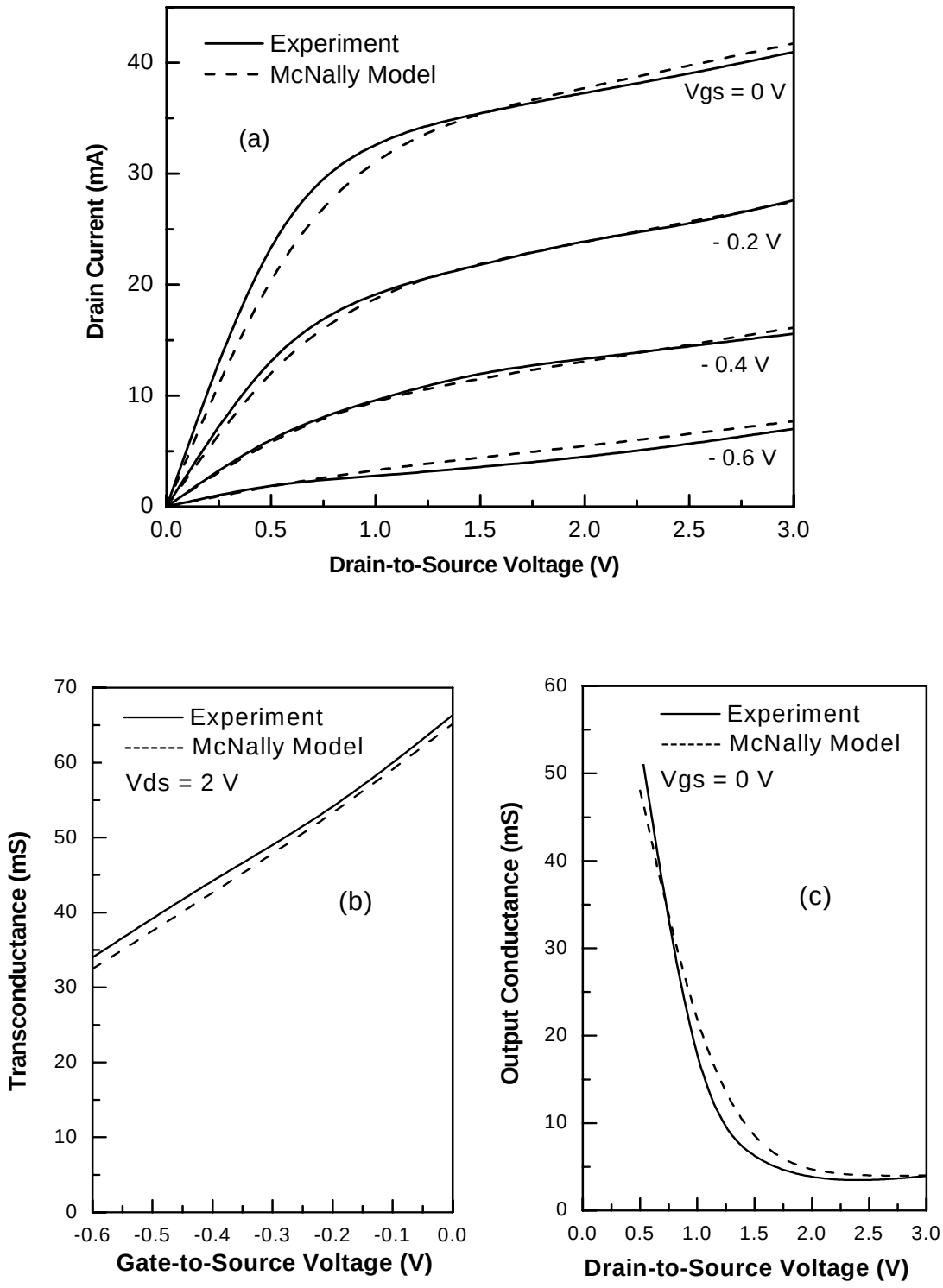


Figure (3.8): Observed and simulated characteristics of a 0.28 x 150 μm^2 GaAs MESFET by using McNally nonlinear DC model (a) output *I-V* characteristics, (b) transconductance and (c) output conductance.

McNally and Islam models. Thus the Ahmed model, which provides a foundation to the other two models under discussion, still appears to be a better option for short channel FET simulation due to its reasonably accuracy with less number of variables.

3.10. Dobes Model

In 2004, Dobes *et al*. converted the Rodriguiz model expression defined in Equation (3.6.1) to a new form by changing its square to a variable *n* [Dobes-2004]. I_{ds} (V_{gs}, V_{ds}) expression for this model is given as

$$I_{ds} = \beta\,(V_{gs} - V_T - \gamma V_{ds})^n \times \tanh(\alpha V_{ds})\,(1 + \lambda V_{dS}) \qquad (3.10.1)$$

The value of *n* shall be chosen that provides best fit between the simulated and the observed characteristics. In Equation (3.10.1) there are five fitting variables used in Dobes model, which, makes it less user friendly as that of Rodriguiz and other models.

The expressions for g_m based on Equation (3.10.1) can be written as

$$g_m = \frac{nI_{ds}}{V_{gs} - V_T - \gamma V_{ds}}\,. \qquad (3.10.2)$$

whereas the variation in g_d for Dobes model is

$$g_d = I_{ds}\left[-\frac{n\gamma}{V_{gs} - V_T - \gamma V_{ds}} + \frac{2\alpha}{\sinh(2\alpha V_{ds})} + \frac{\lambda}{1 + \lambda V_{ds}} \right] \qquad (3.10.3)$$

Figure (3.10) represents the best possible fit attained by using Dobes model for a submicron GaAs MESFET characteristics. An apparent examination of the figure clearly shows that the model under discussion is not suitable to predict *I-V*

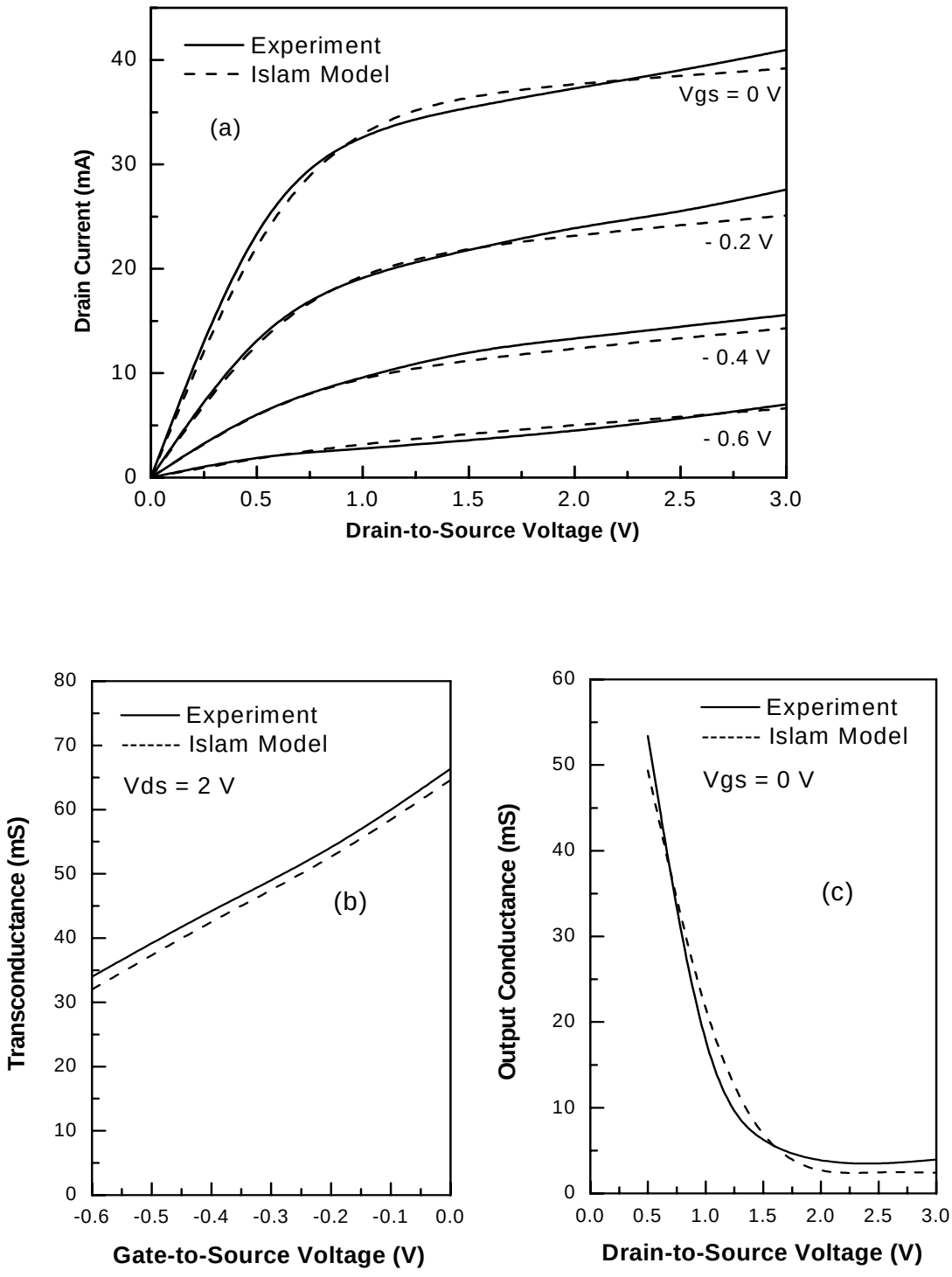


Figure (3.9): Observed and simulated characteristics of a 0.28 x 150 μm^2 GaAs MESFET by using Islam nonlinear DC model (a) output *I-V* characteristics, (b) transconductance and (c) output conductance.

characteristics of a short channel MESFET.

3.11. Root Mean Square (RMS) Error

RMS error values were calculated at different V_{gs} and V_{ds} voltages for the models under consideration as given in Table-3.1 and Table-3.2 respectively. It has been observed that Ahmed model offers lowest RMS errors both as a function of V_{gs} as well as V_{ds}, i.e., 0.80 and 0.96 respectively, whereas the worst observed case is the Statz model whose average RMS errors as a function V_{gs} and V_{ds} were 4.8 and 5.6 respectively. McNallay and Islam models offered RMS errors which are close to Ahmed model. This shows that one of these three models could be a suitable choice for submicron device simulation tools. However, amongst those Ahmed model performance is the best observed one for short channel GaAs MESFETs. Furthermore, Ahmed model has less number of fitting variables compared with McNally and Islam models. Thus, it should be a preferred model for submicron GaAs MESFET simulation tools.

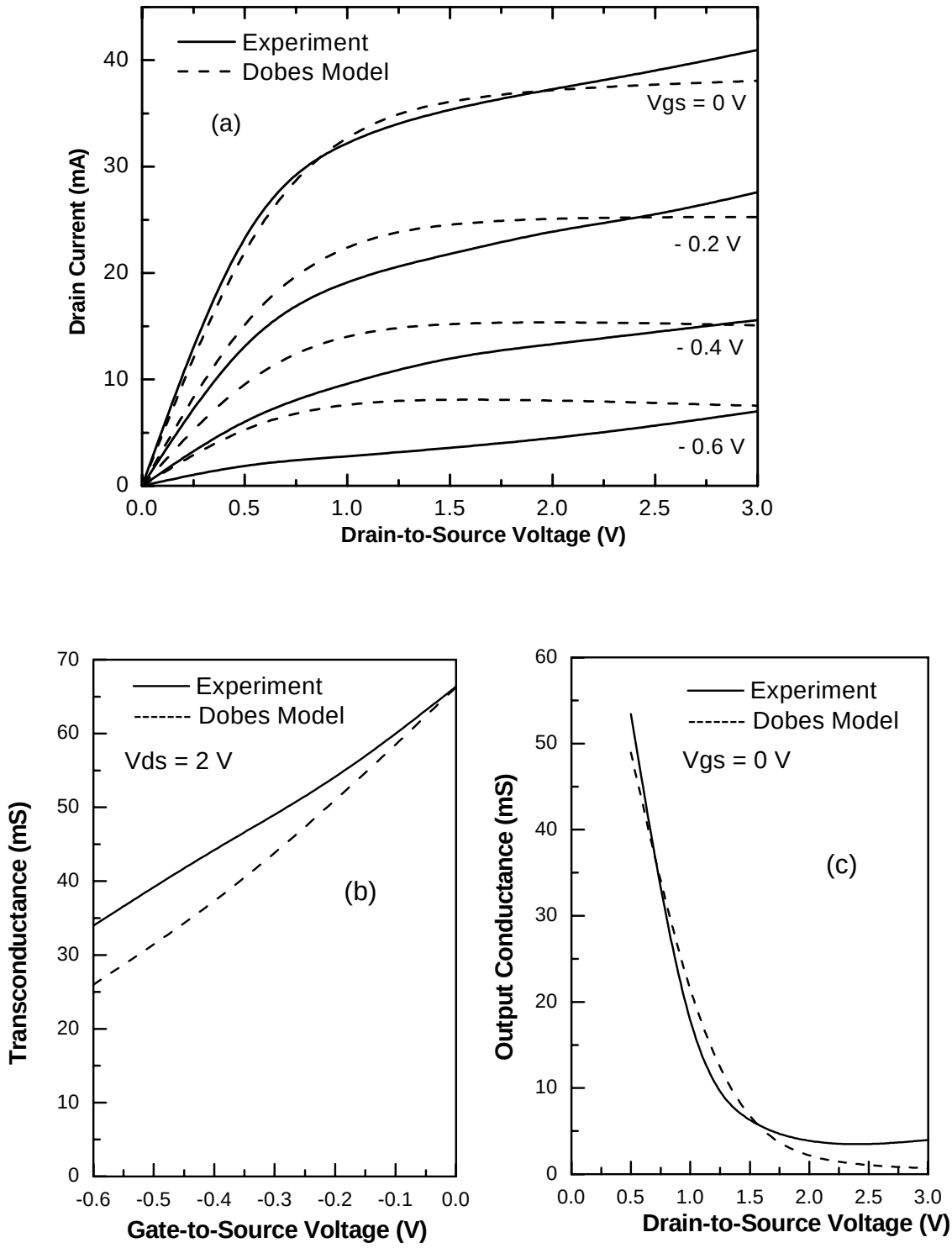


Figure (3.10): Observed and simulated characteristics of a 0.28 x 150 μm^2 GaAs MESFET by using Dobes nonlinear DC model (a) output *I-V* characteristics, (b) transconductance and (c) output conductance.

Table - 3.1
Comparison of RMS errors of different MESFET models as a function of V_{gs}.

S. No.	Model	RMS error at different V_{gs} values				Average Error
		V_{gs} = -0.6	V_{gs} = -0.4	V_{gs} = -0.2	V_{gs} = 0.0	
1	Curtice	4.45	3.77	2.75	1.31	3.07
2	Materka	2.75	4.52	4.29	3.02	3.64
3	Statz	6.82	5.37	3.28	3.74	4.80
4	McCamant	4.33	3.07	2.19	3.44	3.25
5	Rodriguiz	2.77	2.04	1.32	2.00	2.03
6	Ahmed	0.56	0.48	0.93	1.23	0.80
7	McNallay	0.70	0.35	0.61	1.66	0.83
8	Islam	0.40	0.81	1.14	1.23	0.89
9	Dobes	3.37	2.80	2.17	1.54	2.47

Table - 3.2
Comparison of RMS errors of different MESFET models as a function of V_{ds}.

S. No.	Model	RMS error at different V_{ds} values				Average Error
		V_{ds} = 0.5	V_{ds} = 1.5	V_{ds} = 2.5	V_{ds} =3.0	
1	Curtice	3.35	4.21	2.92	2.07	3.14
2	Materka	1.73	3.45	4.82	5.94	3.98
3	Statz	4.72	6.70	6.00	5.00	5.60
4	McCamant	4.09	4.67	2.07	1.22	3.00
5	Rodriguiz	3.23	2.44	0.78	1.35	1.95
6	Ahmed	1.04	0.82	0.61	1.39	0.96
7	McNallay	2.24	0.53	0.61	0.59	0.99
8	Islam	1.08	0.81	0.86	1.66	1.10
9	Dobes	3.19	3.16	1.32	1.89	2.39

3.12. Summary

In this chapter nine different FET models are presented and their validity for the simulation of DC characteristics of submicron GaAs MESFETs has been checked by developing a software tool. The presented models have been analyzed and discussed by considering the variables involved in their definition along with fitting variables. To demonstrate the validity of a model for short channel MESFET, a 0.28 x 150 μm^2 device is selected and then its DC characteristics are compared with the simulated data. The accuracy of a model is then assessed by evaluating its RMS error values as a function of V_{gs} and V_{ds}. It is noted that Ahmed model offers best simulation results compare to other available models, whereas, the simulated results of McNally and Islam models are close to Ahmed model.

Chapter 4

Effects of Interfacial Layer on Submicron GaAs MESFET's Characteristics

4.1. Introduction

GaAs FETs have been widely used both in microwave and digital applications because of their superior speed. The simplest way to improve the device performance is by reducing the value of L_G [Das-1988, Bernstein-1988 and Golio-1991]. However, several important so-called short-channel effects are observed in short channel devices [Adams-1991, Trabelsi-1991, Watts-1989 and Jaeckel-1986]. These effects limit the performance of the device by reducing g_m and by increasing g_d. Both of these effects usually cause a shift in V_T. Increase in g_d and decrease in g_m by decreasing L_G of the device, in the saturation regime of operation, may be associated with V_{ds} dependent Schottky barrier lowering caused by the field lines vertical to the flow of the current. These field lines are generated by uncompensated depletion ions on the drain side of the device [Ahmed-1997] which has a significant contribution in the total depletion, especially when L_G is small.

Furthermore, if the interface of a Schottky barrier has a finite density of states it causes another Schottky barrier lowering and hence a further reduction in g_m of the device is observed [Akkilic-2006, Chen-2006, Kilicoglu-2006 and Ahmed-1997]. This Schottky barrier lowering reduces the value of Φ_b and thus increases the gate leakage current, I_g. The quality of a Schottky barrier and the thickness of interfacial layer may be assessed by observing the magnitude of I_g from the device *I-V* characteristics [Chen-2006, Jang-2002 and Ahmed-1997]. This chapter describes the dependence of GaAs MESFET output and transfer characteristics on the quality of Schottky barrier assessed from its electrical behavior.

4.2. Effect of Interface States

In a simple Schottky-Molt theory the barrier height, Φ_b should depend on the metal work function, Φ_m and given by the relation [Cowley-1965, Ahmed (b)-1995 and Kumar-2006]

$$\Phi_b = \Phi_m - \chi \qquad (4.2.1)$$

where χ is the electron affinity of the semiconductor as shown in Figure (4.1). In this figure the energies of conduction and valance bands are represented by E_c and E_v respectively while E_g shows the band gap. In most practical metal-semiconductor contacts, this situation is never reached because there is usually a thin insulating layer of oxides on the surface of the semiconductor [Tahsin-2005 and Aydin-2004]. Such an insulating film is often known as interfacial layer. Experimentally, it is found that Φ_b is less sensitive function of Φ_m and under certain circumstances; Φ_b may be almost independent of choice of the metal [Ahmed (b)-1995].

An explanation of this weak dependence of Φ_b on Φ_m was put forward by

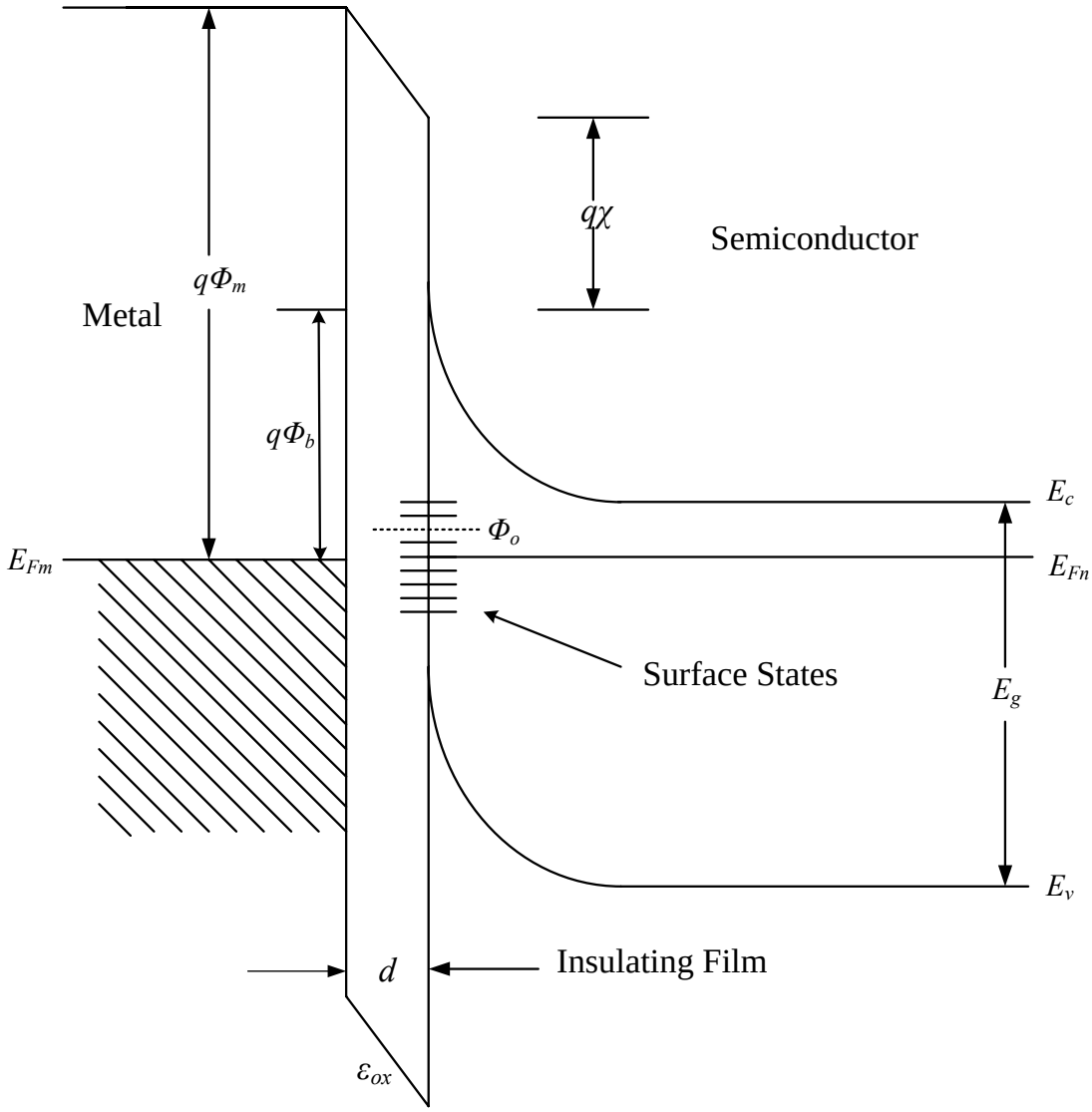


Figure (4.1): Energy band diagram of a Schottky barrier having finite density of surface states.

[Bardeen-1947], who suggested that the discrepancy may be due to the effects of interface states. According to Bardeen, the metal and the semiconductor remain separated by a thin insulating layer as shown in Figure (4.1), and there is a continuous distribution of surface states present at the interface which are characterized by Φ_0.

Since the junction as a whole is electrically neutral, therefore, in the absence of interface states, the negative charge, Q_m on the surface of the metal must be equal and opposite to the positive charge, Q_d in the semiconductor caused by the uncompensated donors [Ladbrook-1991, Cowley-1965 and Ahmed (b)-1995]. But in the presence of interface states, the neutrality condition becomes

$$Q_m + Q_d + Q_{ss} = 0 \qquad (4.2.2)$$

where Q_{ss} is the charge in the interface states [Ahmed-(b)-1995]. The occupancy of the surface is determined by the Fermi level, E_F, which is constant throughout the region in the absence of the applied bias and represented by E_{Fn} and E_{Fm} in semiconductor and metal respectively are shown in Figure (4.1). If Φ_0 happens to be above E_{Fn} as shown in Figure (4.1), the surface states contains a net positive charge and Q_d must therefore, be smaller than if surface states were absent [Park-2005]. This means that the width of the depletion region will correspondingly be reduced and hence the Φ_b [Tataroglu-2005]. On the other hand, if Φ_0 happens to be below E_{Fn}, Q_{ss} is negative and Q_d must be greater than if surface states were absent. This means that the depletion width and Φ_b both will be increased.

4.3. Evaluation of Interfacial Layer Thickness

The current flowing through a Schottky barrier of a GaAs MESFET having interfacial layer is a space charge limited current (SCLC) controlled by the Schottky

depletion [Ahmed-1997]. However, the portion of V_{gs} drop across the interfacial layer is on the expense of reduced gate depletion. Hence, the depletion height of a Schottky barrier having an interfacial layer will be relatively lower than an ideal interface under the same biasing conditions [Karatas-2005, Aydin-2004]. Whereas, the potential drop, V_i, across the interfacial layer can be expressed as [Zeghbroeck-2004]

$$V_i = \frac{qN_d x_d d}{\varepsilon_{ox}} \tag{4.3.1}$$

where d is the interfacial layer thickness, ε_{ox} is its permittivity and x_d is depletion layer thickness in the semiconductor.

It is assumed that the interfacial layer is thick enough to hold finite potential across it and on the other hand is transparent enough to permit the carriers to move across [Kilicoglu-2005, Okutan-2005, Karatas-2005 and Cetin-2005]. If μ_{ox} is the mobility of the free carriers under the applied electric field E, then the current density J crossing interfacial layer is given by [Zeghbroeck-2004]:

$$J = qN_d \mu_{ox} E \tag{4.3.2}$$

Combining Equation (4.3.2) with one dimensional Poisson's equation one gets:

$$\frac{J}{\varepsilon_{ox}\mu_{ox}} = \varepsilon_{ox} \frac{dE}{dx} \tag{4.3.3}$$

which after the integration yields

$$J = \frac{9}{8} \frac{\varepsilon_{ox}\mu_{ox} V_i^2}{d^3} \tag{4.3.4}$$

and

$$d = \left[\frac{8}{9} \frac{J}{\varepsilon_{ox}\mu_{ox} V_i^2} \right]^{1/3} \tag{4.3.5}$$

The value of d could be evaluated by knowing μ_{ox} and V_i for a given biasing.

4.4. Thermionic Emission With Interfacial Layer

According to the thermionic-emission theory of Schottky barriers, the reverse current density of an ideal Schottky barrier should saturate at the value predicted by [Sze-1981]

$$J_o = A^{**} T^2 \, Exp\left(-\frac{q\Phi_b}{kT}\right) \qquad (4.4.1)$$

where k is Boltzmann's constant, T is the absolute temperature, q is the electronic charge and A^{**} is the effective Richardson constant for thermionic emission. The presence of a high density of interface states at a Schottky barrier contributes to non-ideality in the I–V characteristics because, the interface states give rise to parallel processes of current flow via capture and emission of electrons passing through the barrier [Aydin-2004, Karatas-2005 and Cetin-2005]. The trapping of charges in the interface states reduces the barrier height and is a common cause of the soft reverse characteristics of a Schottky contact [Wu-1982, Rhoderick-1988 and Ladbrooke-1973].

Card and Rhoderick have shown that the reverse current of a Schottky junction with a fairly thick interfacial layer may actually be greater than that of a Schottky barrier with a very thin layer because of the reduction in Φ_b [Card-1971]. Although the electrons have to tunnel through a thicker insulator, this layer is still relatively thin and is overcompensated by the reduction in the Schottky barrier height. The magnitude of interface current is, of course, dependent on the density of interface states, and also on the probability that an electron in an interface state can tunnel into the metal [Saha-2004].

Figure (4.2) represents the energy band diagram of a Schottky barrier under non equilibrium conditions where a potential V_R is applied to semiconductor having barrier height, V_{bi}. The diagram explicitly shows the consumption of V_{gs} in the form of V_i at the interface due to finite oxide layer thickness. This consumption will then reduce the band bending and hence the barrier height. Thus, the potential which will alter the gate depletion is $|V_{gs}| - V_i$.

Thermionic emission current density of a Schottky diode, based on the concept of potential drop across the interfacial layer, is given by [Wu-1982].

$$J = J_o \, \theta_n \, Exp\left(-\frac{q V_i}{k T}\right)\left[Exp\left(-\frac{q V_{gs}}{k T}\right) - 1\right] \qquad (4.4.2)$$

where θ_n is the transmission coefficient of electrons across the interfacial layer. Equation (4.4.2) shows that V_i will give additional barrier lowering which together with the image force lowering will eventually increase the reverse current of a Schottky diode.

According to Wu [Wu-1982] there are three factors which increase the reverse current of a Schottky diode: (a) the image force lowering of Φ_b; (b) the presence of V_i,and (c) the voltage dependence of the diffusion velocity. It is an established fact that reverse current of a Schottky barrier is a function of V_i, and its magnitude indicates the quality of the interface [Altindal-2003 and Ahmed-1995].

4.5. Effects of Interfacial layer on MESFETs Characteristics

To evaluate the effects of interfacial layer on submicron GaAs MESFETs characteristics, five devices fabricated on the same wafer have been selected. These devices have the same Schottky barrier gate length but with different electrical response. According to established MESFET models, the value of V_T is independent

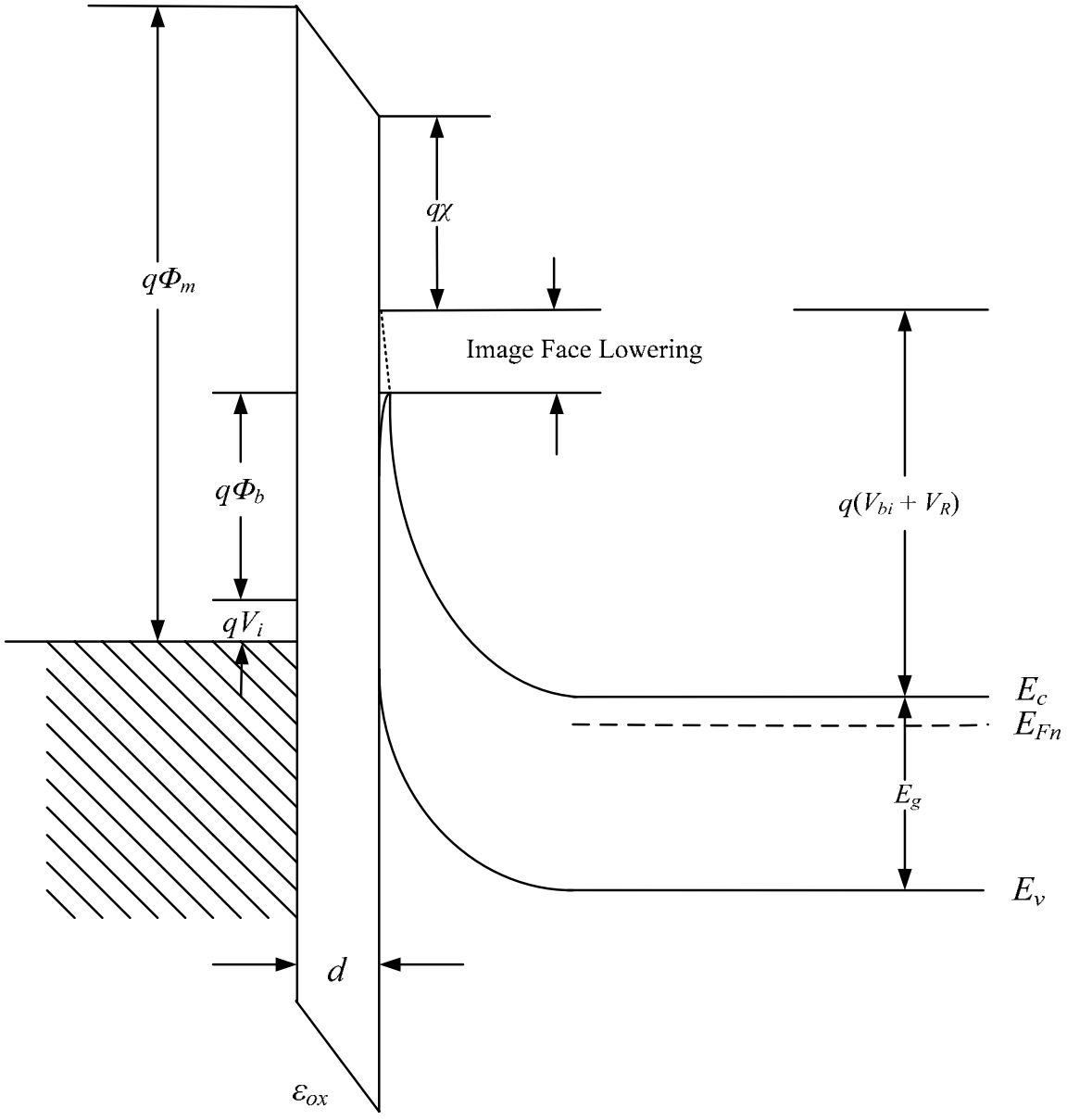


Figure (4.2): Energy band diagram of a reverse biased Schottky barrier with an interfacial layer.

from Schottky barrier quality and channel length and is given by Equation (2.2.9) [Ladbrooke-1991, Ahmed (a)-1995 and Ahmed (b)-1995]. Combining Equations (2.2.9) & (3.7.2) we obtain V_T for short channel MESFET under ideal Schottky barrier conditions as

$$V_T^{/} = \left[\frac{q N_d a^2}{2 \varepsilon_s} - \Phi_b \right] \times \left[1 + \frac{4a}{3L_G} \right] \qquad (4.5.1)$$

Consider *I-V* characteristics of a MESFET shown in Figure (4.3). The device under consideration has the following physical parameters:

N = 5 x 10^{17}cm^{-3};
a = 81 nm;
L_G = 0.23 μm
W = 100 μm
Φ_b = 0.60 V;
$V_T^{/}$ = -2.472 V

Figure (4.3-a) represents output characteristics and in these characteristics the device exhibits excellent pinch-off indicating good gate control on the I_{ds}. An experimental value of V_T = - 2.5 V, whereas the one calculated from Equations (4.5.1) is – 2.472 V. The observed and calculated values are with in 1% margin; hence one can claim that the device response is close to ideal which implies that Schottky barrier is almost clean and the device could be used as a reference device. A careful calculation by Using Equation (4.3.5) reveals that the interface has a nominal interfacial layer of $d \leq$ 5 ºA.

Figure (4.3-b) represents Schottky barrier response of the same device, i.e., A4- 74-11. The observed current flow is much higher and therefore both Fowler-Nordheim tunneling and Poole-Frenkel emission are inadequate to explain it

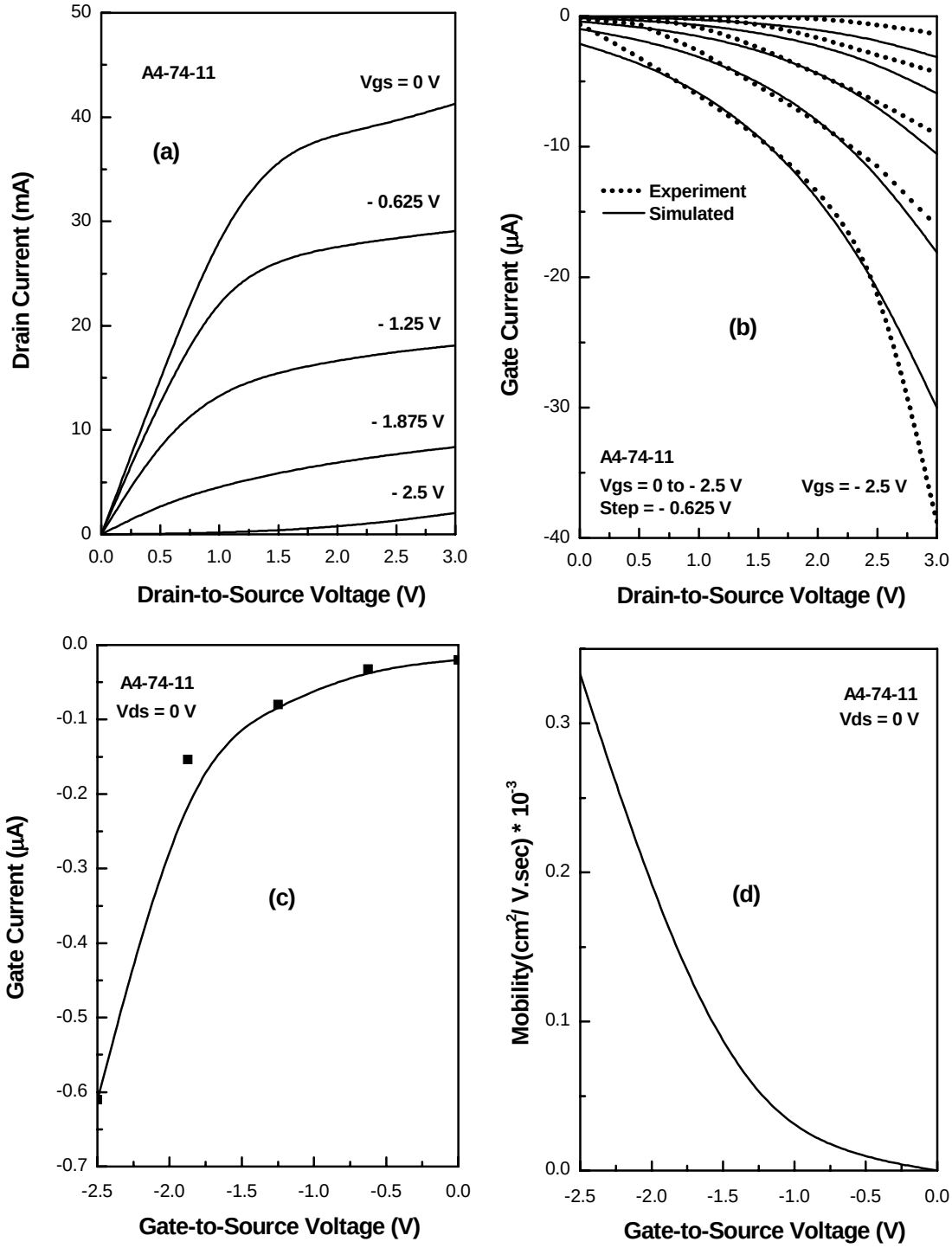


Figure (4.3): DC characteristics of a 0.23 x 100 μm^2 GaAs MESFET (a) output characteristics (b) gate leakage current as a function drain biasing (c) gate leakage current as a function gate biasing and (d) carrier mobility through interfacial layer.

[Fujimaru-1999, Chong-2005, Hill-1971, Hickmott-2005, Jeong-2005 and Jogi-2007]. The observed current is thus simulated by using Equations (4.4.2). The variation of Schottky barrier current as a function of V_{gs} at V_{ds} = 0 is shown in Figure (4.3-c). By observing the magnitude of the gate current, it is evident that the interfacial layer is nominal and the device depletion is control effectively by the Schottky barrier gate [Cetin-2005].

The variation in the value of μ_{ox} as function of V_{gs} is shown in Figure (4.3-d). The calculated value of μ_{ox} at V_{gs} = - 2.5 is 0.32 x 10^{-3} cm^2 / V.Sec, for the device under consideration. This represents an ease by which an electron can move into the gate electrode after passing a barrier collectively defined by the gate depletion and interfacial oxide layer [Moiz-2005, Moiz-2007 and Ahmed-2008]. As the magnitude of J is non-linear and follows an exponential behavior so does the μ_{ox}.

Figure (4.4) represents characteristics of a device having the same fabrication parameters as that of the device of Figure (4.3) but V_T = - 3 V, which is 20% greater than the device of Figure (4.3). Its Schottky barrier response is shown in Figure (4.4-b) & (4.4-c) as a function of V_{ds} and V_{gs} respectively. Comparing the Schottky characteristics of Figure (4.4) & (4.3), it is obvious that the device of Figure (4.4) has relatively higher leakage and thus offers poor gate control on its I_{ds}, and as result it requires more V_{gs} to pinch-off the channel. The value of μ_{ox} for this device is about six times higher than that the device of Figure (4.3). This shows that its Schottky barrier is lower and it is easier for carriers to scatter into the gate and constitute a relatively higher I_g.

It is obvious that a thicker oxide layer will offer relatively higher barrier to the flow of carriers, however the data suggest that a collective barrier defined by the

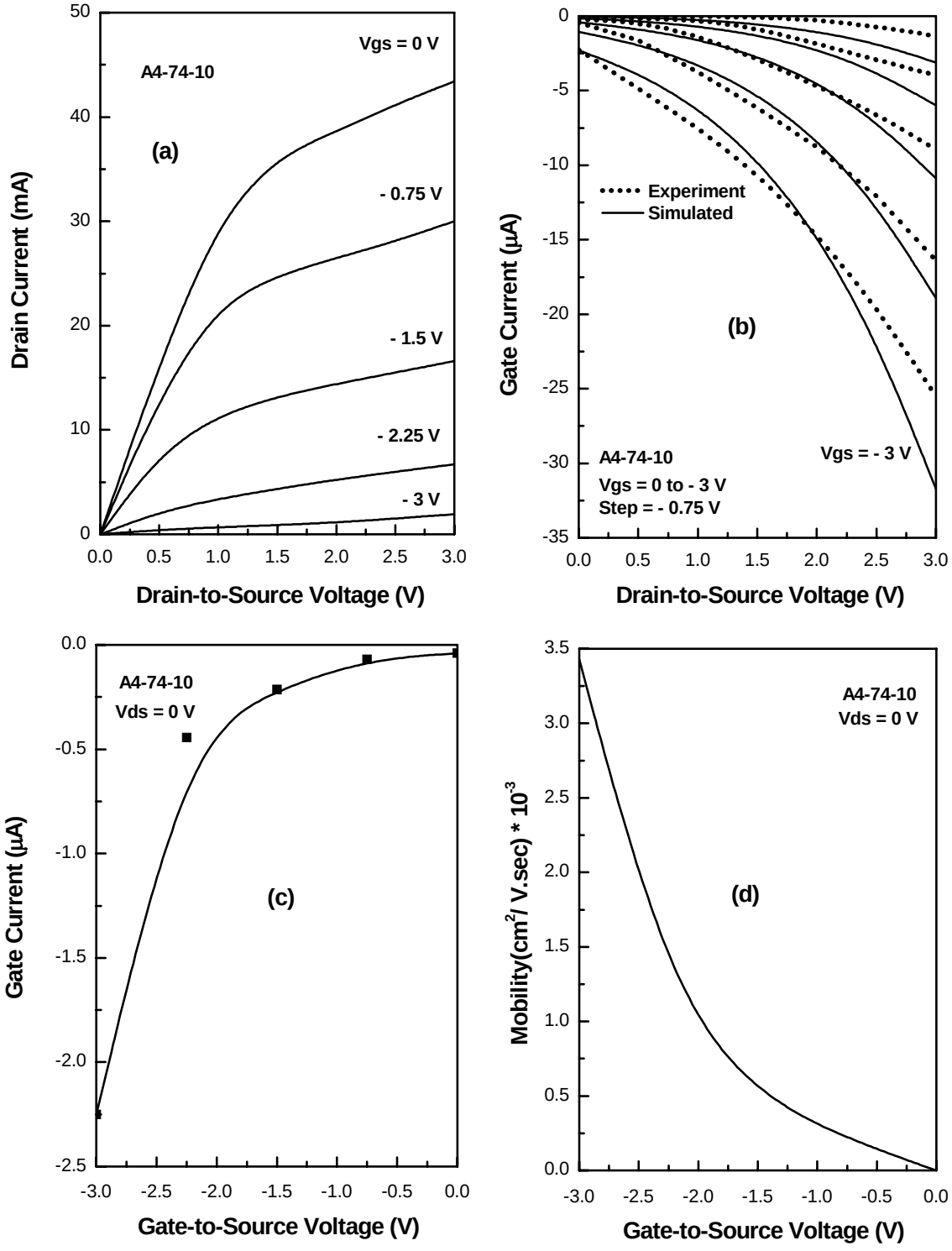


Figure (4.4): DC characteristics of a 0.23 x 100 μm^2 GaAs MESFET (a) output characteristics (b) gate leakage current as a function drain biasing (c) gate leakage current as a function gate biasing and (d) carrier mobility through interfacial layer.

depletion-oxide layer is relatively smaller. This indicates that a definite amount of V_{gs} is masked by the oxide layer which eventually reduces the gate depletion and increases I_g. It has been observed that the masking of V_{gs} due to a relatively thicker oxide layer gives more reduction in the barrier height than an additional increase offered by the oxide layer.

To confirm the proposed explanation of the observed response another device which offers a relatively higher V_T is shown in Figure (4.5). The value of I_g as shown in Figure (4.5-b) & (4.5-c) is exceptionally high as a result the μ_{ox} of this device as shown in Figure (4.5-d) is 50 times higher than the device of Figure (4.3). This once again demonstrated that the reduction in Schottky barrier height is significant for the devices having thicker oxide layer. Such devices will offer poor gate control and hence they have low g_m and high g_d values.

The oxide layer dependent V_T, g_m and g_d response of submicron GaAs MESFETs have been summarized in Figure (4.6). It has been observed that the device of Figure (4.3), which has ~ 5 ºA oxide layer thickness is close to theoretical behavior and one can claim that an oxide of ~ 5 ºA behaves as a transparent layer and causes negligible potential drop across it. The data shows that any value greater than 5 ºA will start creating negative effects on the device response.

An obvious way through which one can assess the presence of oxide layer at the Schottky barrier of the device is the shift in its V_T. This shift can be expressed as

$$V_T^{//} = V_T + \Delta V_T + \Delta V_{Td} \qquad (4.5.2)$$

where ΔV_{Td} is the shift in V_T due to the oxide layer. Examining Figure (4.6-a) it is obvious that the straight line passing through experimental data has the equations

$$V_T^{//} = 2.25d + 1.33 \qquad \text{for } d > 0 \qquad (4.5.3)$$

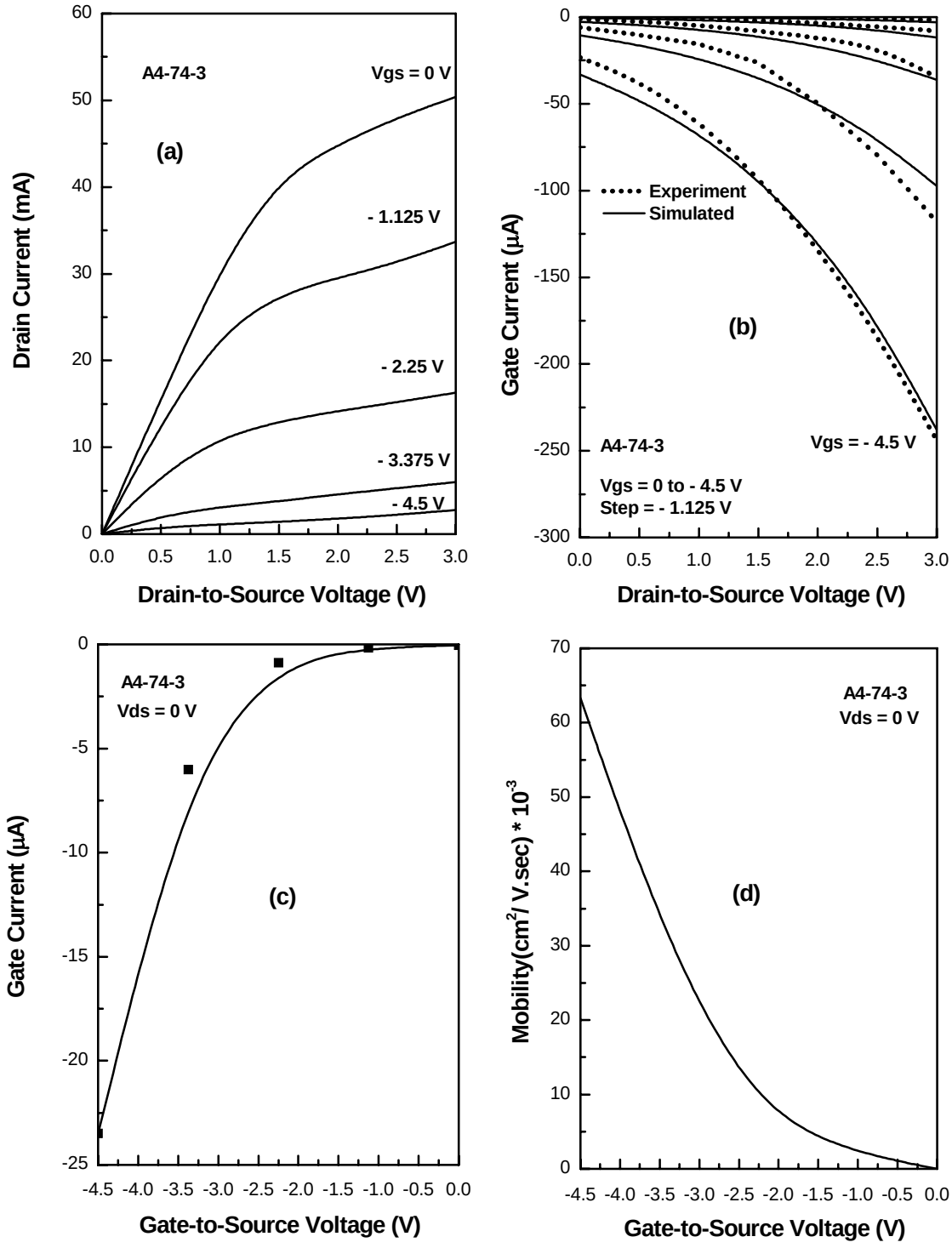


Figure (4.5): DC characteristics of a 0.23 x 100 μm^2 GaAs MESFET (a) output characteristics (b) gate leakage current as a function drain biasing (c) gate leakage current as a function gate biasing and (d) carrier mobility through interfacial layer.

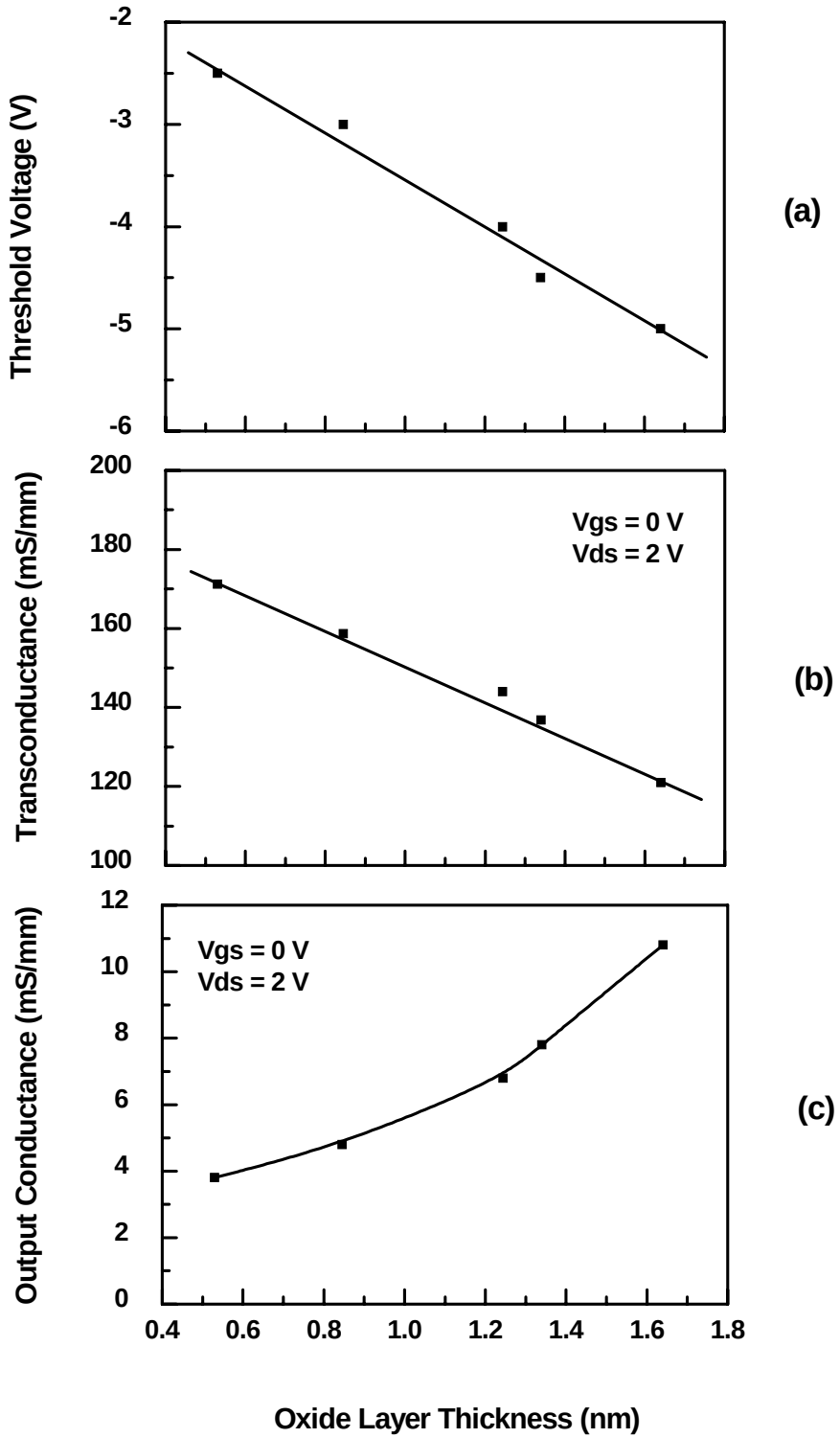


Figure (4.6): Variation of (a) threshold voltage, (b) transconductance and (c) output conductance as a function of oxide layer thickness at Schottky barrier of GaAs MESFETs.

where d is in nm. The value of ΔV_{Td} can then be calculated as

$$\Delta V_{Td} = V_T^{//} - V_T^{/} \tag{4.5.4}$$

The calculated ΔV_{Td} along with other parameters of five different GaAs MESFETs are given in Table-4.1.

4.5.1. Interfacial Layer Resistance

Electrically a barrier is nothing but an obstacle in the flow of carriers which could be represented by a resistor. A cross-sectional view of a biased MESFET is given in Figure (4.7-a) which shows a gate resistor, R_D, that represents resistance offer to electrons trying to move through the gate. In this diagram it has been assumed that the interface is clean and free from surface states. Whereas, in Figure (4.7-b) there is an oxide layer at the Schottky barrier and correspondingly this device has two gate resistors; one representing the oxide layer R_{ox}, and another $R_D^{/}$ associated with depletion. The resistor $R_D^{/}$ is different than R_D due to the modified depletion caused by the oxide layer. The channel height which is available to the flow of carriers is $a^{/}$ for the first case whereas it is $a^{//}$ for the second case. As the observed data show that I_g is higher for the case represented by Figure (4.7-b), thus one can write

$$R_D > R_{ox} + R_D^{/} \tag{4.6.1}$$

It is obvious that by increasing d, the value of R_{ox} also increases; in that case the above inequality will be valid only if $R_D^{/}$ decreases with a rate higher than the rate of increase of R_{ox}. This in return will increase I_g which has been observed in the devices having thicker oxide layer.

The changing behavior of such devices having variable oxide layer thickness has been summarized in Table-4.1. The data of the table shows that the devices

Table-4.1
Comparison of electrical parameters of GaAs MESFET's having variable interfacial layer thickness.

Device No.	I_{dss} (mA)	V_T (V) Exp	V_T (V) Eqn (4.5.1)	ΔV_{Td} (V)	g_m (mS) V_{ds} = 2 V	g_d (mS) V_{gs} = 0 V_{ds} > 2 V	Channel Thickness (*a*) (nm)	Oxide layer Thickness (*d*) (nm)	Mobility (cm^2 / V.sec) x 10^{-3} at Vgs = -2.5 V
A4-74-11	36.5	-2.5	-2.472	-0.028	171	146	81	0.53	0.33
A4-74-10	36.2	-3.0	-2.38	-0.62	158	122	80	0.84	2
A4-74-6	45.0	-4.0	-3.375	-0.625	144	204	90	1.24	9
A4-74-3	41.0	-4.8	-2.956	-1.844	136	208	86	1.34	11
A4-86-11	38.0	-5.0	-2.66	-2.33	100	222	83	1.64	200

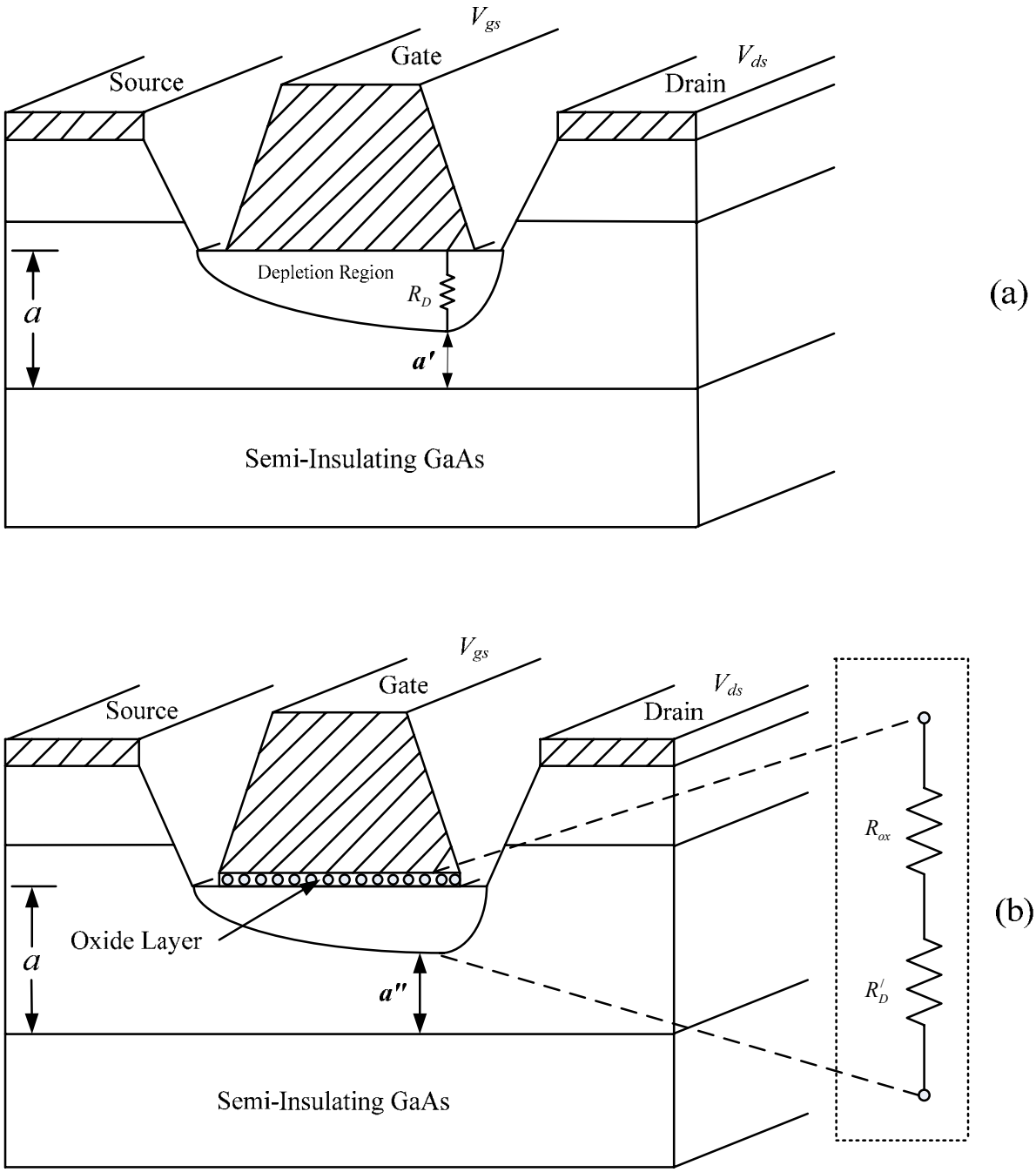


Figure (4.7): Variation in resistance and thickness of the depletion region (a) without oxide layer thickness and (b) with oxide layer thickness at Schottky barrier of GaAs MESFETs.

having oxide layer thickness < 5 ºA behaves closer to an ideal Schottky barrier device. And an oxide layer thickness > 5 ºA shall have detrimental effects on the device performance. It is therefore absolutely imperative to take necessary measures during fabrication to clean the interfacial layer before Schottky barrier metallization process.

4.6. Summary

This chapter discusses the effects of interfacial layer on the Schottky barrier height. It has been shown that the presence of interfacial layer causes soft reverse characteristics of a Schottky barrier diode with higher current, which cannot be explained fully by thermionic emission theory. The increased magnitude of Schottky current was associated with Schottky barrier lowering caused by the masking of the applied potential across the interfacial layer. This layer is of atomic nature which has finite thickness and it can hold a finite potential across it but behaves as a transparent medium for the flow of current. The quality of the barrier is then assessed by the magnitude of current flowing from it.

The Schottky barrier interfacial layer dependent performance of submicron GaAs MESFETs has been discussed by using their output and transfer characteristics. The mobility of carriers scattering from the Schottky barrier gate have been evaluated and it has been observed that the mobility increases significantly for the devices having thicker interfacial layer. The negative effects of this mobility on MESFET characteristics have been discussed and a plausible explanation has been given for degraded device performance. Based on the proposed explanation the definition of V_T has been redefined involving the concept of interfacial layer thickness. While evaluating the interfacial layer dependent characteristics, it has been shown that the

value of V_T and g_m decreases inversely with the d, while the value of g_d increases directly with it.

Chapter 5

A Comprehensive FET *I-V* Model

5.1. Introduction

GaAs MESFET's characteristics depend upon numerous parameters. Thus, a simple model, like Shockley equation, cannot describe its behavior under all conditions with reasonable accuracy [Memon-2007]. Improved versions of non-linear models have, therefore, been presented by different researchers to predict *I-V* characteristics of GaAs MESFETs [Curtice-1980, Kacprzak-1983, Statz-1987, McCamant-1990, Rodriguiz-1992, Ahmed (a)-1997, McNally-2001, Islam-2004 and Dobes-2004]. In Chapter-3, nine different models have been discussed and their accuracy for short channel MESFETs is evaluated. It is shown that Ahmed, McNally and Islam models are close enough and any one of those may be used for the simulation of short channel GaAs MESFET's characteristics. However, Ahmed model is the best observed model because of its better accuracy and efficient handling.

In submicron GaAs MESFETs, quite often, there is a finite density of interface states and the ideal device pinch-off as given by Equation (2.2.9) is usually not observed. [Ahmed-2000, Ahmed-1995 and Memon-2007]. The Schottky interfacial layer, which is a probable cause of V_T shift, is assumed to be of finite thickness that can hold potential across it and, on the other hand, it is transparent enough to allow the flow of electrons [Ahmed-1995, Wu-1982 and Rhoderick-1988]. Devices with interfacial layers exhibit relatively higher gate leakage and consequently the effect of gate potential to control the channel thickness is poor. The loss of finite amount of V_{gs} due to the interfacial layer has not been incorporated in those models presented in Chapter-3. They assumed an ideal Schottky interface of a GaAs MESFET and as a result these models are not accurate enough to simulate *I-V* characteristics of a device having finite Schottky barrier interfacial layer.

In this chapter, a comprehensive *I-V* model is proposed which is an extension to Ahmed model capable to simulate *I-V* characteristics of GaAs MESFETs irrespective of the Schottky barrier response. Furthermore, the applicability of the model was also checked for High Electron Mobility Transistor (HEMT) *I-V* characteristics where parasitic FET may also cause a non ideal response in the device characteristics.

5.2. New Model

The proposed model is conceived, primarily, by considering the fact that the presence of interfacial layer causes a non-ideality in Schottky barrier response of a GaAs MESFET. The presence of interfacial layer consumed a finite amount of V_{gs} and thus the magnitude of the potential which varies the channel height is different than the applied V_{gs}. Under such circumstances a simulation carried out by

considering V_{gs} as one of the variable cannot predict the device behavior accurately. Thus, one can write

$$V_{gs}\left[Gate-to-Source\ Region\right]=V_{gs}\left[Interfacial\right]+V_{gs}\left[Depletion\right] \quad (5.1.1)$$

The above expression indicates that a portion of applied voltage is consumed by the interfacial layer. And if the density of states at the interface of a Schottky junction is high then the contribution of V_{gs} [*Interfacial*] will also be high in equation (5.1.1) and thus cannot be ignored. A simulation based on mere V_{gs} value by ignoring V_{gs} [*Interfacial*] will generate a discrepancy between the observed and the predicted characteristics of a MESFET.

By examining models presented in Chapter-3, it is very obvious that these models are assuming an ideal Schottky barrier interface of a MESFET which is usually not true. To overcome this problem and keeping in view the exponential nature of density of states [Kilicoglu-2006, Campi-1999, Saha-2004, Mustafa-2005], following expression is proposed which modifies V_{gs} variable of Ahmed model as

$$V_{eff}=\frac{V_{gs}}{1+\eta\, e^{V_{gs}}} \quad (5.2.2)$$

This expression defines V_{eff} with η as a fitting variable that simulates quality of a Schottky barrier and gives component of V_{gs} that alter the gate depletion. For $\eta = 0$, the Schottky barrier is close to ideal and the effects of interface states are negligible. The expression of Ahmed model with this proposed modification can now be written as

$$I_{ds}=I_{dss}\left(1-\frac{V_{eff}}{V_T+\Delta V_T+\gamma V_{ds}}\right)^2\times\tanh(\alpha V_{ds})\,(1+\lambda V_{ds}) \quad (5.2.3)$$

This is a comprehensive model capable of simulating *I-V* characteristics of submicron GaAs FETs including those involving second order effects.

In Equation (5.2.3) there are four fitting parameters or empirical constants: (a) α - simulates the dependence of linear region on V_{ds}; (b) γ - simulates the dependence of threshold voltage on V_{ds}; (c) λ - simulates the dependence of $I_{ds(sat)}$ on V_{ds} and (d) η - simulates the quality of Schottky barrier interface. The effects of these variables on the dc characteristics of the device are discussed in Section-5.3

The values of g_m and g_d are derived by differentiating I_{ds}, given in Equation (5.2.3), with respect to V_{gs} and V_{ds} respectively

$$g_m = 2 I_{dss}\left[1-\frac{V_{eff}}{V_T+\Delta V_T+\gamma V_{ds}}\right]\times\left[\frac{V_{eff}}{V_{gs}}\left(1-\eta V_{eff}\, e^{V_{gs}}\right)\right]$$

$$\times\left[\frac{-1}{V_T+\Delta V_T+\gamma V_{ds}}\right]\times\left[\tanh(\alpha V_{ds})\,(1+\lambda V_{ds})\right] \qquad (5.2.4)$$

and

$$g_d = 2 I_{dss}\left[1-\frac{V_{eff}}{V_T+\Delta V_T+\gamma V_{ds}}\right]\times\left[\frac{\gamma V_{eff}}{(V_T+\Delta V_T+\gamma V_{ds})^2}\right]\times\tanh(\alpha V_{ds})\,(1+\lambda V_{ds})$$

$$+ I_{dss}\left[1-\frac{V_{eff}}{V_T+\Delta V_T+\gamma V_{ds}}\right]^2\times\left[1-\tanh^2(\alpha V_{ds})\right](1+\lambda V_{ds})$$

$$+\lambda I_{dss}\left[1-\frac{V_{eff}}{V_T+\Delta V_T+\gamma V_{ds}}\right]^2\times\tanh(\alpha V_{ds}) \qquad (5.2.5)$$

5.3. Effects of Fitting Parameters on GaAs MESFET's DC Characteristics

The effects of fitting parameters on I_{ds} is shown in Figure (5.1) for changing values of α, γ, λ, and η. Figure (5.1-a) shows the variation in I_{ds} as function of V_{gs} for

different values of α while keeping other variables constant. The figure is plotted by using Equation (5.2.3) and the plot represents that the magnitude of I_{ds} is very sensitive to the chosen values of α. Examination of the figure reveals that the effect of α reduces with its increasing magnitude as it is obvious from hyperbolic tangent function of Equation (5.2.3) in which α is used to define its argument. This indicates that for smaller values of α the voltage $V_{ds(sat)}$ will be relatively higher compared to its higher values. Thus, the linear region prior to the saturation and the knee voltages of *I-V* characteristics of a GaAs MESFET can be controlled by appropriately choosing the value of α in Equation (5.2.3).

Figure (5.1-b) represents the variation in I_{ds} for changing values of γ. The figure shows that each curve is starting from the same point on y-axis indicating the same value of I_{ds}, but follows a different profile for its termination, thus, defining an independent value of V_T for each case. The same value of I_{ds} in Figure (5.1-b) specifies an identical *a* in Equation (5.2.3) for all the plots, however, a different V_T for each case demonstrates that the variable γ can be used to simulate the shift in V_T. This shift is usually observed in *I-V* characteristics of a short channel device commonly called short channel effects.

The effect of λ on the magnitude of I_{ds} is shown in Figure (5.1-c). The plot shows that for positive values of λ the drain current increases whereas, for negative values the magnitude of I_{ds} decreases. Thus, enabling Equation (5.2.3) to simulate both positive and negative output conductance of the device. It is also observed that its effect prominent at $V_{gs} = 0$, but at higher negative values of $V_{gs,}$ there is relatively a small change in I_{ds} magnitude. This property can, therefore, be involved to simulate non-zero output conductance of a GaAs FET.

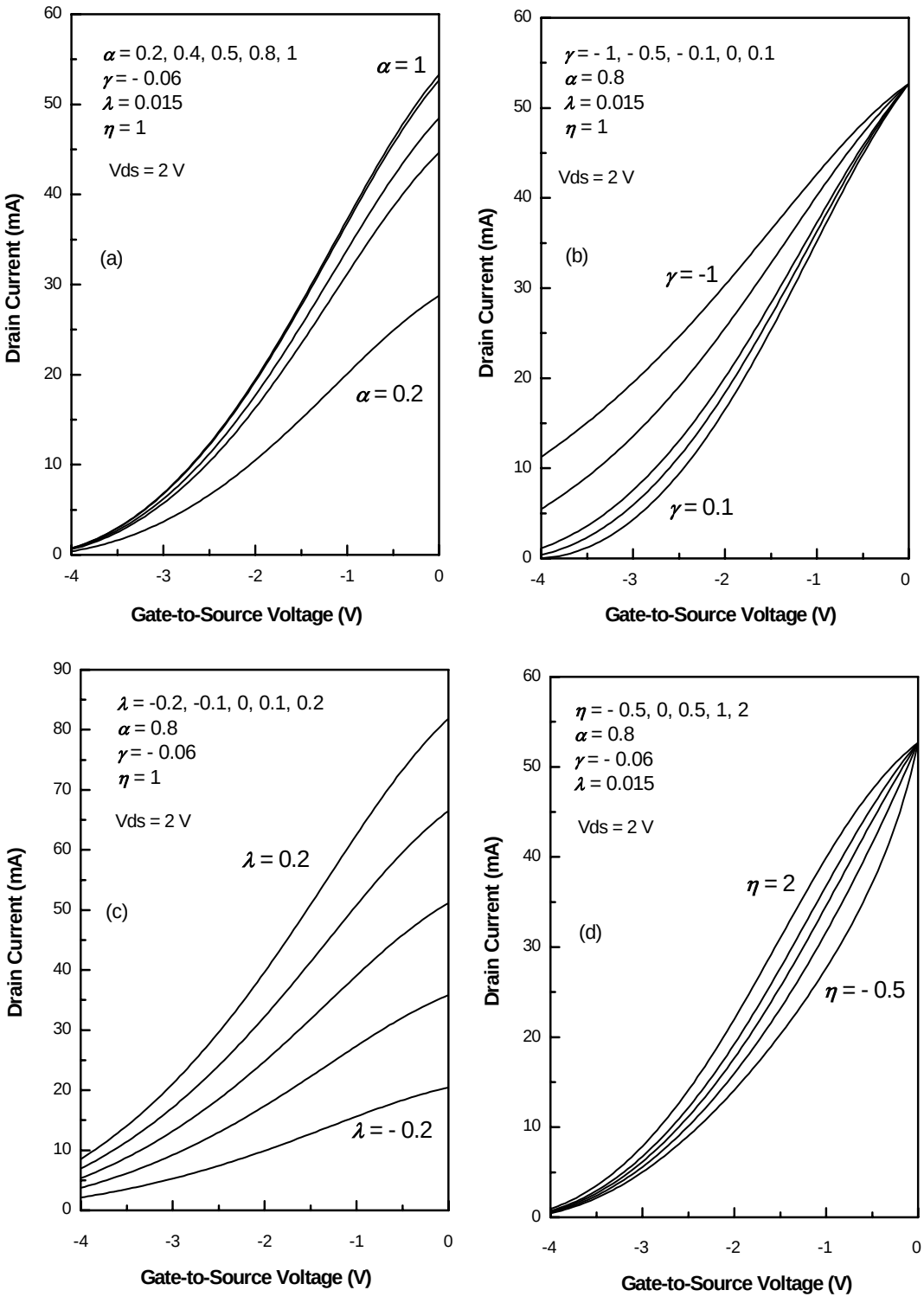


Figure (5.1): Effects of fitting variables: (a) α (b) γ (c) λ (d) η on drain current of a submicron GaAs MESFET

The effect of η on I_{ds} is shown in Figure (5.1-d). The figure shows that there is no change in I_{ds} with changing η at $V_{gs} = 0$ and also at $V_{gs} = V_T$. However, I_{ds} profile changes for $0 < V_{gs} < V_T$. This is a unique control provided by Equation (5.2.3) to simulate non-ideal Schottky gate response of a GaAs FET which is usually observed due to high density of interface states at Schottky junction of the device. By using Equations (5.2.4) & (5.2.5), the variation of $g_m(V_{gs})$ and $g_d(V_{ds})$ with changing values of fitting variables are shown in Figures (5.2) & (5.3) respectively.

5.4. Simulated MESFET's DC Characteristics

To demonstrate the validity of the developed model and to compare its performance with the best model reported in the literature [Ahmed (a)-1997] a submicron GaAs MESFET having following device parameters was selected:

$N = 5 \times 10^{17} cm^{-3}$;
$a = 90$ nm;
$L_g = 0.23\ \mu$m
$W = 100\ \mu$m
$\Phi_b = 0.6$ V;
$V_T = -2.49$ V
$\Delta V_T = -1.32$ V;

Figure (5.4) shows observed and simulated $I_{ds}(V_{gs},V_{ds})$, $g_m(V_{gs})$ and $g_d(V_{ds})$ characteristics of the device by using Ahmed model. The figure clearly shows a significant discrepancy between observed and simulated data, especially at lower V_{gs} values while its performance improves with increasing magnitude of V_{gs}. The characteristics of the same device were then simulated with the proposed model and the result is shown in Figure (5.5). The figure clearly illustrates that simulated

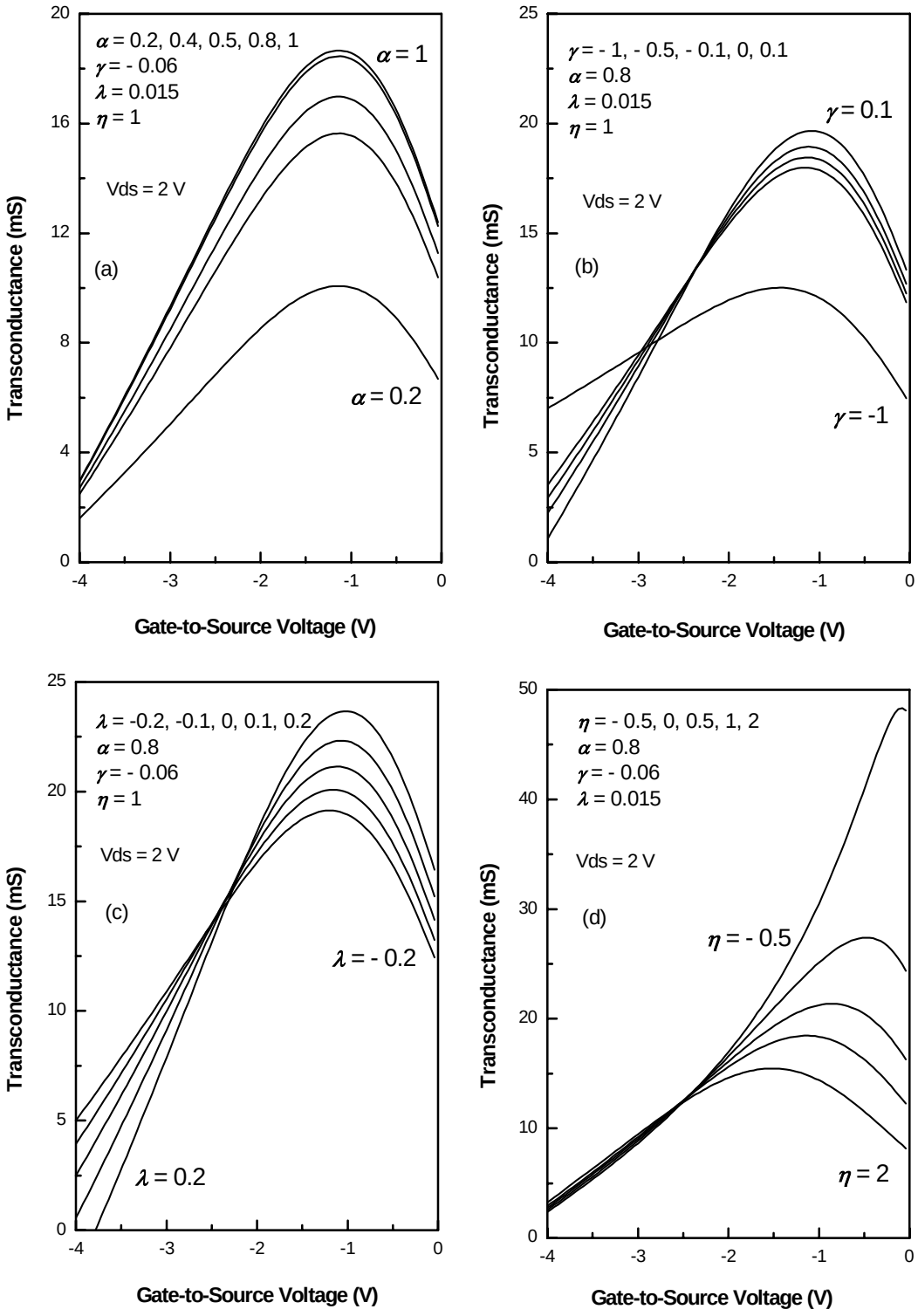


Figure (5.2): Effects of fitting variables: (a) α (b) γ (c) λ (d) η on transconductance of a submicron GaAs MESFET.

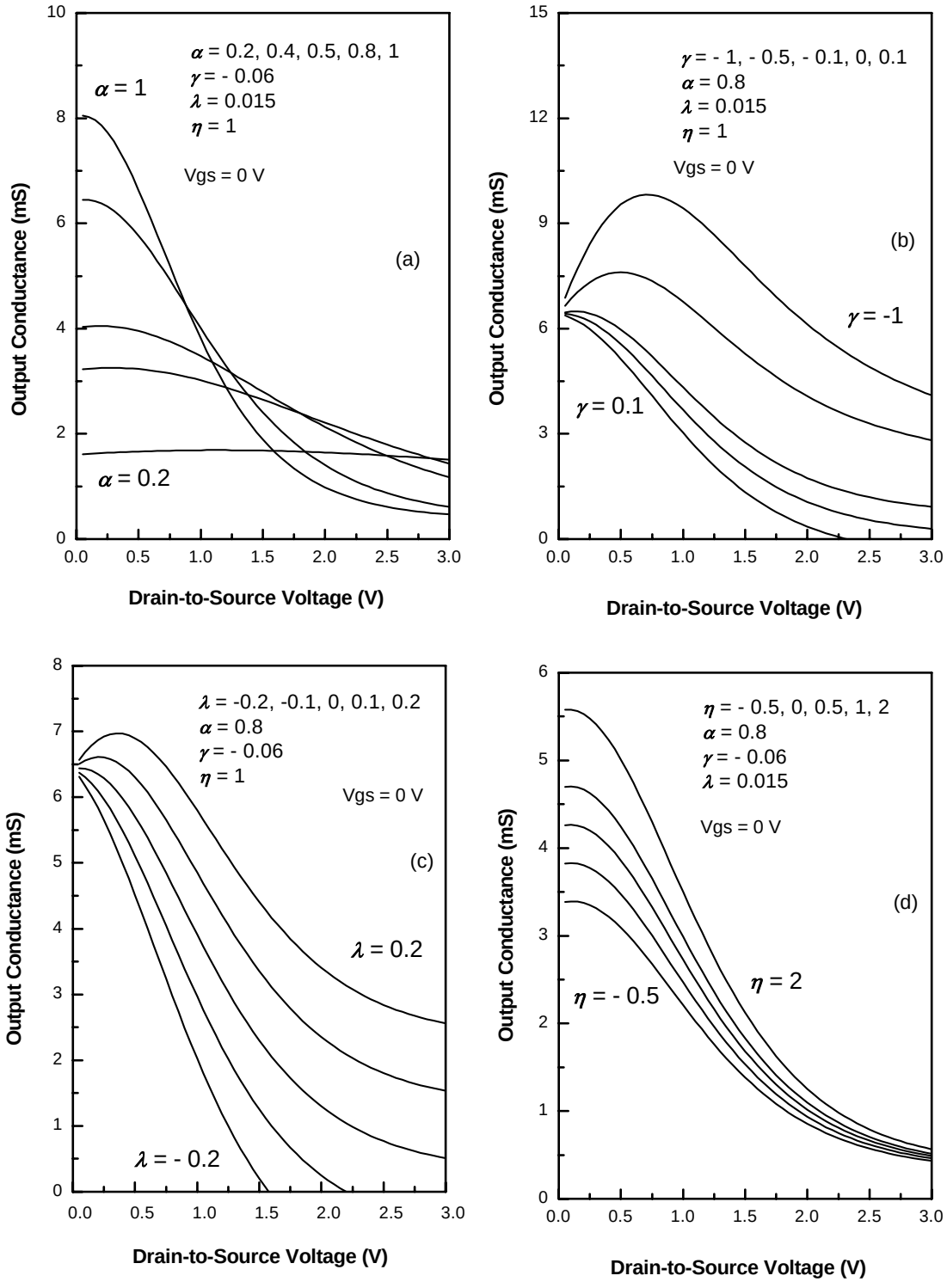


Figure (5.3): Effects of fitting variables: (a) α (b) γ (c) λ (d) η on output conductance of a submicron GaAs MESFET.

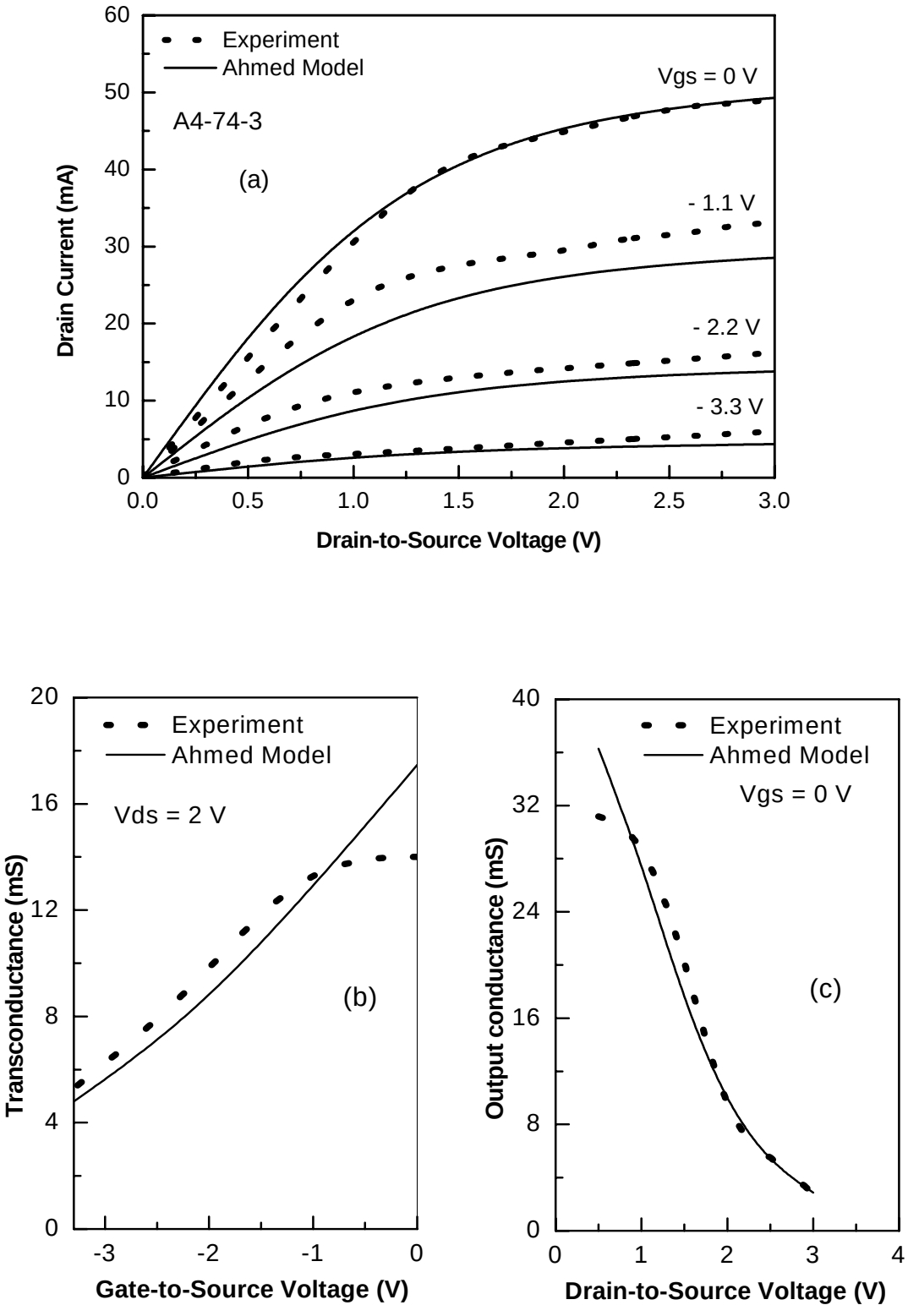


Figure (5.4): Observed and simulated characteristics of a 0.23 x 100 μm^2 GaAs MESFET by using Ahmed model (a) output *I-V* characteristics, (b) transconductance and (c) output conductance.

characteristics match reasonably well with observed data, especially in the saturation region of operation.

Another device similar to that of Figure (5.4) but with higher pinch-off voltages is also simulated and the result is shown in Figure (5.6). It is worth mentioning that the observed $V_T + \Delta V_T$ = -4.0 V, as seen from Figure (5.6.a), whereas the calculated one is -3.81 V. This discrepancy may be attributed to the consumption of Vgs potential by the interfacial layer at Schottky junction of the device which is not catered for in Ahmed model. Figure (5.7) shows the simulation carried out by using the new model and all three plots of the figure show a reasonably good match between observed and simulated characteristics. Thus, demonstrating the ability of the new model to simulate *I-V* characteristics of short channel MESFETs under varying Schottky barrier conditions.

RMS error values as a function of Vgs for devices of A4-74-3 & A4-74-6 are shown in Table-5.1 and Table-5.2 respectively. The data of both the tables show that the proposed model offers significant improvement especially at low V_{gs} potential compared to the best available GaAs MESFET model for the devices having different Schottky barrier qualities.

5.5. Simulated HEMT's DC Characteristics

A cross-sectional view of modulation doped GaAs field effect transistor also known as HEMT is shown in Figure (5.8). The Schottky gate has been placed in gate recess is also shown in figure GaAs donor layer which provides electrons to the channel has been fabricated such that it should be fully depleted with Schottky junction. However, due to the presence of interface states a finite portion of Φ_b is

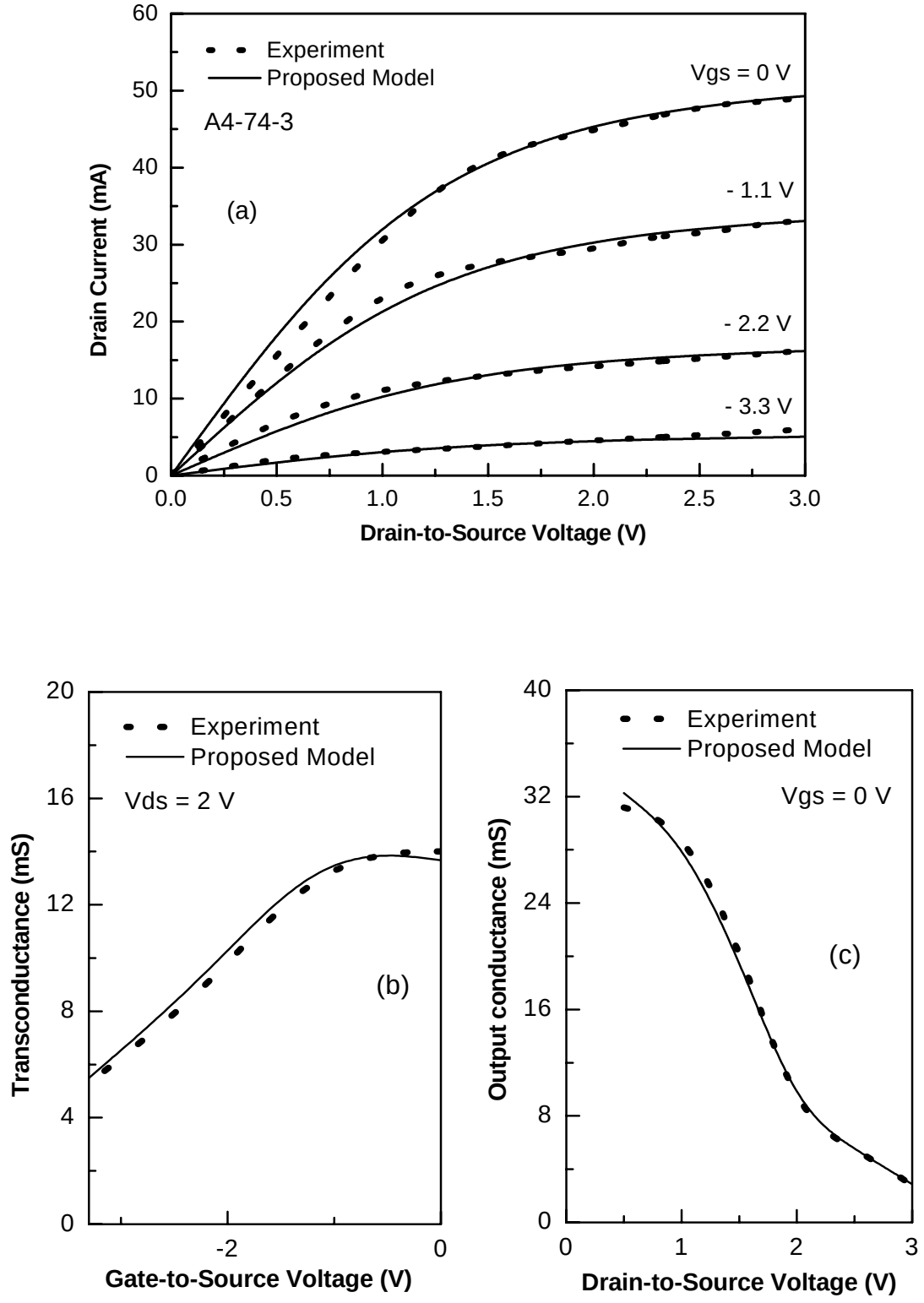


Figure (5.5): Observed and simulated characteristics of a 0.23 x 100 μm^2 GaAs MESFET by using proposed model (a) output *I-V* characteristics, (b) transconductance and (c) output conductance.

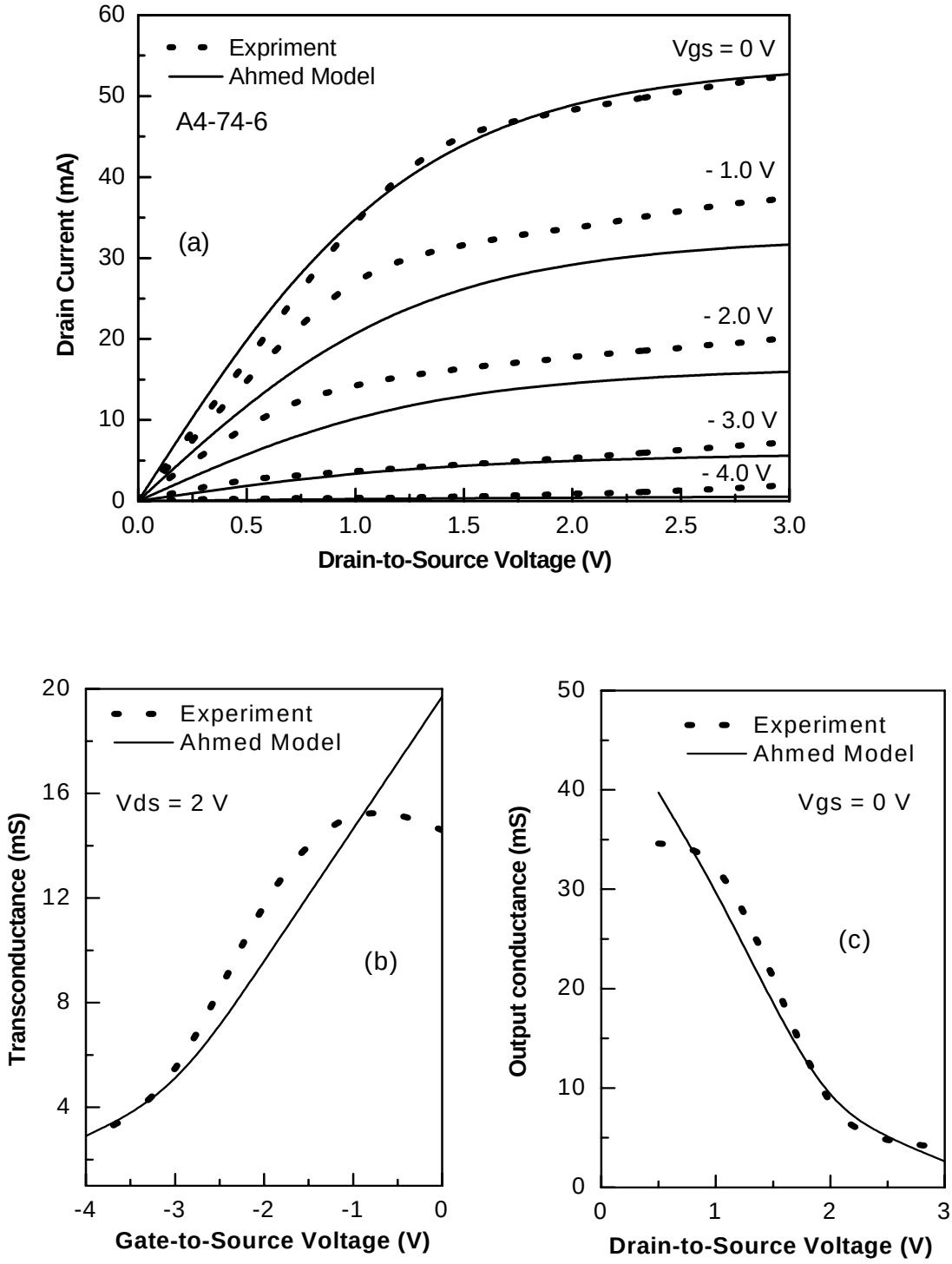


Figure (5.6): Observed and simulated characteristics of a 0.23 x 100 μm^2 GaAs MESFET by using Ahmed model (a) output *I-V* characteristics, (b) transconductance and (c) output conductance.

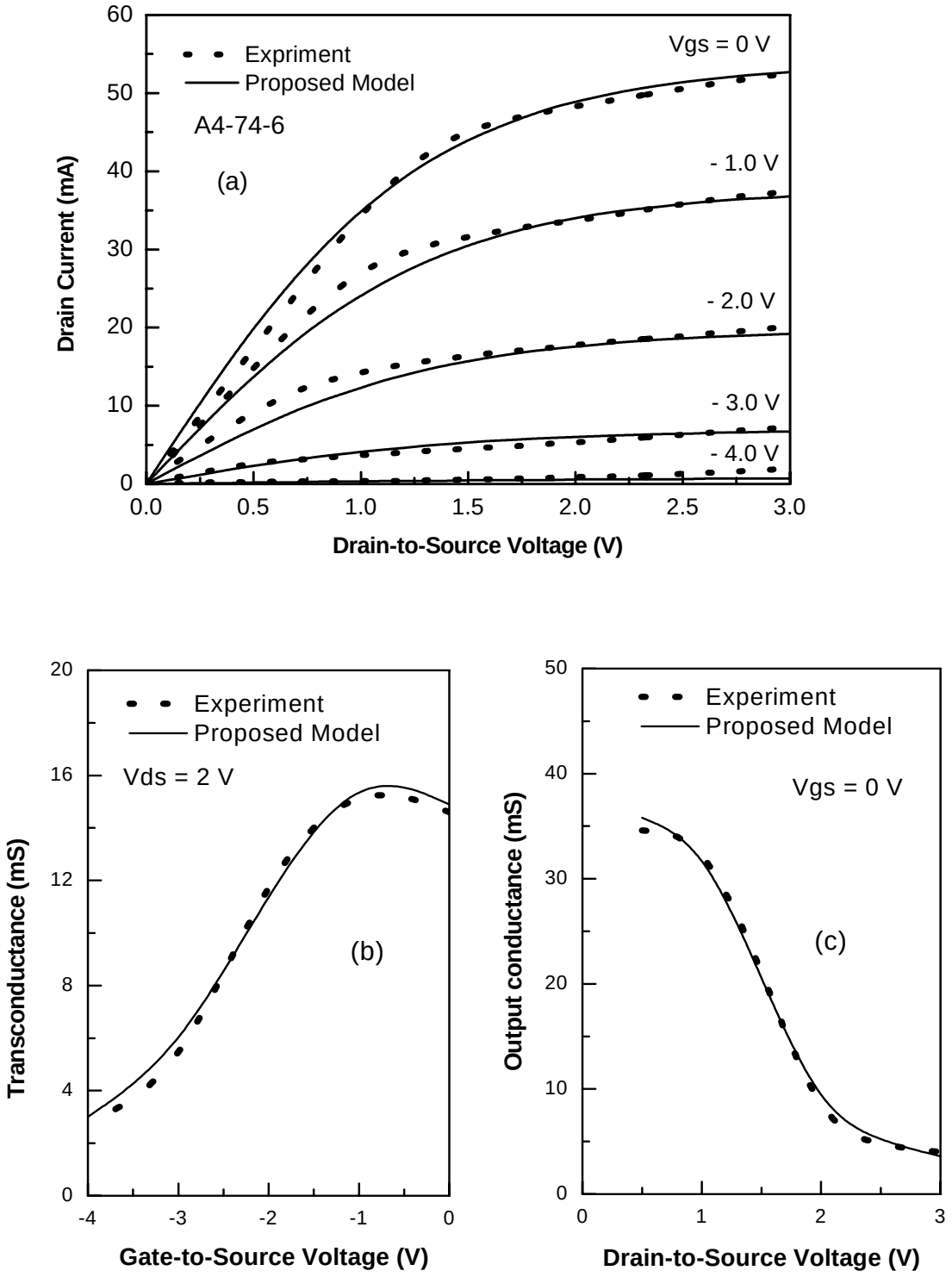


Figure (5.7): Observed and simulated characteristics of a 0.23 x 100 μm^2 GaAs MESFET by using proposed model (a) output *I-V* characteristics, (b) transconductance and (c) output conductance.

Table - 5.1
Comparison of RMS errors of proposed MESFET model with Ahmed model for device A4-74-3

Model	RMS error at different values of V_{gs}				Average Error
	V_{gs} =0.0	**V_{gs} = -1.1V**	**V_{gs} = -2.2V**	**V_{gs} = -3.3V**	
Ahmed	0.91	3.56	1.68	0.68	1.71
Proposed	0.91	1.30	0.71	0.35	0.82

Table - 5.2
Comparison of RMS errors of proposed MESFET model with Ahmed model for device A4-74-6

Model	RMS error at different V_{gs} values					Average Error
	V_{gs} = 0V	**V_{gs} = -1V**	**V_{gs} = -2V**	**V_{gs} = -3V**	**V_{gs} = -4V**	
Ahmed	1.22	5.15	3.65	0.86	0.71	2.32
Proposed	1.13	1.29	1.19	0.46	0.54	0.92

consumed by the interfacial layer resulting in an un-depleted portion of the donor layer. This generates second order effects in the device *I-V* characteristics known as parasitic FET effects. Under such conditions whenever the device is biased, the initial values of V_{gs} will be first used to deplete the parasitic FET after that the gate depletion will touch the channel to control two dimensional electron gas (2DEG).

Since the proposed model offers a versatile control on the Schottky barrier gate, hence it could be possible to simulate *I-V* characteristics of a HEMT having parasitic FET by using Equation (5.2.3). An accurate DC simulation will then provide a ground to predict AC equivalent circuit of the device. Figures (5.9) & (5.11) shows simulated and observed *I-V* characteristics of 0.7 x 200 μm^2 and 0.12 x 100 μm^2 HEMTs respectively by using Ahmed model. Whereas the simulation of the same devices by using the new model is presented in Figures (5.10) & (5.12) respectively. The RMS error values data against V_{gs} is presented in Tables-5.3 & 5.4 respectively. The data shows and average RMS error improvement up to 50% for the device of Figures (5.9) & (5.11) whereas an average RMS error improvement up to 35% for the device of Figures (5.10) & (5.12). The data clearly shows that the simulation carried out by using Ahmed model is not within acceptable range for HEMTs devices having parasitic FET effects, whereas the accuracy of the new model is reasonably well and provides a significant improvement over the existing models.

5.6. Summary

A comprehensive new model is developed to simulate *I-V* characteristics of short channel GaAa FETs. The validity of the model is established by simulating I_{ds},

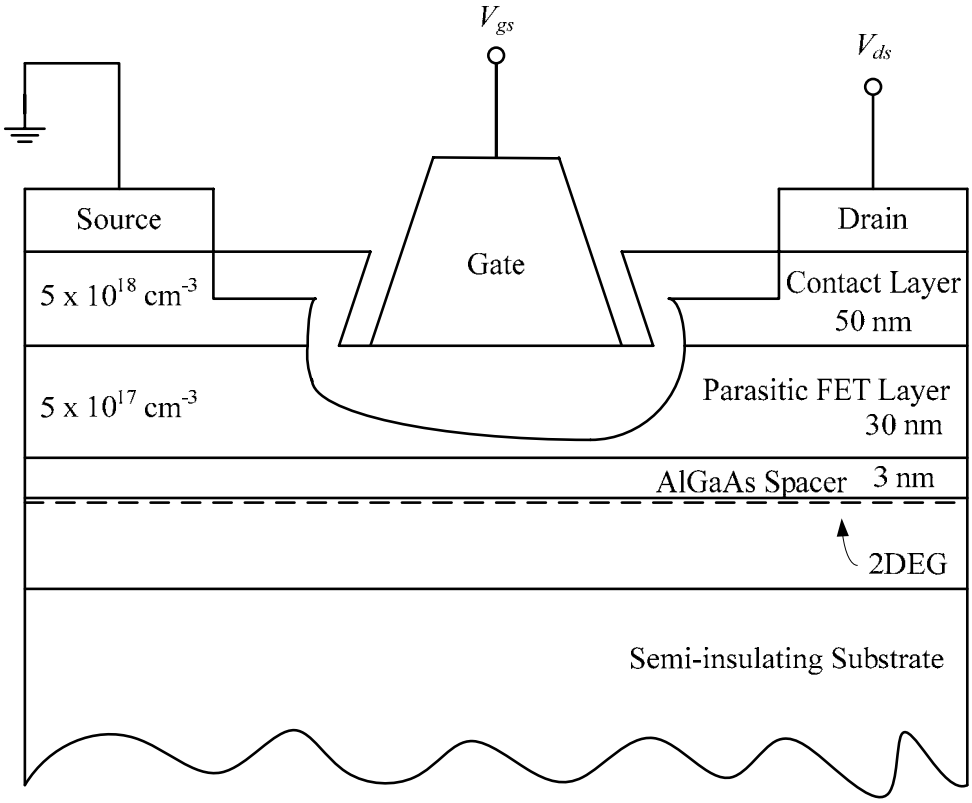


Figure (5.8): A Cross-sectional view of a GaAs HEMT illustrating the presence of parasitic FET.

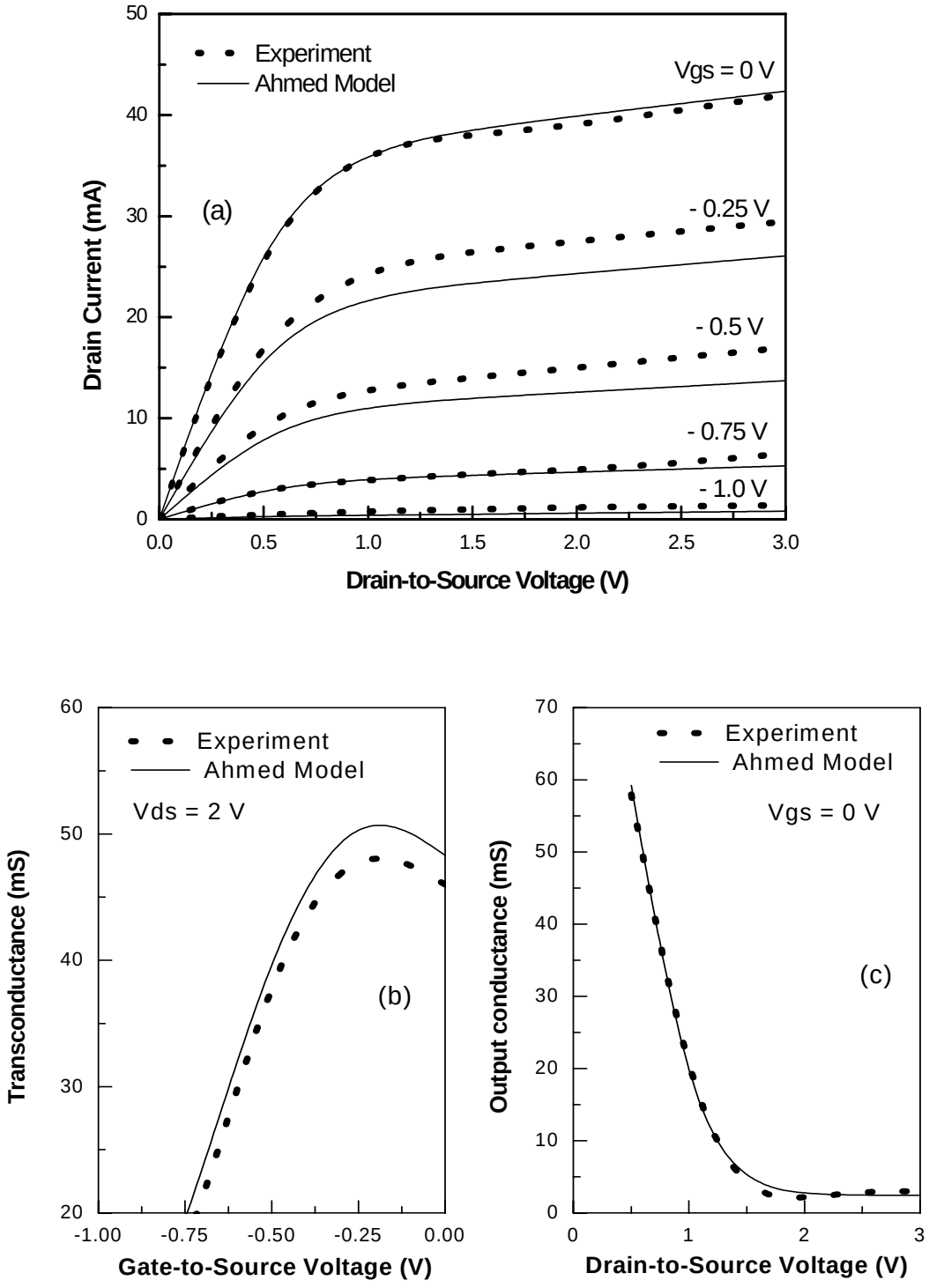


Figure (5.9): Observed and simulated characteristics of a 0.7 x 200 μm^2 HEMT by using Ahmed model (a) output *I-V* characteristics, (b) transconductance and (c) output conductance.

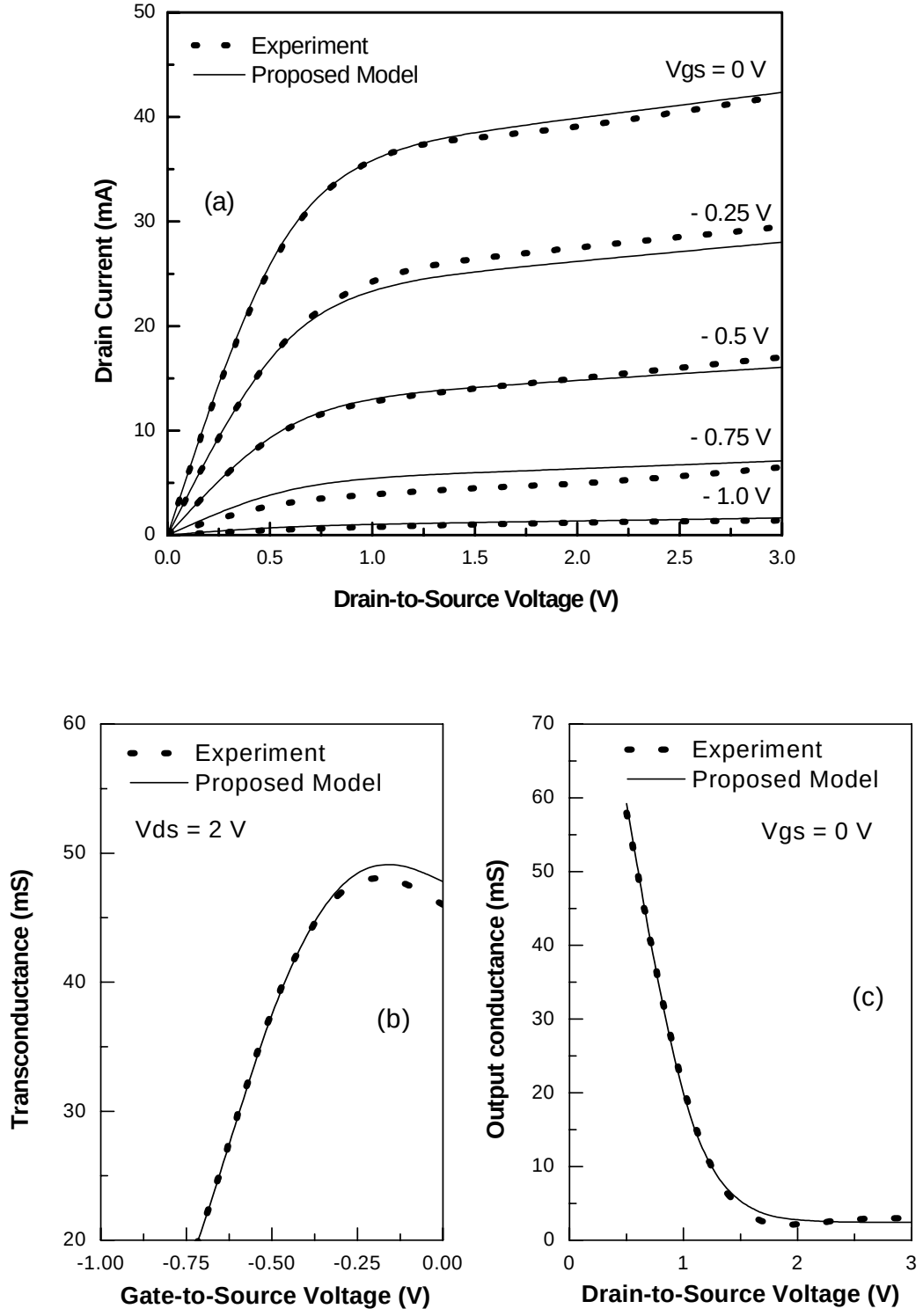


Figure (5.10): Observed and simulated characteristics of a 0.7 x 200 μm^2 HEMT by using proposed model (a) output *I-V* characteristics, (b) transconductance and (c) output conductance.

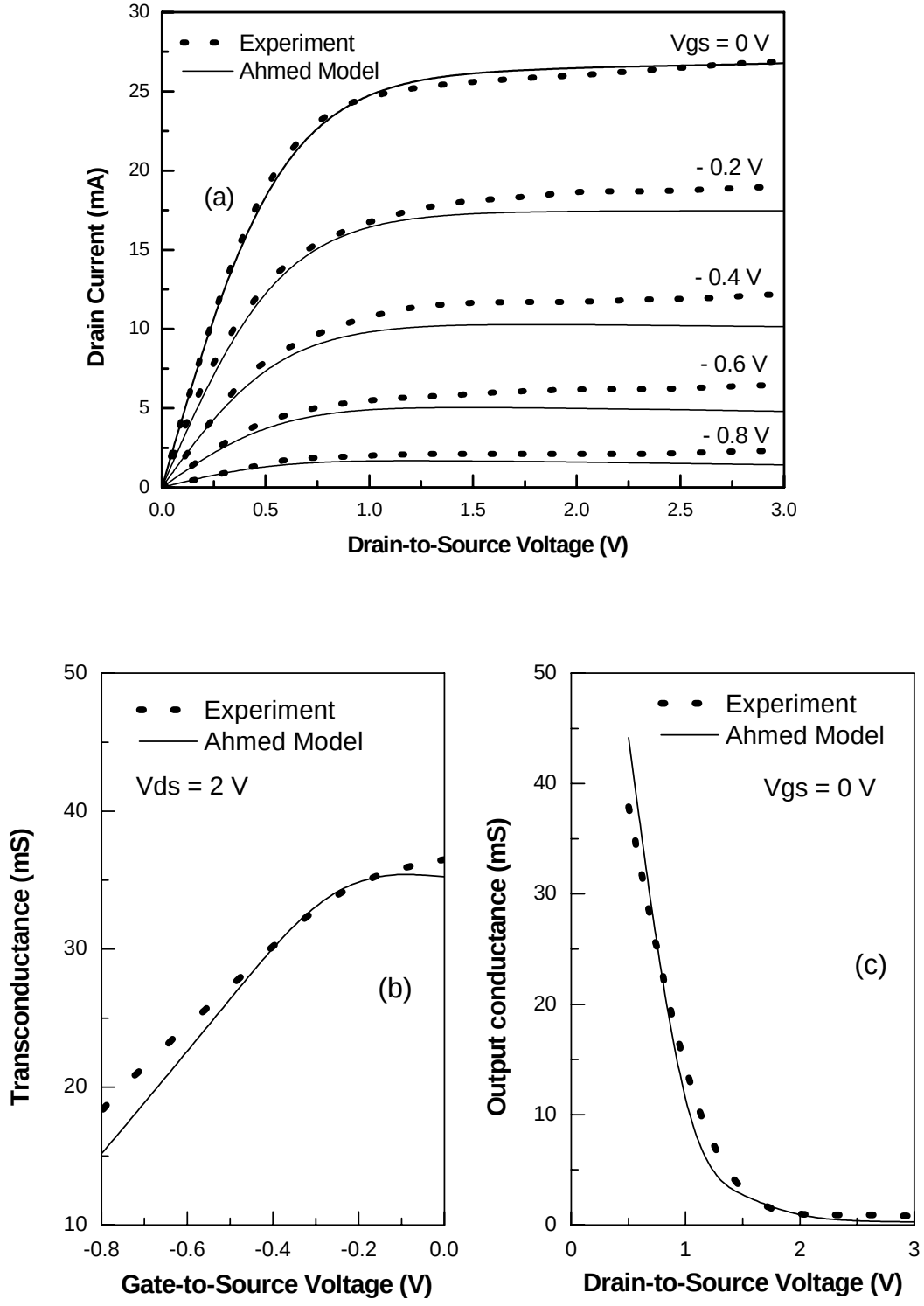


Figure (5.11): Observed and simulated characteristics of a 0.12 x 100 μm^2 GaAs HEMT by using Ahmed model (a) output *I-V* characteristics, (b) transconductance and (c) output conductance.

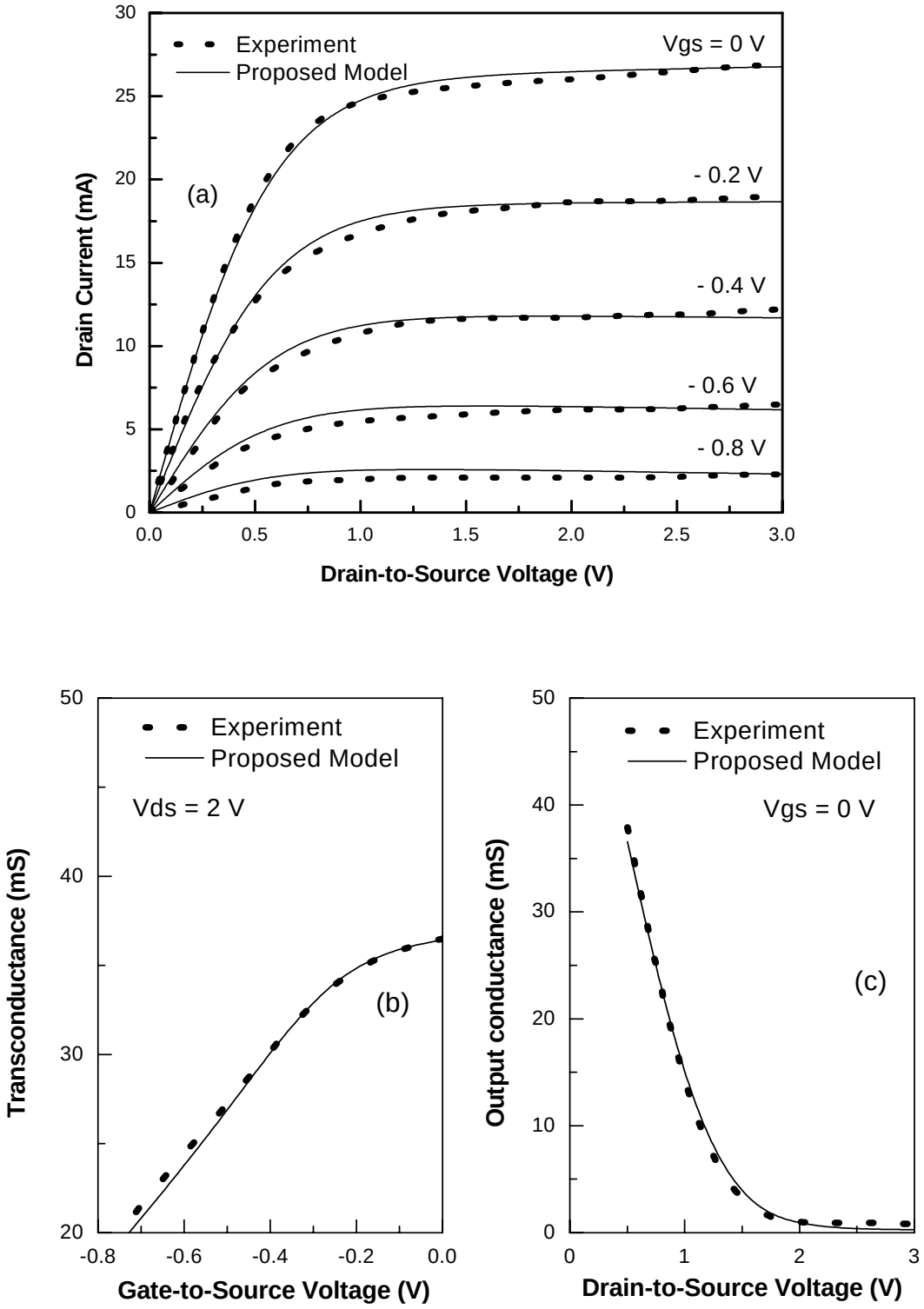


Figure (5.12): Observed and simulated characteristics of a 0.12 x 100 μm^2 GaAs HEMT by using proposed model (a) output *I-V* characteristics, (b) transconductance and (c) output conductance.

Table - 5.3
Comparison of RMS errors of Ahmed and proposed model for 0.7 µm HEMT

Model	RMS error at different V_{gs} values					Average Error
	V_{gs} = 0V	**-0.25V**	**-0.5V**	**-0.75V**	**V_{gs} = - 1V**	
Ahmed	0.93	1.5	1.68	1.85	2.21	1.63
Proposed	0.6	0.9	0.91	0.88	0.84	0.82

Table - 5.4
Comparison of RMS errors of Ahmed and proposed model for 0.12 µm GaAs HEMT

Model	RMS error at different V_{gs} values					Average Error
	V_{gs} = 0V	**-0.2V**	**-0.4V**	**-0.6V**	**- 0.8V**	
Ahmed	0.48	0.74	0.87	1.06	1.43	0.91
Proposed	0.44	0.49	0.29	0.16	0.31	0.33

g_m and g_d characteristics of different devices. The performance of the model is compared with the best available model, by calculating RMS error values. It has been demonstrated that the proposed model is a comprehensive one capable of simulating DC characteristics of GaAs MESFETs including those having significant non-ideal Schottky barrier response. The model has also been applied successfully on *I-V* characteristics of GaAs HEMTs with non-ideality caused by the parasitic FET. It has been shown that proposed model could be a useful tool for device simulators involving short channel FETs.

Chapter 6

Extraction of AC Parameters

6.1. Introduction

A properly designed short channel MESFET can operate comfortably at 100 GHz, whereas a HEMT, because of its superior g_m values, can function at much higher frequencies than MESFET [Golio-1991 and Das-1987]. To assess AC parameters of MESFETs and HEMTs at such a high frequency is an exceptionally difficult task. Conventional AC probers offer much lower frequency range than the maximum expected device response. Hence, the AC parameters of the device under test are usually predicted by extrapolation techniques [Enoki-1990 and Golio-1989].

It is an established fact that the evaluation of FET DC characteristics is a straightforward process and can be performed readily for both packed and unpacked devices [Ahmed-2003, Iqbal-2005]. On the other hand, an AC prober requires a very precise calibration for accurate AC parameters extraction. Thus, the process by its very nature is cumbersome and can affect an industrial throughput [Hwnag-1989 and

Debie-1995]. In 2003, a technique for assessing MESFET's AC parameters by employing its DC characteristics had been proposed by Ahmed [Ahmed -2003]. The validity of the technique was demonstrated by employing a 0.5 x 80 μm^2 MESFET characteristics. The proposed technique is valid for the devices which offer a reasonably good Schottky response, whereas it fails to simulate those devices which exhibit non-ideal Schottky barrier response.

DC characteristics based AC parameter evaluation process employs a nonlinear DC model which simulates the output and the transfer characteristics of the device by employing an optimization algorithm. Once a good fit is attained, the model is then extended to predict AC response of the device. The developed technique thus reduces the discrepancy between observed and simulated data which may arise due to non-ideal Schottky barrier response and short channel effects.

This chapter provides an extension to Ahmed's work, in which AC parameters of GaAs MESFETs have been assessed even for those devices which offer non-ideal Schottky barrier response. Furthermore, the technique is also extended for assessing AC parameters of short channel HEMTs. The proposed technique is a comprehensive one and capable to simulate MESFET's and HEMT's intrinsic AC parameter with reasonable accuracy for changing Schottky barrier conditions.

6.2. MESFET's and HEMT's AC Parameters

MESFETs and HEMTs are, primarily, used in front-end amplifiers because of their superior noise and high frequency properties. To establish high frequency capabilities of these devices AC equivalent circuit parameters are used which are controlled by the device fabrication and designing processes and assessed from its electrical response.

Figure (6.1) shows, simulated and observed *I-V* characteristics of a 0.3 x 280 μm^2 GaAs MESFET. The simulation is carried out by using Equation (5.2.3) where the chosen values of empirical constants are: $\alpha = 3$; $\lambda = 0.14$; $\gamma = -0.06$ and $\eta = 0.15$. The simulation data revealed that about 87% of applied V_{gs} is used to change the depletion while the remaining V_{gs} voltages are consumed by the parasitic resistances and surface states. A reasonably good fit is attained in Figure (6.1) which suggests that Equation (5.2.3) can be employed to assess electrical parameters of the device. The AC parameters, which are to be assumed, are discussed in the following sections.

6.2.1. Gate-to-Source Capacitance, C_{gs}

This is one of the major components which determines AC response of the device, and is commonly known as Miller's capacitor [Ahmed-2003]. The magnitude of C_{gs} capacitor can be assessed as [Ladbrooke-1991, Fukui-1979 and Fukui-1980]

$$C_{gs} \approx \frac{q\, N_d\, v_s\, Z^2\, \varepsilon_s\, L_G}{a\, q\, N\, v_s\, Z - I_{ds}} \tag{6.2.1}$$

Where

$$I_{ds} = I_{dss}\left(1 - \frac{V_{gs}}{(1+\eta\, e^{V_{gs}})\,(V_T + \Delta V_T + \gamma V_{ds})}\right)^2 \times \tanh(\alpha V_{ds})\,(1+\lambda V_{ds}) \tag{6.2.2}$$

Equation (6.2.1) represents variation in C_{gs} as a function of V_{gs} and V_{ds}, where η is used to accommodate interface states.

Figure (6.2) represents change in the magnitude of C_{gs} at various values of η. Examination of the figure revealed that by increasing the value of η the magnitude of C_{gs} also increases. High value of η means lesser component of applied V_{gs} is

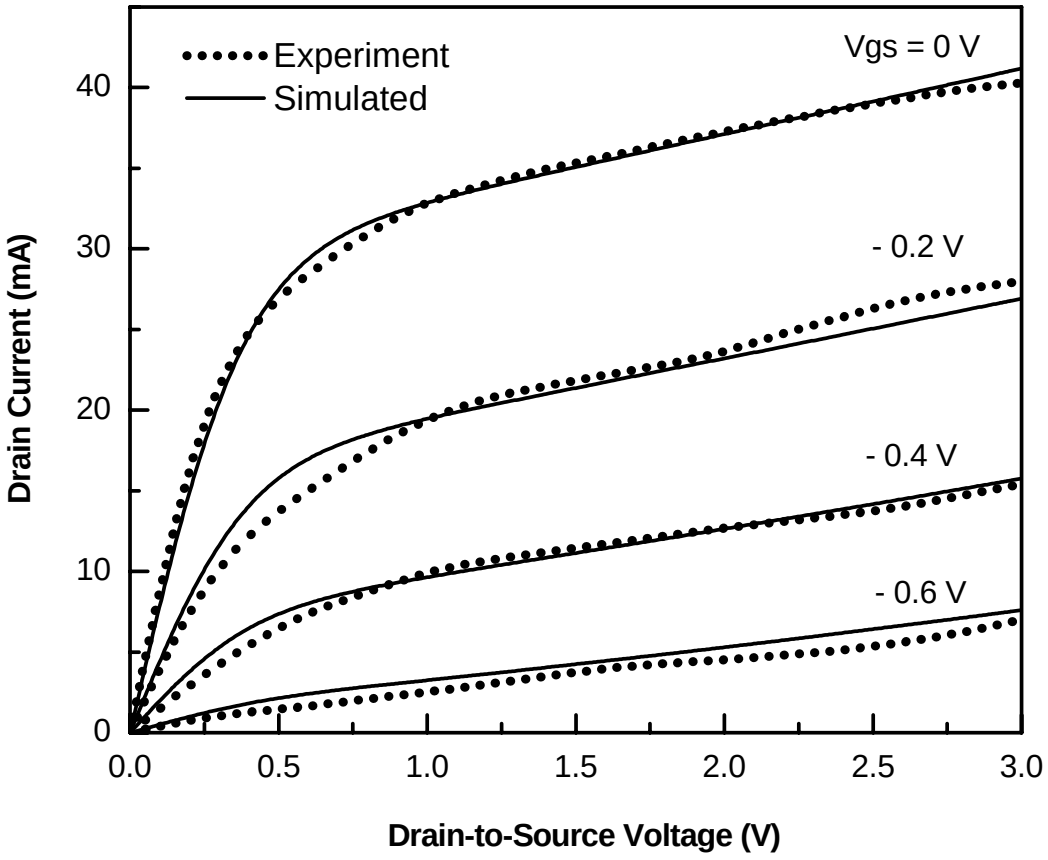


Figure (6.1): Observed and simulated output *I-V* characteristics of a 0.3 x 280 μm^2 GaAs MESFET.

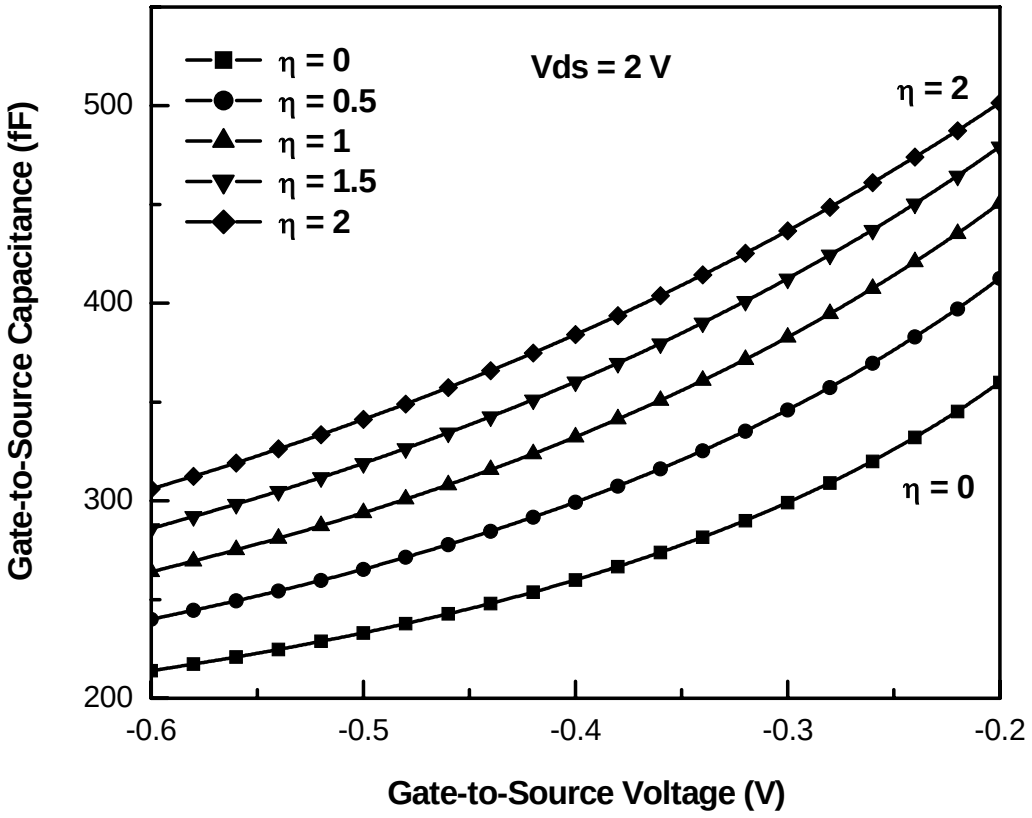


Figure (6.2): Variation in Gate-to-Source capacitance as a function of simulation parameter η for a 0.3 x 280 μm^2 GaAs MESFET.

consumed in changing the gate depletion thus increasing the value of C_{gs}. While a higher value of C_{gs} capacitor limits the high frequency response of the device [Wren-2005], which has not been taken care off in the model given by Equation (3.7.1). So, estimation of C_{gs} value by using this equation is bound to show a discrepancy in observed and simulated characteristics.

6.2.2. Gate-to-Drain Capacitance, C_{gd}

Another component that is used to evaluate AC performance of the device is C_{gd}. The magnitude of C_{gd} capacitor can be assessed as [Enoki-1990]

$$C_{gd} \approx \frac{\varepsilon_s \pi Z \sqrt{\Phi_b}}{2 A I_{ds}} \tag{6.2.3}$$

where

$$A = \sqrt{\frac{(V_{ds} - V_{gs} + \Phi_b)}{I_{ds}} - (R_d + R_s)} \tag{6.2.4}$$

Equation (6.2.3) shows the variation in C_{gd} values as a function of V_{gs} and V_{ds} whereas, Figure (6.3) shows variation in C_{gd} at different values of η. Comparing Figures (6.2) and (6.3), it is evident that the magnitude of C_{gd} is at least 10 times less than C_{gs}. Hence, C_{gd} will have a relatively lower impact in determining the AC response of a FET However, the plot of Figure (6.3) shows that there is a finite impact of η on the value of C_{gd}. Thus, the quality of the Schottky barrier can not be ignored if one has to determine an accurate AC equivalent circuit of a FET.

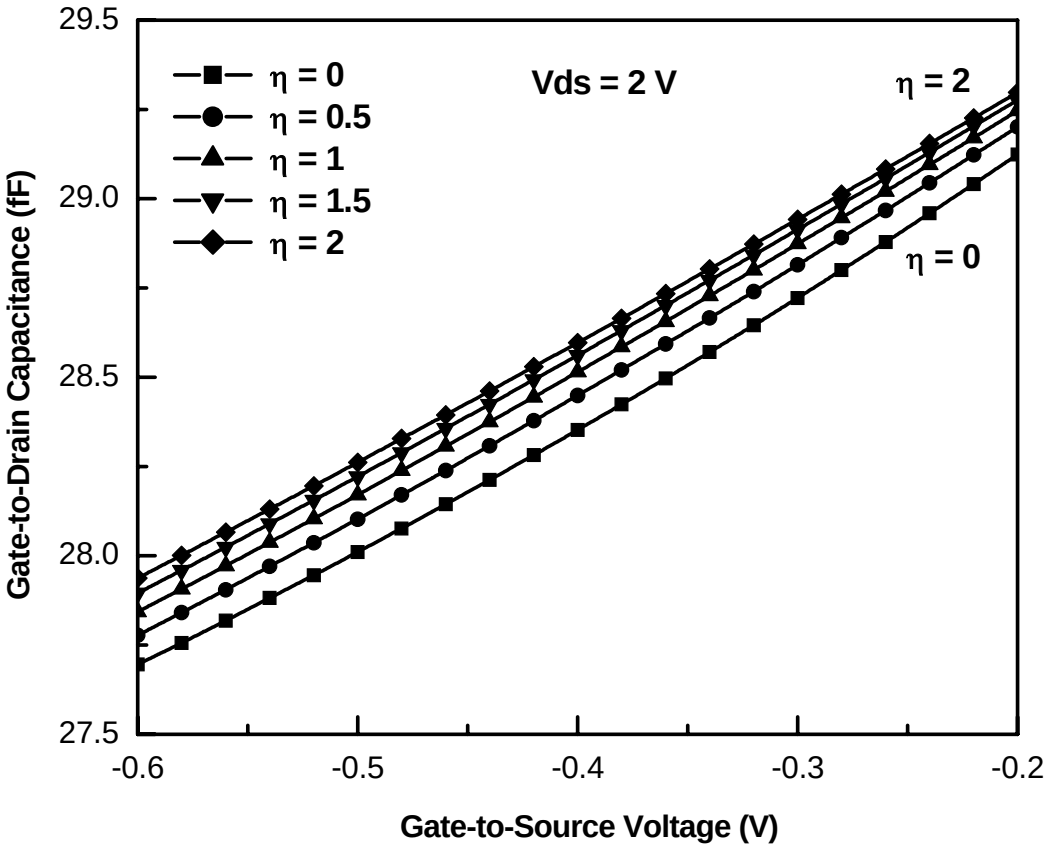


Figure (6.3): Variation in Gate-to-Drain capacitance as a function of simulation parameter η for a 0.3 x 280 μm^2 GaAs MESFET.

6.2.3. Drain-to-Source Capacitance, Cds

By considering the quarter circle approximation at the two edges of the Schottky depletion, the magnitude of Cds capacitor can be assessed as

$$C_{ds} \approx \frac{2\pi\varepsilon_s Z I_{ds}}{L_G} \times \sqrt{\frac{2\varepsilon_s A}{q N_d}} \qquad (6.2.5)$$

Equation (6.2.5) shows that the value of C_{ds} is dependent directly on channel current I_{ds}. Since L_G is small, i.e., less than 1 μm, therefore the contribution of C_{ds} in defining the AC response of the device is relatively higher than C_{ds}.

Figure (6.4) shows variation in C_{ds} as a function of V_{gs}. An important point to note is that the plot of Figure (6.4) represents an inverse profile compared to Figures (6.2) & (6.3). This could be associated with shrinking of gate depletion from the drain side while it is being pushed into the channel as shown in Figure (6.5) [Ladbrooke-1991, Niekerk-2000 and Niekerk-1998].

It is also worth mentioning that the value of C_{ds} decreases with increasing values of η while keeping V_{ds} and V_{gs} constant. This behavior is also once again contrary to what has been observed for C_{gs} and C_{gd} as shown in Figures (6.2) and (6.3) respectively. This, once again, supports the arguments of depletion modification as suggested in Figure (6.5).

6.2.4. Output Conductance, g_d

In short channel devices, the most unpredictable parameter is the value of g_d. A high value of g_d would mean that the gate has poor control on I_{ds} and as a result such devices will also have poor g_m. Ideally, the value of g_d after the onset of current

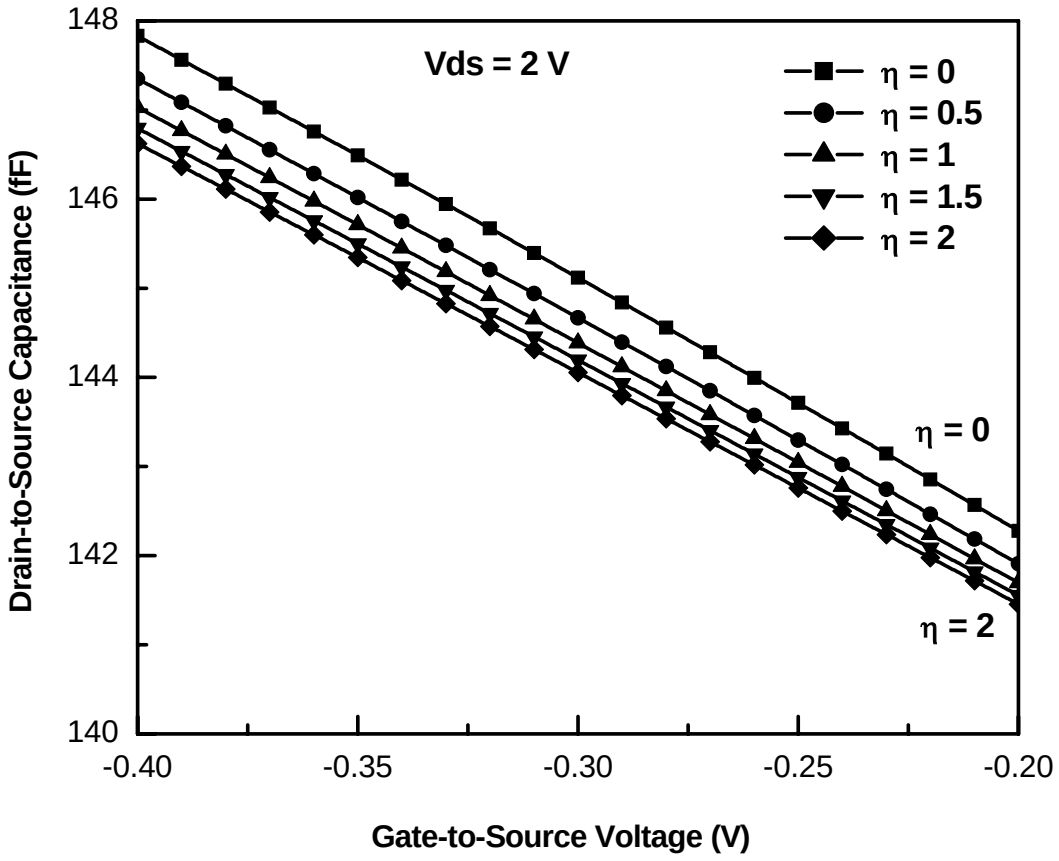


Figure (6.4): Variation in Drain-to-Source capacitance as a function of simulation parameter η for a 0.3 x 280 μm^2 GaAs MESFET.

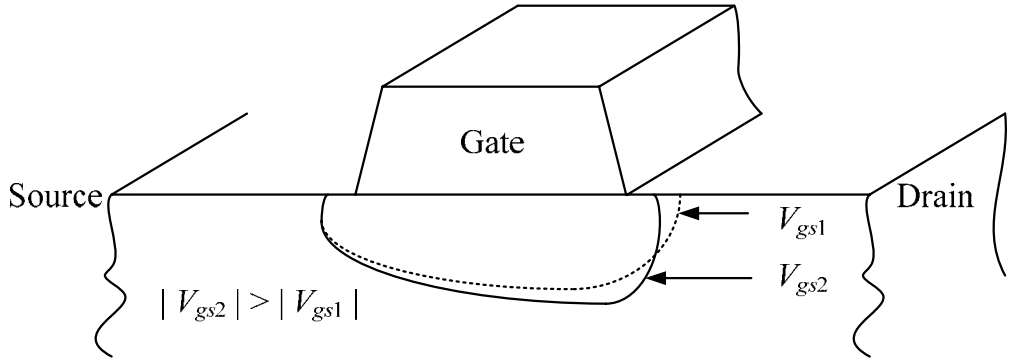


Figure (6.5): Modification in gate depletion by changing the potential at gate electrode.

saturation should be zero but in MESFET, especially, when $L_G < 1$ μm, its value is usually positive and heavily dependent on field conditions inside the channel. It is, therefore, highly advisable to calculate its value by involving the channel conditions as given by the following expression

$$g_d = 3\times\left\{\begin{array}{l} 2\,I_{dss}\left[1-\dfrac{V_{gs}}{(1+\eta\, e^{V_{gs}})\,(V_T+\Delta V_T+\gamma V_{ds})}\right]\times\left[\dfrac{\gamma V_{gs}}{(1+\eta\, e^{V_{gs}})\,(V_T+\Delta V_T+\gamma V_{ds})^2}\right] \\ \times\tanh(\alpha V_{ds})\,(1+\lambda V_{ds})+I_{dss}\left(1-\dfrac{V_{gs}}{(1+\eta\, e^{V_{gs}})\,(V_T+\Delta V_T+\gamma V_{ds})}\right)^2\times\tanh(\alpha V_{ds}) \\ \times(1+\lambda V_{ds})+\lambda\, I_{dss}\left[1-\dfrac{V_{eff}}{(1+\eta\, e^{V_{gs}})\,(V_T+\Delta V_T+\gamma V_{ds})}\right]^2\times\tanh(\alpha V_{ds}) \end{array}\right\} \tag{6.2.6}$$

A scaling factor of 3 is used in Equation (6.2.6) to accommodate the effects of Schottky barrier interface states and deep level traps [Ahmed-2008, Moiz-2005 and Moiz-2007]. These states and traps are ineffective at microwave frequencies and thus increases ~ 3 times the value of g_d relative to its study state value.

Figure (6.6) shows the variation in g_d versus V_{ds} at different values of η. The plot demonstrates that the presence of interface states do have an impact on the value of g_d which have been ignored conventionally.

6.2.5. AC Transconductance, $g_{m(ac)}$

The difference between AC and DC values of g_m is governed by τ, and is given by

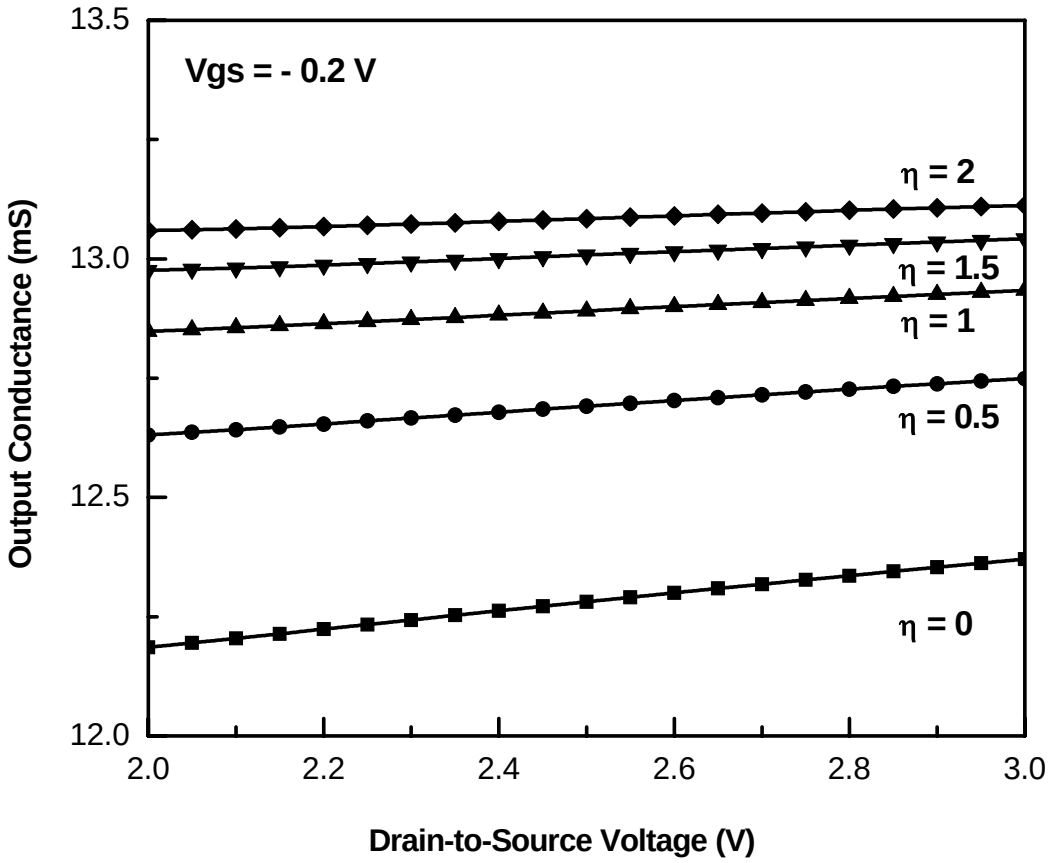


Figure (6.6): Variation in output conductance as a function of simulation parameter for a 0.3 x 280 μm^2 GaAs MESFET.

$$g_{m(ac)} = g_m \, e^{-j\omega\tau} \tag{6.2.7}$$

combining Equation (5.2.4) with (6.2.7)

$$g_{m(ac)} = 2\, I_{dss} \left[1 - \frac{V_{gs}}{(1+\eta\, e^{V_{gs}})\,(V_T + \Delta V_T + \gamma V_{ds})} \right] \times \tanh(\alpha V_{ds})\,(1+\lambda V_{ds})$$

$$\times \left[\frac{1}{(1+\eta\, e^{V_{gs}})} \left(1 - \frac{\eta V_{gs}}{(1+\eta\, e^{V_{gs}})} e^{V_{gs}} \right) \right] \times \left[\frac{-1}{V_T + \Delta V_T + \gamma V_{ds}} \right] \times e^{-j\omega\tau} \tag{6.2.8}$$

The variation of $g_{m(ac)}$ as a function of V_{gs} keeping η as a constant, is shown in Figure (6.7). The plot of the figure clearly demonstrates that increasing the value of η the magnitude of g_m reduces significantly. This fact may be attributed to the consumption of V_{gs} by the increased density of interface states at the Schottky barrier.

Increasing the frequency of oscillation at the gate, a point reaches where the gate signal cannot be amplified due to high leakage from gate Miller capacitors, this is a point called unity gain. The value of f_T is thus controlled by Miller capacitors and given by [Ladbrooke-1991 and Ahmed-2003]

$$f_T \approx \frac{g_{m(ac)}}{\pi (C_{gs} + C_{gd})} \tag{6.2.9}$$

where

$$\tau \approx \frac{1}{2} \left[\frac{C_{gs} + C_{gd}}{g_{m(ac)}} \right] \tag{6.2.10}$$

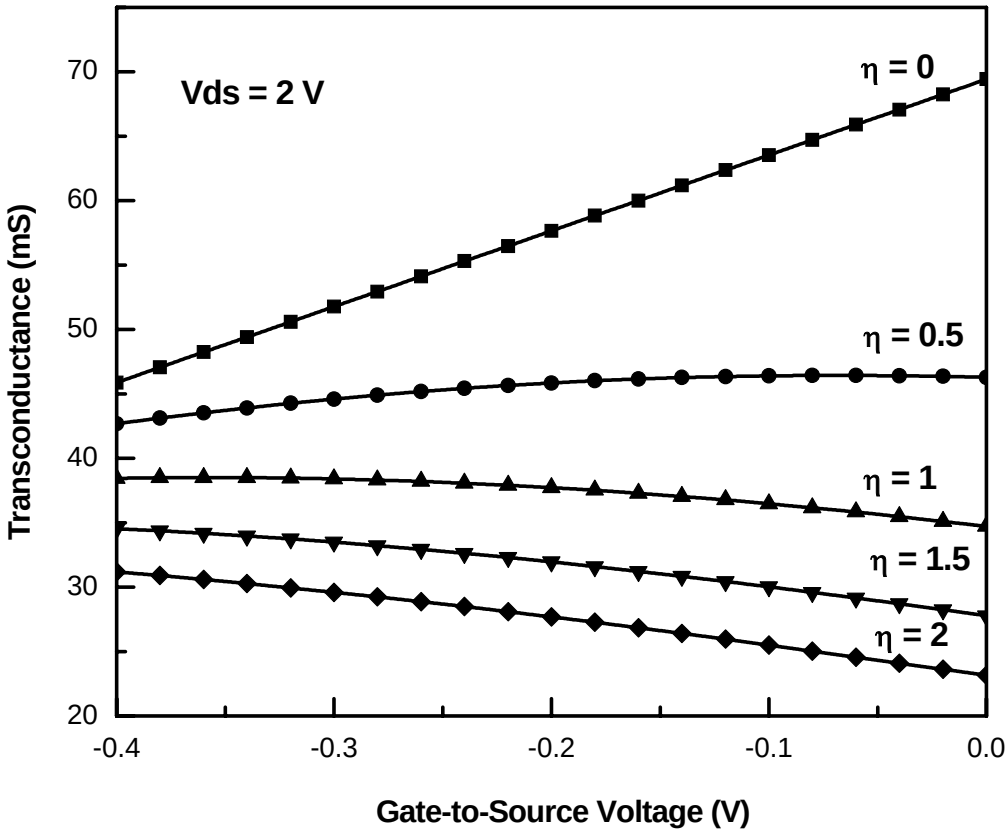


Figure (6.7): Variation in transconductance as a function of simulation parameter η for a 0.3 x 280 μm^2 GaAs MESFET.

A factor of and ½ in Equation (6.2.10) is used to accommodate the over shooting of the carriers in the entire channel due to the submicron gate geometry, which generates a very high electric field underneath the entire gate [Barton-1990 and Ahmed-2003]. The variation in f_T and τ as a function of V_{gs} with η as a variable is shown in Figure (6.8). The increasing value of τ by increasing η signifies the slow response of Schottky barrier gate due to the presence of interface states.

6.2.6. Channel Resistance, R_i

The value of R_i as a function of channel parameters and biasing potential is given by [Ahmed-2003]

$$R_i = \frac{1}{3}\left[\frac{v_s L_G}{\mu_e I_{ds}}\right] \tag{6.2.11}$$

Equation (6.2.11) represents R_i once the carriers have attained v_s and a factor of 1/3 is used as per Equation (6.2.6). Since the value of g_d is heavily dependent on the gate conditions so does the value of $R_{i.}$. Equation (6.2.11) thus incorporates the second order effects which a device may have during its fabrication. Figure (6.9) shows variation in the value of R_i verses V_{gs} with η as a variable. The plot shows that the values of R_i for submicron FETs are very low, i.e., less than 0.001 Ω.

6.3. Estimated MESFET AC Equivalent Circuit Parameters

The MESFET of Figure (6.1) is biased to V_{ds} = 2 V and V_{gs} = - 0.2 V for the estimation of AC parameters. A reasonably good DC fit shown in Figures (6.1) allows estimating AC parameters by using Equations (6.2.1) to (6.2.11). The evaluated AC parameters are summarized in Table-6.1. In this table a comparison has been made

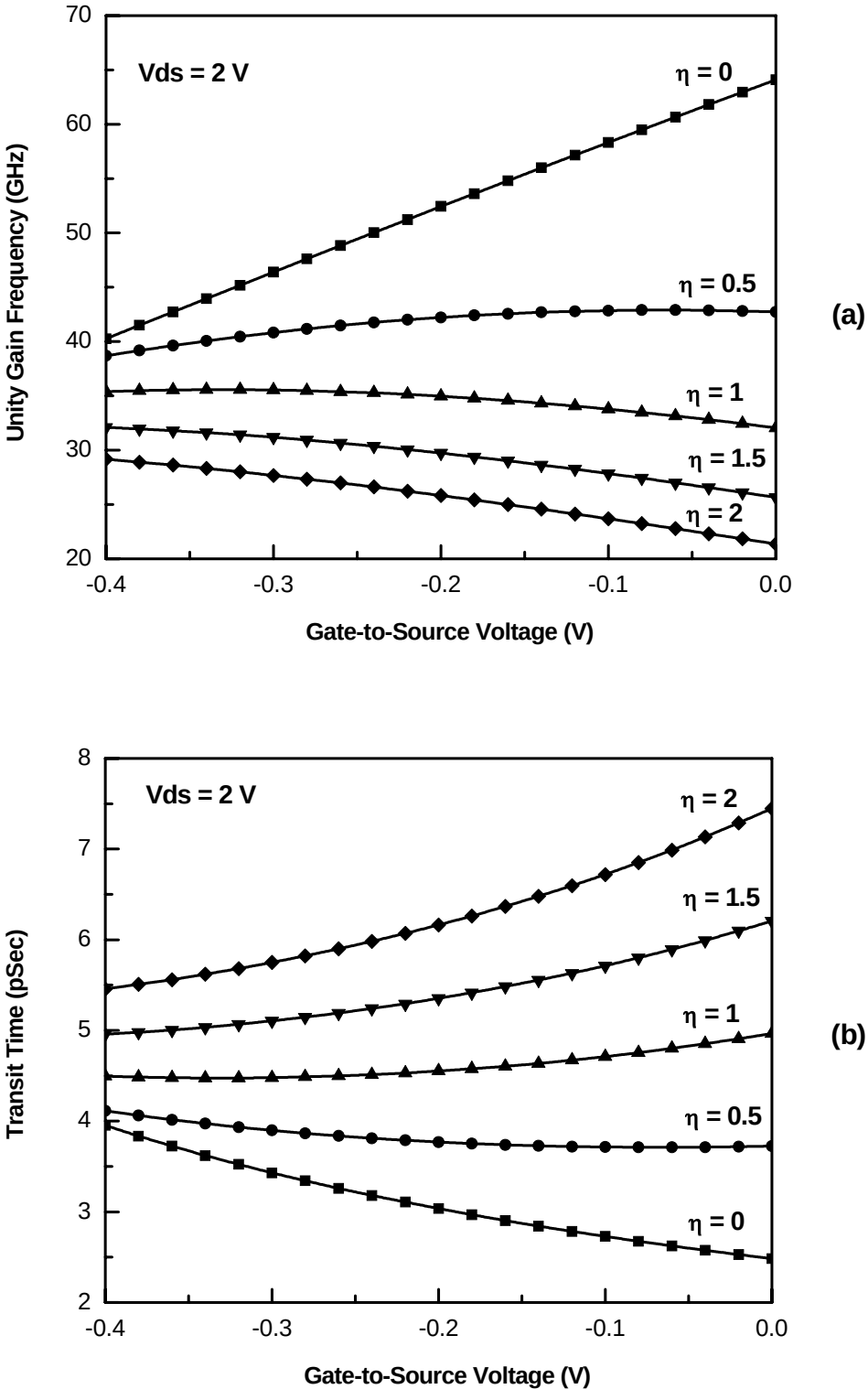


Figure (6.8): Variation in unity gain frequency and transit time delay as a function of simulation parameter for a 0.3 x 280 μm^2 GaAs MESFET.

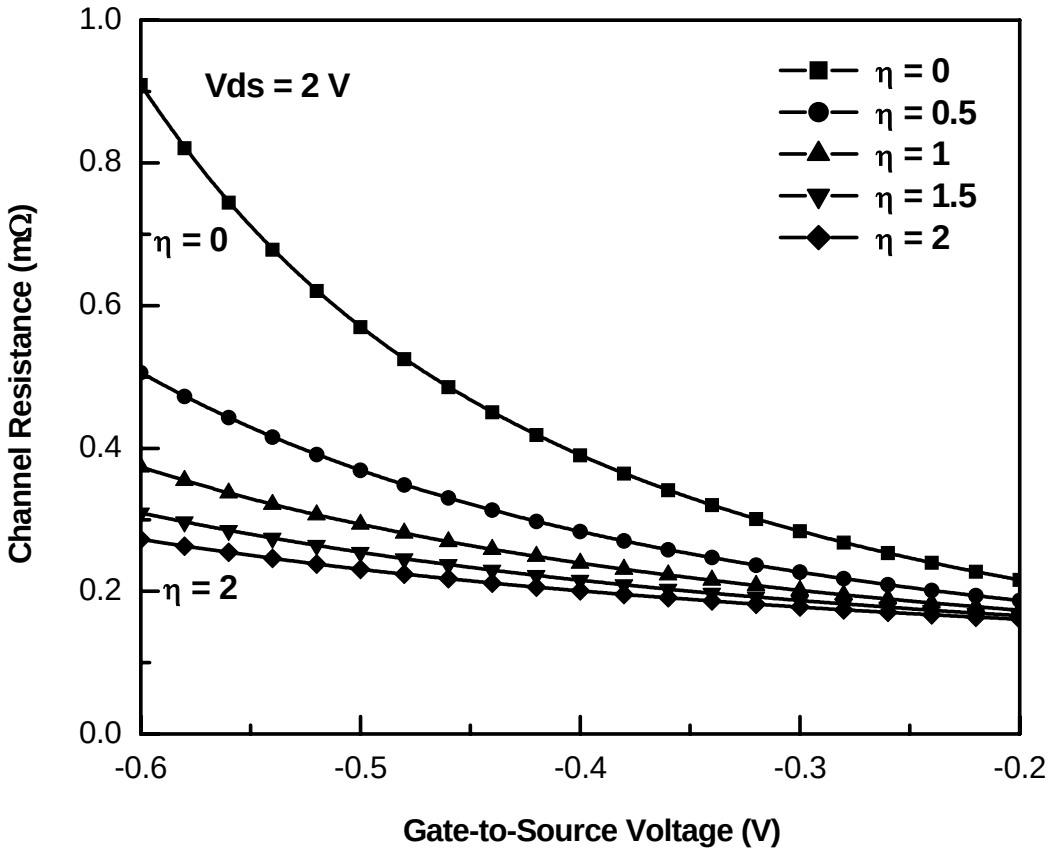


Figure (6.9): Variation in channel resistance as a function of simulation parameter η for a 0.3 x 280 μm^2 GaAs MESFET.

Table-6.1
Intrinsic equivalent circuit parameters of a 0.3 x 280 μm^2 GaAs MESFET [NE-71300] at Vds = 2 V and Vgs = - 0.2 V

Elements	Experiment	Estimated With		Difference %	
		Conventional Technique	New Technique	Conventional Technique	New Technique
R_i (mΩ)	0.25	0.27	0.25	8	0
g_d (mS)	13	12.2	13.2	- 6.15	+ 1.53
$g_{m(ac)}$ (mS)	50	57	49	+ 14	- 2
τ (pS)	5.2	3	5.2	- 42.3	0
C_{gs} (fF)	490	320	480	- 34.7	- 2.04
C_{gd} (fF)	32	29.1	29.5	- 9.06	- 7.81
C_{ds} (fF)	150	142.5	142.5	- 5	- 5

between the observed and calculated AC parameters both from the conventional as well as from the modified technique. Examining the data available in the table clearly shows that the modified technique is better and the values thus obtained are within acceptable experimental error margin.

In general, the proposed technique provides the estimation of AC intrinsic small signal parameters by using the device DC characteristics for variable Schottky barrier gate conditions. Since the surface states of a GaAs material are unavoidable [Dhar-2000 and Ahmed (a)-1995] and till to-date it is very hard to eliminate these states completely, so it is very hard to predict the Schottky barrier conditions of a finished device. The technique therefore provides an effective mechanism of estimating AC parameters through measured DC characteristics and it overcomes the limitations of a conventional model.

Consider the value of f_T given in Table-6.2 calculated by three different approaches. The data of Table-6.2 clearly demonstrates that one cannot rely on a model which assumes an ideal Schottky barrier conditions. Ahmed's model suggests that f_T of the device is ~ 52 GHz, whereas in actual, the device f_T is ~ 30 GHz. A slow response of the device as observed in the Ahmed model could be associated with Schottky barrier conditions and other second order effects.

6.4. Estimated HEMT AC Equivalent Circuit Parameters

The estimation of HEMT AC parameters are even more difficult than MESFET owning to the fact that there could be a parasitic FET other than interface states which could cause even more prominent second order effects [Hosoya-2003, Cidronali-2003, Wren-2005, Katz-2005, Wang-1986 and Das-1987]. This will lead to greater

Table-6.2
Unity gain frequency of a 0.3 x 280 μm^2 GaAs MESFET.

S. No.	Technique Used	Unity Gain Frequency f_T (GHz)
1	Experiment	30.62
2	Ahmed Model	51.86
3	Proposed Model	30.6

discrepancy between the observed and estimated values of intrinsic small signal AC parameters of a HEMT.

To demonstrate the validity of established technique for all types of FET devices, HEMTs of 0.3 x 280 μm^2 and 0.2 x 200 μm^2 are chosen. Figures (6.10) & (6.11) show the observed and simulated DC characteristics of the two chosen HEMT devices by employing the proposed technique. A good match in Figures (6.10) & (6.11) suggests that the technique could be extended to estimate AC parameters of submicron HEMTs. The estimated AC values using Ahmed and Proposed method along with experimental data are shown in Tables-6.3 & 6.4 for the devices of Figures (6.10) & (6.11) respectively. A reasonably good match between the observed and the estimated values demonstrate the validity of the proposed technique for submicron HEMTs. Hence, the established technique is a comprehensive one and allows to estimate AC intrinsic parameters based on DC measurements for all types of FET including those which offer second order effects due to their non-ideal Schottky barrier response.

6.5. Summary

This chapter deals with the estimation of intrinsic small signal parameters of GaAs MESFETs and HEMTs. The origins of small signal AC parameter were first discussed in detail by describing their dependence on the device physics.

To estimate AC parameters of a MESFET its DC characteristics were first evaluated; and the observed data were then simulated by using an algorithm involving a non-linear model. The model was capable to simulate *I-V* characteristics of GaAs MESFETs with varying Schottky barrier conditions. Thus, its incorporate second

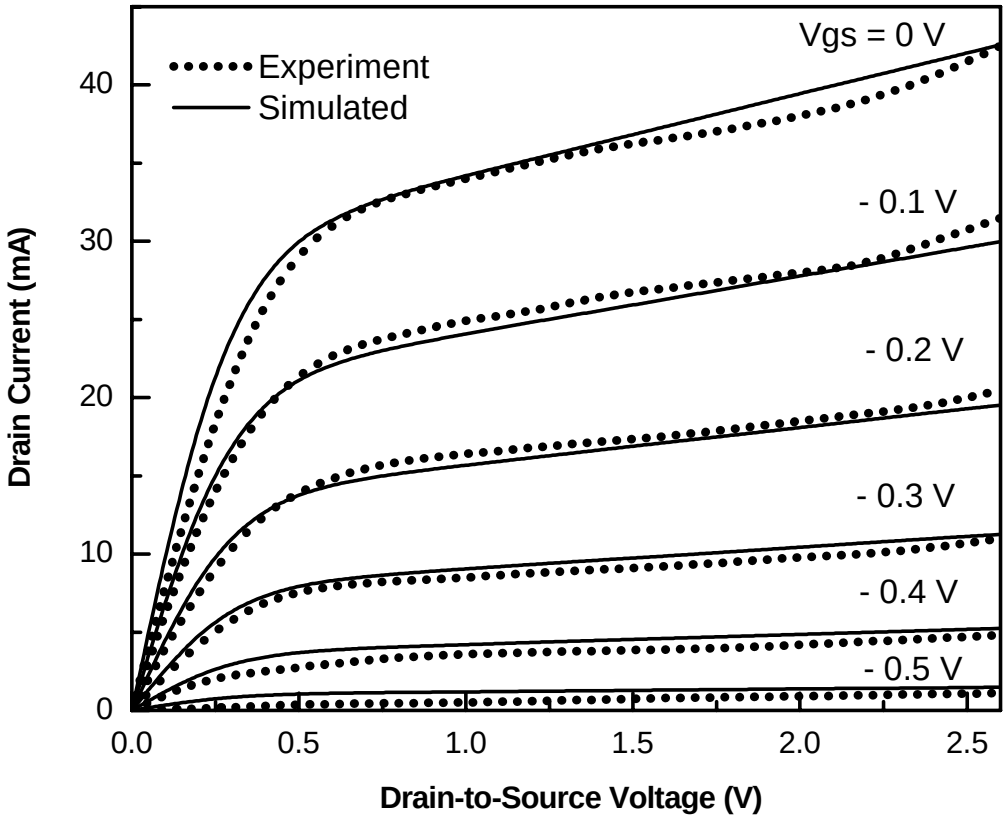


Figure (6.10): Observed and simulated output *I-V* characteristics of a 0.3 x 280 μm^2 GaAs HEMT.

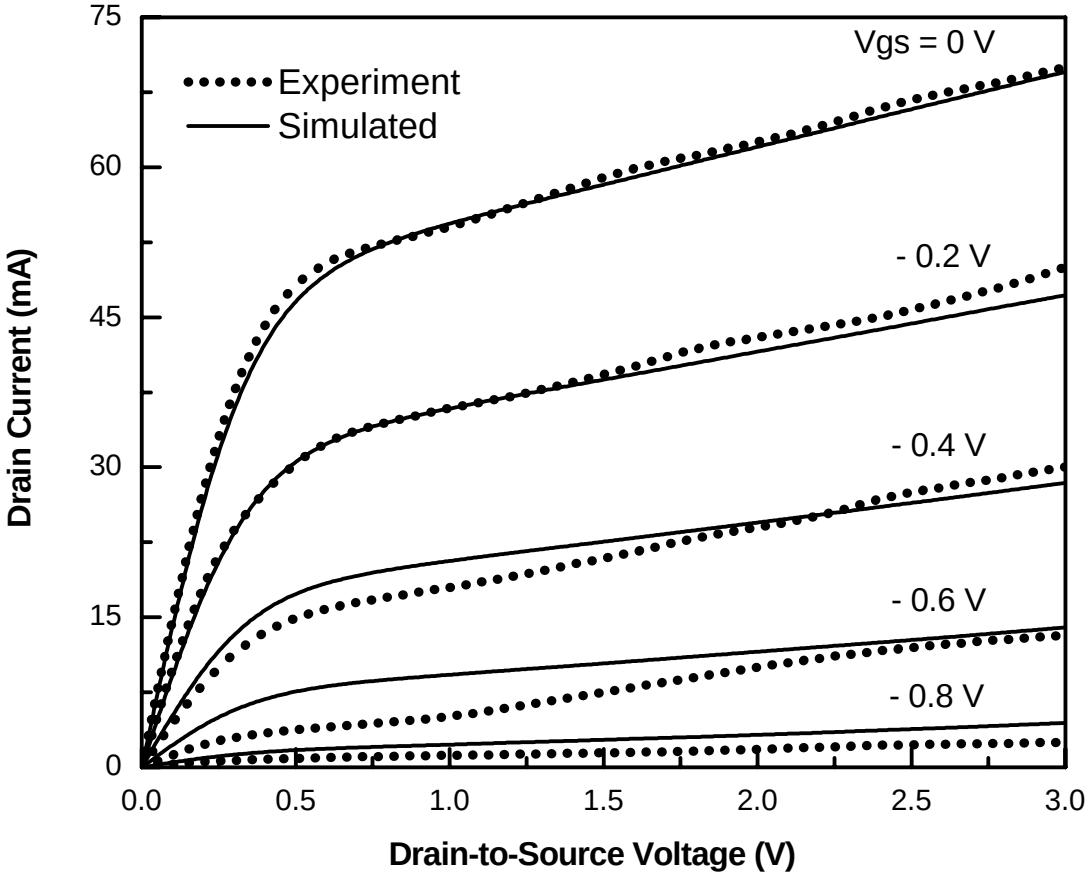


Figure (6.11): Observed and simulated output *I-V* characteristics of a 0.2 x 200 μm^2 GaAs HEMT.

Table-6.3
Intrinsic equivalent circuit parameters of a 0.3 x 280 μm^2 GaAs HEMT [NE-33200] at Vds = 2 V and Vgs = - 0.2 V.

Elements	Experiment	Estimated With		Difference %	
		Conventional Technique	New Technique	Conventional Technique	New Technique
R_i (mΩ)	2	2.8	1.5	+ 40	- 25
g_d (mS)	14	7.2	12.4	- 48.57	- 11.42
$g_{m(ac)}$ (mS)	50	68	50	+ 36	0
τ (pS)	4	2.5	3.9	- 37.5	- 2.5
C_{gs} (fF)	400	382	395	- 4.5	- 1.25
C_{gd} (fF)	50	43.4	43.9	- 13.2	- 12.2
C_{ds} (fF)	160	155.5	157	- 2.81	- 1.87

Table-6.4
Intrinsic equivalent circuit parameters of a 0.2 x 200 μm^2 GaAs HEMT [NE-32584C] at Vds = 2 V and Vgs = -0.4 V.

Elements	Experiment	Estimated With		Difference %	
		Conventional Technique	New Technique	Conventional Technique	New Technique
R_i (mΩ)	1	1.5	1	+ 50	0
g_d (mS)	15	7	13.5	- 53.33	- 10
$g_{m(ac)}$ (mS)	50	75	55	+ 50	+ 10
τ (pS)	5	2.5	3.5	- 50	- 30
C_{gs} (fF)	300	215	280	- 28.33	- 6.66
C_{gd} (fF)	20	18	18.4	- 10	- 8
C_{ds} (fF)	130	148	148	+ 13.84	+ 13.84

order effects a device may have in its characteristics due to its technological constraints.

During the evaluation process, once a good match was attained then by employing simulated *I-V* characteristics intrinsic small signal parameters were estimated. The data thus obtained were compared with the observed one and it was found that the proposed technique was better than its counterparts.

The established technique was also applied on GaAs HEMTs having submicron L_G and it was observed that it can also simulate, to a reasonable accuracy, both DC and AC characteristics of submicron HEMTs. In general, it has been demonstrated that the proposed method is accurate as well as efficient to estimate AC parameters of GaAs FETs by using their DC characteristics and could be a useful tool in device simulation software.

Chapter 7

Conclusion and Future Work

This thesis discusses electrical response of submicron GaAs MESFETs and HEMTs to develop a physical model. The output and transfer characteristics are evaluated as a function of device Schottky barrier quality. An attempt is made to explain the observed electrical response of FETs by using physical modeling techniques.

Nine different FET models have been presented and their ability to simulate submicron GaAs MESFET's characteristics are checked by developing a software tool. These models have been examined and discussed by considering the variables involved in their definition along with fitting parameters. To demonstrate the validity of a model, *I-V* characteristics of short channel MESFETs, are simulated and compared with experimental data. The accuracy of a model is reported by evaluating its RMS error values as a function of device biasing. It is noted that the Ahmed model, when applied to high frequency MESFETs, offers better simulation results compared to other available models. Whereas, the simulated results of McNally and

Islam models are close to the Ahmed model. However, none of the model simulates accurately for devices having finite interfacial layer thickness.

First, a comprehensive new model is developed to simulate *I-V* characteristics of short channel GaAa FETs. The validity of the model is checked by simulating output and transfer characteristics of different devices. The performance of this model is compared with the best available model, by calculating RMS error values. It has been demonstrated that the proposed model is a comprehensive one, capable of simulating DC characteristics of GaAs MESFETs including those having significant non-ideal Schottky barrier response. The model has also been applied successfully on *I-V* characteristics of GaAs HEMTs with non-ideality caused by the parasitic FET. It has been shown that the proposed model could be a useful tool for device simulators involving short channel FETs.

Second, the effects of the interfacial layer on the Schottky barrier height of submicron GaAs MESFET have been studied. It has been shown that the presence of a interfacial layer causes soft reverse characteristics of a Schottky barrier diode with higher current density, which cannot be explained fully by thermionic emission theory. The increased magnitude of the Schottky current is associated with the Schottky barrier lowering caused by the masking of the applied gate potential across the interfacial layer. This layer is of atomic nature, which has finite thickness. It can hold potential across it, but behaves as a transparent medium for the flow of current. The quality of a Schottky barrier can be assessed by the magnitude of current flowing from it.

Furthermore, the Schottky barrier interfacial layer dependent performance of submicron GaAs MESFETs has been discussed by using their output and transfer

characteristics. The mobility of carriers, scattering from the channel into the Schottky barrier gate, increases significantly for the devices which have relatively thicker interfacial layer. The negative effects of increased carriers' mobility from MESFET Schottky barrier gate are discussed and a plausible explanation is given for reduced barrier lowering in the presence of interfacial layer. While considering the negative effects of interfacial layer, it has been shown that the value of threshold voltage and transconductance decreases inversely with the thickness of oxide layer, whereas, the value of output conductance increases directly with it. Based on the proposed explanation the definition of threshold voltage has been redefined involving the concept of interfacial layer thickness.

Third, a technique is developed to estimate intrinsic small signal parameters of GaAs MESFETs and HEMTs. In the proposed technique DC characteristics of a device under consideration are first evaluated. The observed characteristics are then simulated by using the proposed model. The developed model has the capability to simulate *I-V* characteristics of GaAs MESFETs with varying Schottky barrier conditions. Thus, it incorporates second order effects a device may have in its characteristics due to technological constraints.

During AC parameters extraction process, once a good DC match is attained then by employing simulated *I-V* characteristics, intrinsic small signal parameters are evaluated for which a complete set of mathematical expressions has been discussed. To check the validity of the proposed technique for submicron GaAs MESFETs of varying gate length have been simulated. The parameters thus obtained are compared with the observed one and it has been shown that the proposed technique gives better results than its counterparts.

The established technique is also applied on GaAs HEMTs having submicron gate length. This technique can also simulate, to a reasonable accuracy, both DC and AC characteristics of submicron HEMTs, even those which do not follow the square law condition. In general, it has been shown that the proposed method is accurate as well as efficient in estimating AC parameters of GaAs FETs by using their DC characteristics, and could be employed as a useful tool in device simulation software.

The project could be extended for the estimation of S-parameters of the device based on calculated intrinsic small signal parameters. Once a good match between the observed and simulated S-parameter is attained, the data can be translated into Y-parameters. This will enable a design engineer to calculate the device physical parameter through its electrical measurements. The tool thus established will be comprehensive. It can be employed in device simulation software which involves submicron GaAs FETs to predict their DC and AC characteristics.

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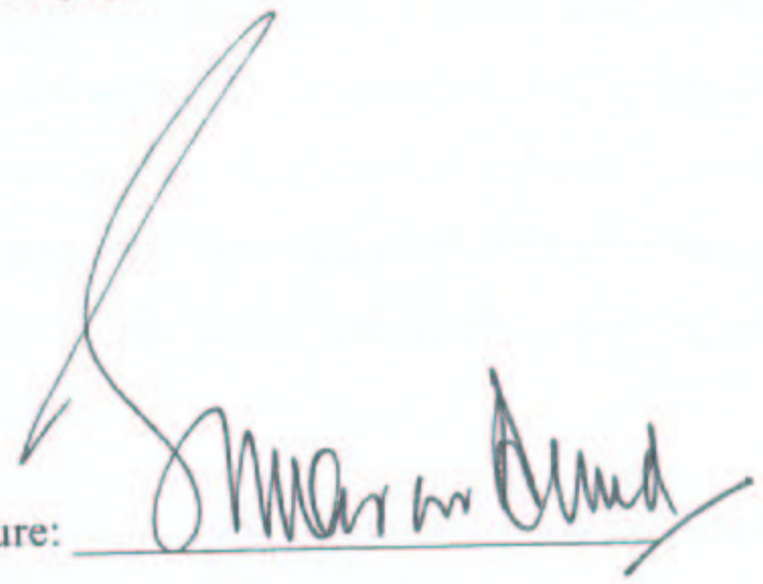
Certificate

It is certified that the research work contained in this dissertation has been carried out under the supervision of Dr. Muhammad Mansoor Ahmed, at Mohammad Ali Jinnah University, Islamabad Campus. It is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Signature: 

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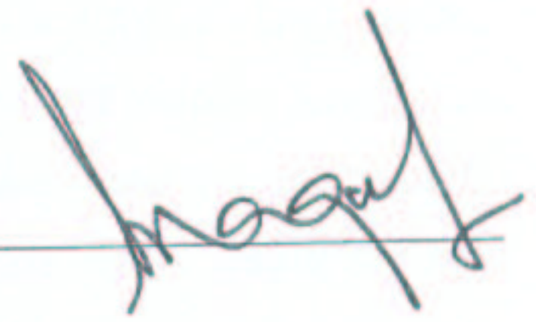
Signature: 

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