CAPITAL UNIVERSITY OF SCIENCE AND TECHNOLOGY, ISLAMABAD


# Harmonic and Switching Loss Analysis of Improved Space Vector Modulation for Modular Multilevel Converters

by

Ghufran Ul Haq

A thesis submitted in partial fulfillment for the degree of Master of Science

in the

Faculty of Engineering
Department of Electrical Engineering

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*I dedicate this work to my loving parents*


# CERTIFICATE OF APPROVAL

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Ghufran Ul Haq

(MEE171028)

### THESIS EXAMINING COMMITTEE

| S. No. | Examiner | Name | Organization |
|---|---|---|---|
| (a) | External Examiner | Dr. Muhammad Jafar | FAST, Islamabad |
| (b) | Internal Examiner | Dr. Muhammad Ashraf | CUST, Islamabad |
| (c) | Supervisor | Dr. Umer Amir Khan | CUST, Islamabad |

Dr. Umer Amir Khan
Thesis Supervisor
December, 2020

Dr. Noor Muhammad Khan
Head
Dept. of Electrical Engineering
December, 2020

Dr. Imtiaz Ahmad Taj
Dean
Faculty of Engineering
December, 2020

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**(Ghufran Ul Haq)**

Registration No: MEE171028

# *Abstract*

Different pulse width modulation techniques which include sinusoidal pulse width modulation, space vector modulation and nearest level modulation are used to generate the output of inverter in order to convert DC voltage into AC. Space vector modulation technique is the best among all these techniques because it gives less THD and less losses during switching as compared to others.

However increase in the number of levels of inverter causes the space vector modulation technique more complex, more switching states are stored in the memory and it is difficult to implement. This study presents an improved space vector pulse width modulation which simplifies the detection of the head of the reference vector and gives a simpler method to generate the switching sequences which were generated by complex algorithms earlier. The presented space vector modulation technique is improved and easy to implement. The detection of rotating reference vector is easy as the number of levels increases so this technique can be applied to modular multilevel converters (MMCs). This improved space vector technique is applied to 2-level VSI, 5-level MMC and 21-level MMC. A method to calculate the switching losses during switching is also developed. Results of THD and switching losses are compared with the conventional sinusoidal pulse width modulation to demonstrate that the presented technique is suitable for VSI and MMC or not. Simulation results of THD for 2-level VSI, 5-level MMC and 21-level MMC are given in MATLAB/Simulink. Switching losses results for 2-level VSI and 5-level MMC are performed.

# Contents

# List of Figures

# List of Tables

# Abbreviations

| | |
|---|---|
| **AC** | Alternating Current |
| **DC** | Direct Current |
| **HVDC** | High Voltage Direct Current |
| **Hz** | Hertz |
| **H** | Henry |
| **IGBT** | Insulated Gate Bipolar Transistor |
| **kHz** | Kilo Hertz |
| **LCC** | Line Commutated Converter |
| **MMC** | Modular Multilevel Converter |
| **MOSFET** | Metal Oxide Semiconductor Field Effect Transistor |
| **PWM** | Pulse Width Modulation |
| **PV** | Photovoltaic |
| **SSVPWM** | Simplified Space Vector Pulse Width Modulation |
| **SM** | Sub Module |
| **SMs** | Sub Modules |
| **SPWM** | Sinusoidal Pulse Width Modulation |
| **SVM** | Space Vector Modulation |
| **THI** | Third Harmonic Injection |
| **THD** | Total Harmonic Distortion |
| **VSI** | Voltage Source Inverter |
| **W** | Watt |

# Symbols

| | |
|---|---|
| $V_{ref}$ | Reference vector rotating inside space vector diagram |
| $V_a$ | Voltage of Phase A |
| $V_b$ | Voltage of Phase B |
| $V_c$ | Voltage of phase C |
| $S_{wa}, S_{wb}, S_{wc}$ | Switching states of phase A,B and C |
| $V_{dc}$ | DC voltage |
| $V_{refnew}$ | New reference vector |
| $T_s$ | Sampling Period |
| $E_{on}, E_{off}$ | Turn on and turnoff energies |
| $I_c$ | Collector current |
| $V_{CES}$ | Blocking voltage |
| $V_{ccnom}, I_{cnom}$ | Voltage and current taken from data sheet |
| $K_v$ | Exponent of voltage dependencies |
| $t$ | Time |
| $V_{an}$ | Phase to neutral voltage of phase A |
| $n_{up}, n_{low}$ | Sub modules in upper and lower arm of MMC |
| N | Number of sub modules |

# Chapter 1

# Introduction

## 1.1 Background

Energy was mainly produced by fossils fuels in the past which lead to carbon emissions and very bad effects on the environment and all living beings. The energy produced was mainly from fossil fuels which are depleting, due to that the energy produced from solar, wind and other renewable energy sources has come into focus.

Solar and Wind energy are now used in most of the countries these renewable sources produce DC power. Most of our home devices work on AC so there is a need to convert DC power into AC. Inverter is a device which converts DC power into AC. An inverter has the following modes of operation: standalone inverter, grid tied inverter and bimodel inverter.

A stand alone inverter is not connected to the grid; it provides fixed voltage for AC loads. A grid tied inverter is connected to the grid; the frequency and phase of the output voltage of the inverter is matched with the grid. A bimodel inverter has the hardware which makes the inverter operate in both standalone and grid-tied modes according to the conditions.

A three phase 2-level inverter generates the output voltage by varying the duty cycle of the pulse given to the gate of the IGBT. The power electronic switches at

non zero currents and voltages causes switching losses. The output produced by the inverter is not purely sinusoidal and have some distortion. These distortions are the integer multiples of fundamental frequencies.

One of the measures of harmonics in the power system is total harmonic distortion (THD). These harmonic distortions are very dangerous as they produce heat and damages the equipment so these harmonics must be reduced.

Switching frequency is increased to reduce the THD but the disadvantage of increasing the switching frequency is more losses during switching as it is directly proportional to the losses during switching.

Different PWM techniques such as SPWM , nearest level modulation and SVPWM were developed to control the switching devices in power electronic converter. These PWM techniques are also used to reduce the THD to some extent. SVPWM produces less THD and switching losses as compared to other PWM techniques.

SVPWM technique gives less THD as compared to other PWM techniques but it is difficult and very complex method for higher level converters. A simpler SVPWM technique is needed for multilevel converters.

## 1.2 Motivation

These harmonic distortions can be very dangerous and can damage the equipment. These distortions can also lead to losses and heating in electromagnetic devices such as transformers, motors etc. Capacitors which are used for reactive power compensation for power factor improvement in the system, if the harmonics are high this can lead to resonant conditions and further leads to more harmonics in voltage and current. So these harmonic distortions must be reduced to certain level [1].

It has been seen that SVPWM produces less THD and switching losses as compared to other PWM techniques [2]. Although SVPWM technique produces less THD as compared to other PWM strategies in 2-level VSI, the harmonics produced by 2-level VSI are more than the specified limits. Filters are also used to reduce the harmonic content in output voltage of 2-level VSI but the designing of

the filters for high harmonic system is very costly [3]. In order to further reduce the harmonics multilevel converters are used. However this SVPWM technique becomes complicated and difficult to implement in high level converters. This study is conducted in the motivation to develop an algorithm which simplifies the SVPWM technique for multilevel converters so that we can take into account the benefits of the SVPWM technique.

## 1.3 Inverters

In this study improved SVPWM technique is applied to DC to AC converters (inverters). Inverter is a device which converts DC power coming from renewble resources like PV system and wind turbines into AC for the appliances used in our homes. Inverters can be classified on modes of operation.

### 1.3.1 Modes of Operation of Inverter

There are three modes of operation of inverters.

- Standalone inverter
- Grid-tied inverter
- Bimodel inverters

#### 1.3.1.1 Standalone Inverters

PV systems which are not connected to grid have standalone inverters connected to them. Standalone inverters generate AC output of fixed voltage and frequency for AC load. In the day inverter converts the DC coming from the PV system to AC power and the extra power is stored in the storage devices i.e. batteries. At night inverter converts the DC coming from the batteries to AC [4]. Standalone inverter connected to PV system is shown in the Figure 1.1.

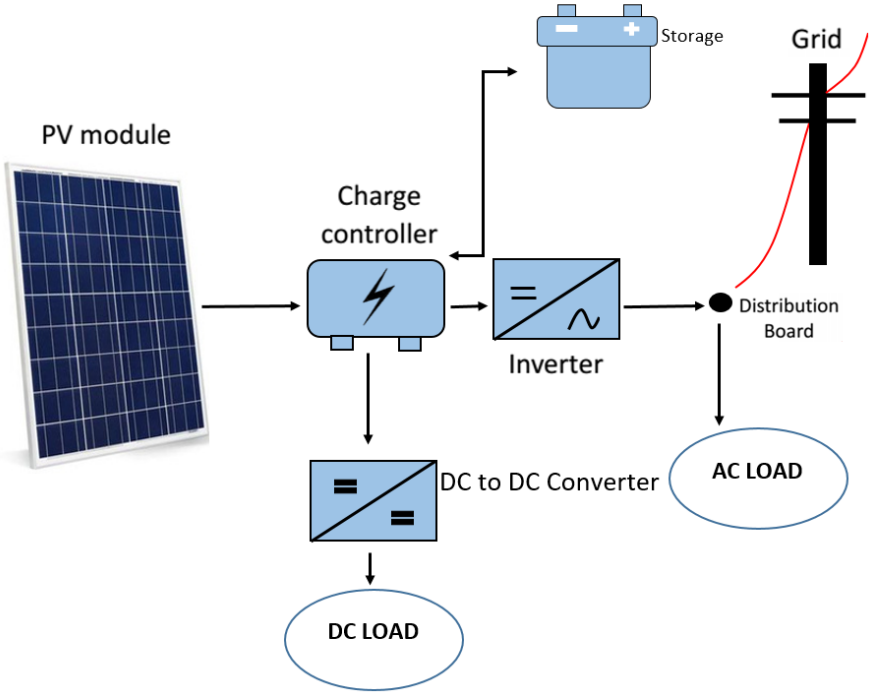



FIGURE 1.1: Standalone PV System With Standalone Inverter

#### 1.3.1.2 Grid-Tied Inverters

Grid-tied inverters are connected to the grid as shown in the Figure 1.2. An inverter which is connected with the grid has grid frequency, voltage and phase. PLL is used to synchronize the phase of the inverter with the grid [5].

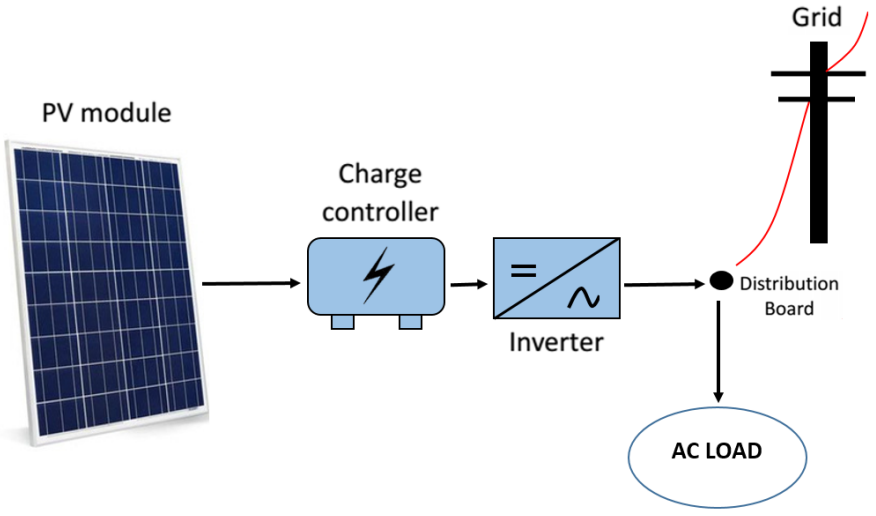



FIGURE 1.2: Grid Tied PV System With Grid Tied Inverter

The inverter injects AC power into the grid. The grid acts as voltage source and the inverter which injects AC power acts as the current source. The user can inject excess power generated by the PV system to the grid and can get compensation in the electricity bill using net metering. No batteries are required in grid connected system the grid acts as a voltage source which makes the system cheaper and saves the user from maintenance of the batteries Ref. [4].

#### 1.3.1.3 Bimodel Inverters

Bimodel inverter can act as both standalone and grid-tied inverter as shown in the Figure 1.3. It has the required hardware to act as grid-tied and standalone as per operating conditions. The PV system in which bimodel inverters are used also contains a battery bank. The battery bank can store power temporarily and can supply the power to the grid during the hours when the user get paid more for the price of the unit [4].

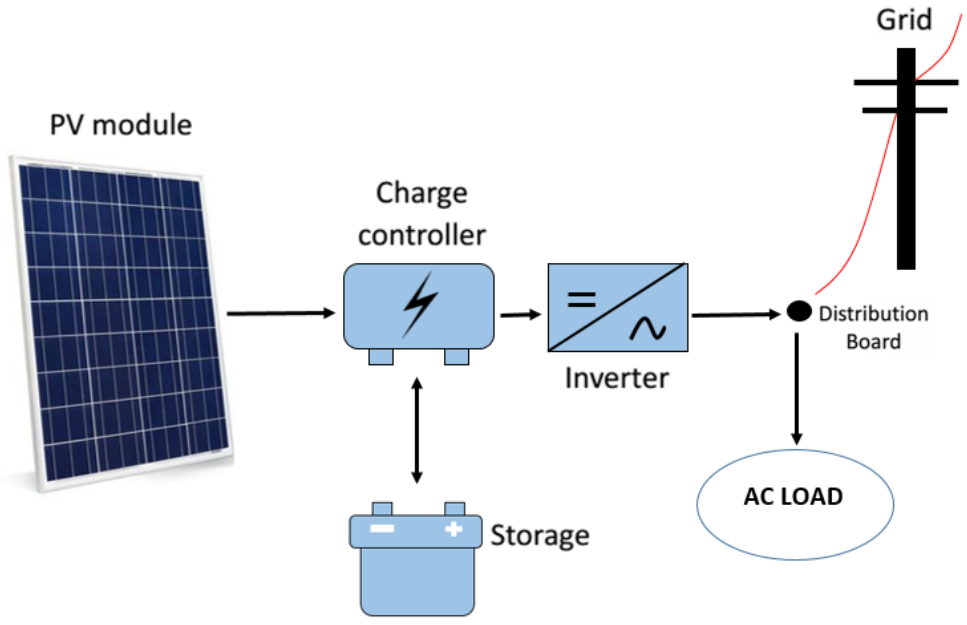



FIGURE 1.3: Grid Tied PV System With Bimodel Inverter

In order to improve the quality of AC power, PWM is used in inverters. PWM is a method to control the power electronic switch in an inverter.

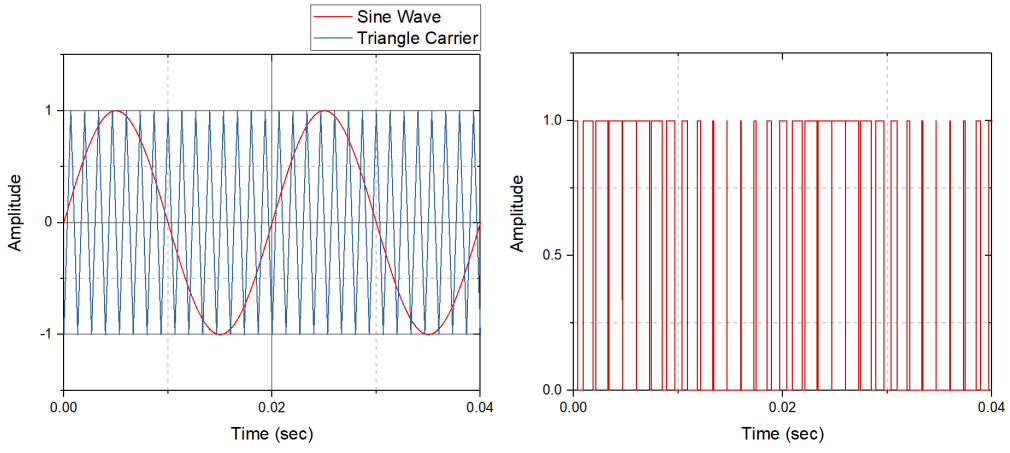
## 1.4 Overview of Pulse Width Modulation Techniques

Power electronic switches in inverters transition from off to on state and on to off state in order to generate the AC output. To improve the quality of AC output generated by the inverter PWM techniques are used some of which are given below

- Sinusoidal pulse width modulation
- Third harmonic injection
- Space vector modulation

### 1.4.1 Sinusoidal Pulse Width Modulation

In SPWM simple sine wave is compared with a triangular carrier to get the gating signals. The modulation index is defined as the ratio of amplitude of reference sine wave to the amplitude of the carrier wave. When ever the instantaneous value of sine wave is higher than that of the carrier wave the gate pulse will be high and when the instantaneous value of sine wave is less than that of carrier wave the gate pulse will be low as shown in the Figure 1.4 [6].




(a) Comparison of Sine Wave With Triangular Carrier

(b) Gate drive signals using SPWM

FIGURE 1.4: Generation of Gate Drive Signals By Comparing Sine Wave With Triangular Carrier

In SPWM when the peak of the reference sine wave is greater than that of the triangular wave over modulation occurs and the THD of the output voltage increases in SPWM [7].

### 1.4.2 Third Harmonic Injection Pulse Width Modulation

In THI PWM, summation of fundamental and $3^{rd}$ harmonic is done to generate the modulating signal and compared with the triangular carrier to generate the gate pulses. Due to the addition of $3^{rd}$ harmonic component in reference voltage the output is 15.5 % more then the conventional SPWM [6].
In this PWM technique the fundamental sine wave which has a frequency of 50 Hz. This 50Hz frequency is multiplied with 3 to generate the $3^{rd}$ harmonic component. This $3^{rd}$ harmonic component is added to the fundamental sine wave as shown in the Figure 1.5 [8].

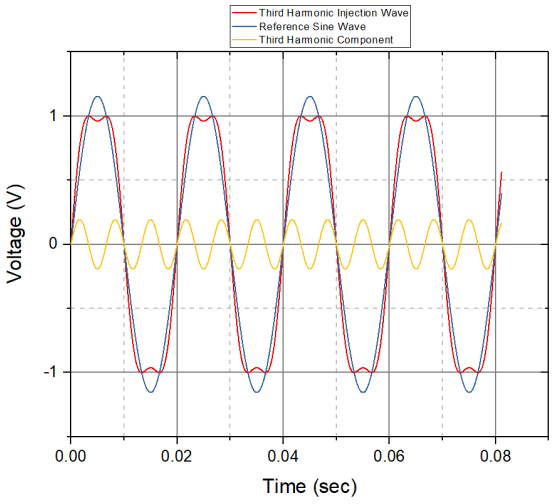



FIGURE 1.5: Summation of Fundamental and Third Harmonic Component for THI PWM [9]

### 1.4.3 Space Vector Modulation (SVM)

SVM takes the switching states of the inverter and generates a reference vector which rotates in hexagon that produces sinusoidal output voltage. SVPWM works with the line voltages it provides better DC bus voltage utilization, low harmonic

content and lower switching losses as compared to SPWM [2]. In the above mentioned PWM techniques SVPWM turns out to be the best as it gives less total harmonic distortion (THD) and switching losses.

## 1.5 Objective

The main objective of this study are :

- To develop a simplified and improved SVPWM algorithm.
- To apply this algorithm to 2-level VSI and modular multilevel converters.
- To analyze the total harmonic distortion and losses during switching of the converter at different load conditions.

## 1.6 Thesis Outline

The rest of the thesis is organized in the chapters as given below:
Chapter 2
Chapter 2 discusses the previous work done on SVPWM technique. It also discusses the gap in the recent research and problem statement is formed in light of the gaps in the research. It also gives the research methodology and software used to conduct the simulations.
Chapter 3
Chapter 3 discusses the proposed improved space vector technique. Also flow chart of the presented technique is given in this chapter.
Chapter 4
Chapter 4 discusses the modular multilevel converters and its sub-module topologies. It also gives a mathematical approach to find arm voltages and currents. This chapter also describes the modeling of MMC in Simulink.
Chapter 5 gives the simulation and results of harmonic distortion and switching

losses between SPWM and improved SVPWM technique which is applied on 2-level VSI, 5-level MMC and 21-level MMC.

Chapter 6

Chapter 6 gives the conclusions drawn from the above study and future work which can be done using this improved SVPWM.

# Chapter 2

# Literature Review

## 2.1 SVPWM for 2-level VSI

SVPWM technique takes the switching states of the inverter and generates a reference vector which rotates in a hexagon that produces sinusoidal output voltage. SVPWM works with the line voltages it provides better DC bus voltage utilization, low harmonic content and lower switching losses as compared to SPWM [2]. In the above mentioned PWM techniques SVPWM turns out to be the best as it gives less total harmonic distortion (THD) and switching losses.

The authors in [2] discuss the SVPWM in which pulse is generated by switching three-phase two-level inverter depending on the switching of eight different voltage vectors. These eight voltage vectors form a hexagon consisting of six sectors. A voltage vector rotates in this hexagon and forms a sinusoidal output. In order to generate the required gating pulses the voltage vector which is rotating in the hexagon is synthesized. Then the sector in which the reference vector is located is determined and the duty cycle is calculated for the pulses which is fed to the gate of the IGBT.

The authors in [10] applies the SVPWM technique in [2]. The output of the inverter is fed to the induction motor. The AC drive system is simulated in no load and full load conditions in order to see the THD. THD comes out to be 30%

without filter which is less than SPWM but still very high harmonic distortion [10].

## 2.2 Disadvantages of 2-level VSI

2-level voltage source inverters (VSI) has high distortion in output voltage therefore reducing the power quality. Three strategies are used to reduce the harmonics in the 2-level VSI.

- Increase the switching frequency.
- Include a filter.
- Increase the number of levels of inverters.

Switching frequency is the rate at which the switch turns on and off. In case of power electronic devices switches are IGBT, MOSFET, transistors or diodes. The increase in switching frequency causes the THD to reduce. Increasing the switching frequency causes more switching losses. The second strategy is to design and include a filter to reduce harmonics. A filter contains the circuitry which diverts the harmonics in the output of the inverter from their normal path. These filters are tuned in such a way that they let some harmonics at particular frequencies pass through and cuts off the harmonics at other frequencies. A low pass filter lets the harmonics at low frequencies pass through and cuts off the harmonics at high frequencies after cut off frequency. As the harmonics increase in the power system more than one filter is required which is costly. These filters generate unwanted resonance which involves other frequencies [3].

## 2.3 SVPWM for Multi-level Converters

Multilevel inverters are used in order to reduce the harmonics. There are various topologies of multilevel inverters: cascaded H-bridge converter [11], diode clamped

inverter (neutral clamped) [12], [13] and [14], capacitor clamped (flying capacitors) [15] and modular multilevel converter (MMC).

The authors of [16] discuss SVPWM technique for 3-level inverters. In [16] the space vector diagram of 3-level inverter which has an additional hexagon is first converted into the space vector diagram of 2-level inverter then the pulses are generated as discussed in [10].

The authors of [17] give the SVPWM technique for 3-level inverter. [17] locates the head of the reference vector in the triangle (region in a 60 degree sector) which is formed due to additional hexagon in space vector diagram. Once the region is known the duty cycles are calculated and pulses are generated according to the duty cycle.

The authors of [17] uses diode clamped multilevel converter which has some disadvantages discussed in [18].

- Increase in the number of diodes in multilevel inverters makes the system complex.
- The voltage across the capacitor cannot be maintained.
- Additional circuitry is required to balance the neutral point voltage in multilevel inverters.
- This inverter topology is not suited for HVDC applications.

The authors in [11] discuss the SVPWM technique for cascaded H-bridge inverters. However as the number of levels increases in this topology, more DC sources are required for supply which increases the complexity of the circuit for transformer connection [18]. Due to the operation of individual cell in single phase which has large number of capacitors this topology generates more ripples [18].

Modular multilevel converter (MMC) is very promising topology for high power applications due to its simplicity, reduction of power losses and filters. The fault currents in DC side are smaller [19] as the number of levels in the converter increases. The next section gives the gap analysis in the above discussed literature and a problem statement is formulated for SVPWM technique.

## 2.4 Gap Analysis

The problem with SVPWM technique is that when multilevel inverters are used the switching states in an inverter increases. In 2-level inverter there are eight switching states. So eight voltage vectors are formed which makes a hexgaon [2]. In 3-level inverter there is an additional hexagon and more triangles in the space vector diagram because of increased switching states. [16] and [20] give a SVPWM technique which gives the solution for 3-level inverter.

The head of the reference vector is detected by determining the triangle in the hexagon. 3-level space vector diagram is converted into 2-level space vector diagram and then the duty cycle of the pulses is calculated. The duty cycle is multiplied with the switching states. The switching states are pre-stored in the memory.

As the number of levels increase from three to four and onwards in an inverter, the switching states also increase forming an additional hexagon and additional triangles in the space vector diagram. The head of the reference vector in the space vector diagram becomes more and more difficult to detect and the switching states stored in the memory consume more and more time to execute.

The authors of [21] present a SVPWM technique for cascaded H bridge inverters. In this proposed technique the cascaded H bridge inverter is considered a set of 3-level inverter then the SVPWM technique for 3-level inverter is applied. The switching states are still stored in the memory.

[22] detects the location of the reference vector by determining the nearest three vectors. Nearest three vectors are determined by detecting the nested hexagon in 5-level space vector diagram. In [22] and [23] a table is given for determining the switching states and has two modes of operation but the implementation of this table is quite complex. In [23] a new table is given which gives the new duty cycles but these duty cycles still have to be multiplied with the switching states generated by the table given in [22]. Appropriate redundant switching states have to be selected for ascending and descending modes. Moreover [23] does not apply the SVPWM technique to an actual converter it puts the SVPWM algorithm in DSP

and the output is measured on DAC. It does not generate the gating signals so no method for generating the gating signals for the converter is given in [23]. Considering the limitations of the SVPWM technique, it is felt that a solution is required that makes the SVPWM technique easy and simple for multilevel converters.

## 2.5 Problem Statement

Considering the gaps in the SVPWM technique this study gives an improved and simplified method for the detection of the head of the rotating vector in n-level space vector diagram. This study also gives a simplified method to get the switching states which were previously stored in the memory or generated by complex algorithms as discussed in the previous section. Moreover this study applies the presented technique on 2-level VSI, 5-level MMC and 21-level MMC and gives the analysis based on total harmonic distortion and switching losses under load conditions. A technique for the calculation of switching losses is developed which calculates the losses during switching. SSVPWM technique is applied to MMC for their advantages over other topologies as discussed earlier.

## 2.6 Research Methodology

### 2.6.1 Software Tool

The software used to conduct this research on SVPWM technique is MATLAB. The SSVPWM algorithm is developed using MATLAB function block.
The model of 2-level VSI, 5-level MMC and 21-level MMC is designed in MATLAB/SIMULINK using Simscape Power Systems. Simscape Power Systems has the required blocks used in the modeling of converters.All the graphical work is done in Origin pro software.

# Chapter 3

# Improved Space Vector Modulation

This chapter presents the improved and simplified SVPWM for multilevel converters, method of generating the gating signals for the power electronic switches in converters and also gives a flowchart of the presented SVPWM algorithm.

## 3.1 Introduction To Space Vector Modulation

The diagram of the three-phase VSI is shown in Figure 3.1. There are three arms in three-phase VSI each arm contains two switches so the total number of switches is six in the three-phase inverter.

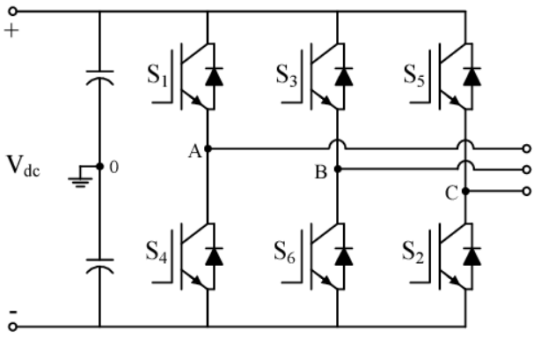



FIGURE 3.1: Three Phase 2-level VSI [2]

These six switches are controlled in a certain way to generate the output voltage. If the upper switch is on i.e 1 the lower switch in the arm should be off i.e 0. Depending upon the switching states three-phase VSI inverter generates eight different voltage vectors. If the upper switch in the arm of the three-phase VSI is on the switching function is defined as 1. If the lower switch in the arm of the three-phase VSI is on the switching function is defined as 0 as given in the Figure 3.2 [2].

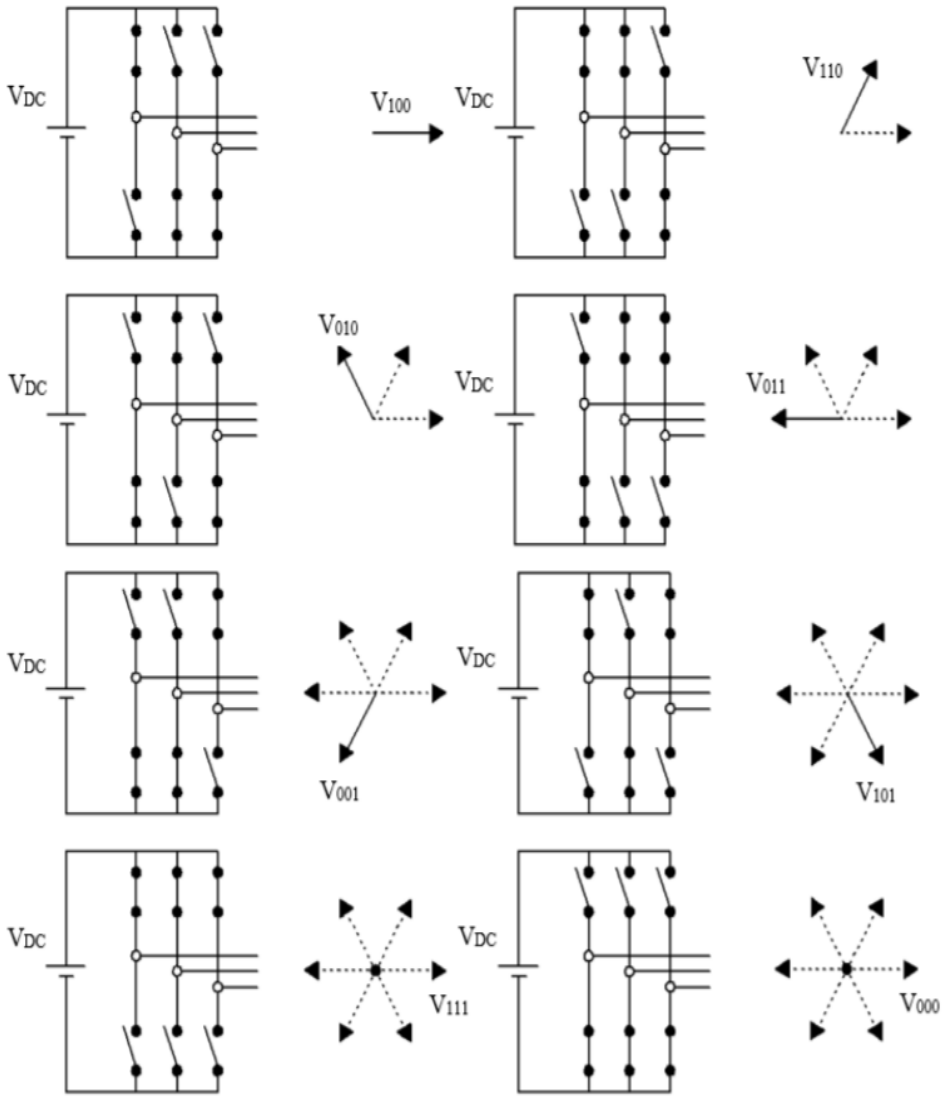



FIGURE 3.2: Three Phase VSI Voltage Vectors [2]

When the heads of these eight voltage vectors are joined together it forms a hexagon. This hexagon contains six sectors at 60 degrees. There are six active voltage vectors and two zero vectors and the switching states are written at

the head of the voltage vector as shown in the Figure 3.3.

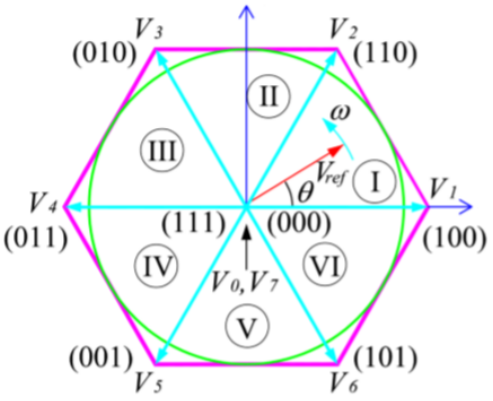



FIGURE 3.3: Space Vector Diagram of 2-level Inverter

When these switching states are executed for a time period a reference vector is formed inside the hexagon which rotates inside the hexagon to form the sinusoidal output. The reference vector rotates in a circular path as shown in the Figure 3.3. In order to implement the SVPWM technique the reference vector which is rotating inside the hexagon has to be first detected and then synthesized.

As the levels of inverter increases the switching states of the inverter also increases which generates an extra hexagon in the space vector diagram. For n-level inverter n-1 hexagons are generated where n is the number of levels in the inverter. Figure 3.4 shows the space vector diagram of 5-level inverter.

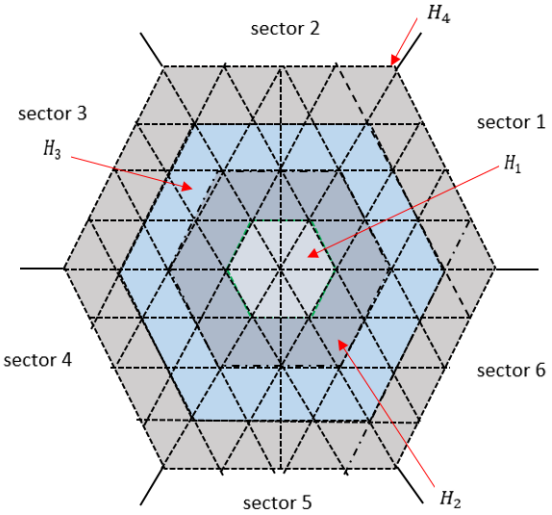



FIGURE 3.4: Space Vector Diagram of 5-level Inverter

The 5-level space vector hexagon contains several 2-level hexagons and the head of the reference vector is in one of the 2-level sub hexagon. Figure 3.5 shows three 2-level sub hexagons which are inside 5-level space vector hexagon and the rotation of the reference vector inside it.

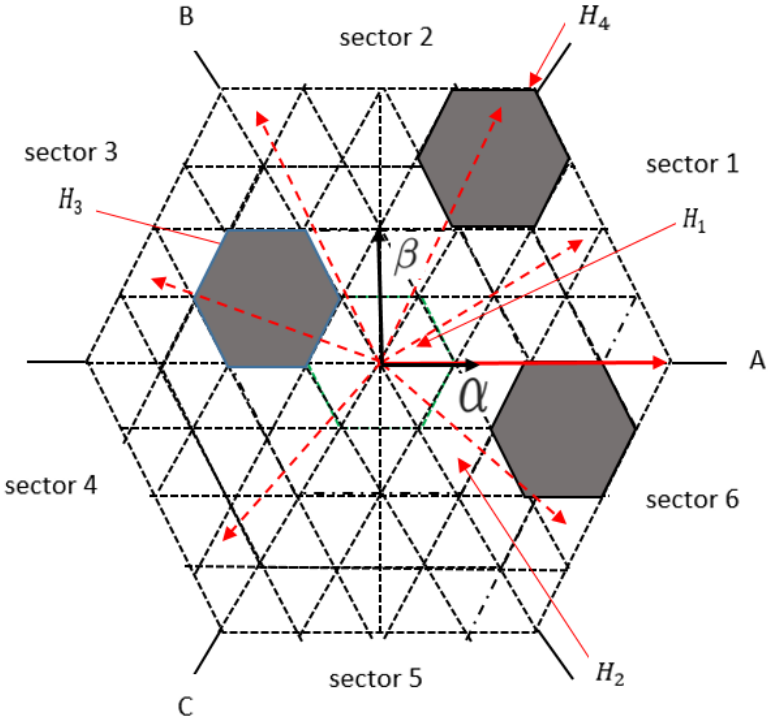



FIGURE 3.5: 2-level Sub Hexagon in 5-level Space Vector Diagram and Rotation of Reference Vector in 6 Sectors

The reference vector which is rotating in the 5-level space vector diagram as shown in the Figure 3.5 has to be synthesized. The location of the head of the reference vector has to be known to generate the required vector. Once its location is detected it always lies in a 2-level sub hexagon. After we detect the 2-level sub hexagon we find the switching states of that 2-level sub hexagon and execute them for the calculated duty cycles which gives us the required reference vector. The synthesized reference vector is then compared with the symmetrical triangular wave to get the gate drive signals for power electronic switches present in the converter Figure 3.10.

## 3.2 Simplified Space Vector Algorithm

The proposed SSVPWM algorithm is discussed for 5-level converter but this algorithm is for n-level converter. Where n is the number of levels of the converter.

### 3.2.1 Three Phase System

The reference vector for three-phase n level converter is generated by equation 3.1 from [23]. Where $V_a, V_b$ and $V_c$ represent the instantaneous voltage of phase a, b and c respectively. These three-phase voltages are 120 degrees apart from each other and n represents the number of levels of the converter. The location of the reference vector has to be known in the space vector diagram to generate the required reference vector.

$$V_{ref} = (n-1)(V_a + V_b.e^{\frac{j2\pi}{3}} + V_c.e^{\frac{j4\pi}{3}}) \tag{3.1}$$

### 3.2.2 Coordinate Transformation

The reference vector is rotating in 3-phase system which are 120 degrees apart from each other. It is hard to find the coordinates of the rotating vector in three phase system. We have to transform this 3-phase system into $\alpha$ and $\beta$ coordinate system to get the coordinates of the head of the reference vector in the 5-level space vector hexagon as shown in the Figure 3.6. The transformation is done by putting the value of equation 3.2 and 3.3 in equation 3.1 we get equation 3.4.

$$e^{\frac{j2\pi}{3}} = \cos(\frac{2\pi}{3}) + j\sin(\frac{2\pi}{3}) \tag{3.2}$$

$$e^{\frac{j4\pi}{3}} = \cos(\frac{4\pi}{3}) + j\sin(\frac{4\pi}{3}) \tag{3.3}$$

This gives real and imaginary components of the reference vector which is rotating inside 5-level hexagon as shown in equation 3.4

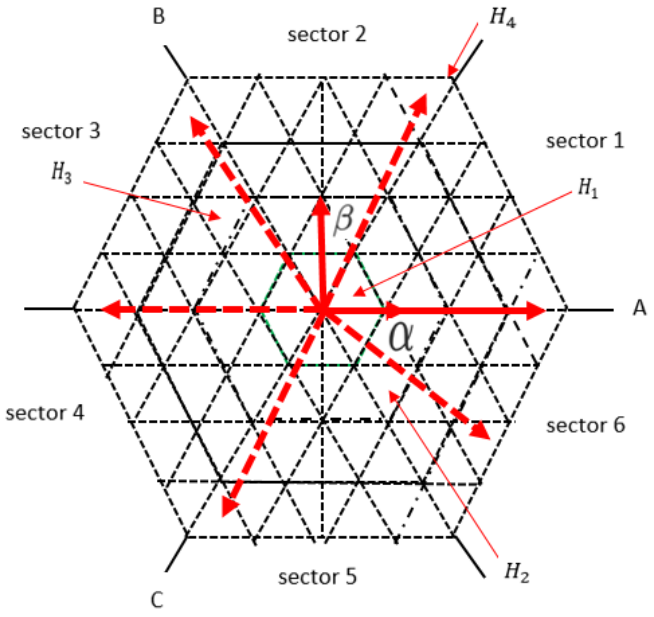



FIGURE 3.6: *abc* to $\alpha$-$\beta$ Transformation

$$V_{ref} = V_{ref(\alpha)} + jV_{ref(\beta)} \tag{3.4}$$

Now in equation 3.4 the reference vector which was rotating in abc coordinate system is now in $\alpha$-$\beta$ coordinate system as shown in the Figure 3.6. Where $V_{ref(\alpha)}$ and $V_{ref(\beta)}$ in equation 3.4 are the real and imaginary components of $V_{ref}$. As we have now converted the abc to $\alpha-\beta$ coordinate system we can find the coordinates of the head of the reference vector by equation 3.5 and 3.6.

$$\alpha = \frac{V_{ref(\alpha)}}{V_{dc}} \tag{3.5}$$

$$\beta = \frac{V_{ref(\beta)}}{V_{dc\sqrt{3}}} \tag{3.6}$$

In equation 3.5 and 3.6 $\alpha$ and $\beta$ are the two coordinates of the reference vector. Lets say we get the coordinates of the reference vector in triangle with vertex $T_1$, $T_2$ and $T_3$ as shown in Figure 3.7. The triangle where the reference vector is located is called the modulation triangle. In this case triangle with vertex $T_1$,

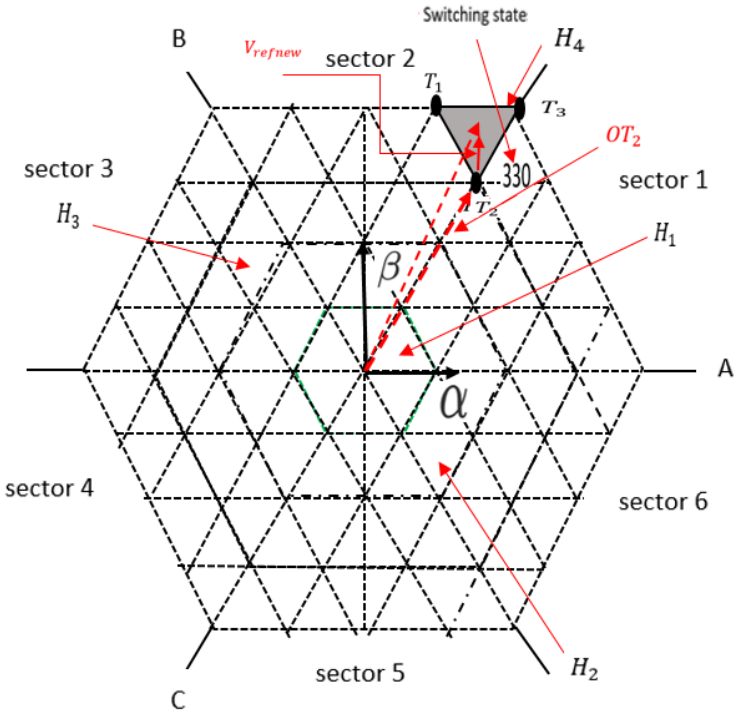



FIGURE 3.7: Location of The Reference Vector, Modulation Triangle and Vector $OT_2$

$T_2$ and $T_3$ is the modulation triangle. This modulation triangle is located in a 2-level sub hexagon. If we can find the switching state at the center of the 2-level sub hexagon i.e switching state at vertex $T_2$ we can convert 5-level space vector hexagon to 2-level hexagon. The switching states, duty cycle and the six regions in the 2-level sub hexagon can be found just like in 2-level space vector modulation technique.

The reference vector shown in the Figure 3.7 is made up of $\alpha$, $\beta$ and $-\beta$. The switching state at vertex $T_2$ can be found using equation 3.7 from [23].

$$\begin{bmatrix} S_{Wa} \\ S_{Wb} \\ S_{Wc} \end{bmatrix} = int \left( \begin{bmatrix} \alpha - min(\alpha, \beta, -\beta) \\ \beta - min(\alpha, \beta, -\beta) \\ -\beta - min(\alpha, \beta, -\beta) \end{bmatrix} \right) \tag{3.7}$$

In equation 3.7 $S_{Wa}$, $S_{Wb}$ and $S_{Wc}$ are the three switching states at the vertex $T_2$. Once we have found the switching states at the vertex $T_2$ we can get the vector centered at the origin. The value obtained from equation 3.7 from [23] is fed into

equation 3.8 from [23] to get the vector $OT_2$ as shown in Figure 3.7.

$$V_{ref} = V_{dc}.(S_{Wa} + S_{Wb}.e^{\frac{j2\pi}{3}} + S_{Wc}.e^{\frac{j4\pi}{3}}) \tag{3.8}$$

Now if we subtract the reference vector given in equation 3.1 and vector $OT_2$ a new reference vector is formed which is inside the 2-level sub hexagon centered at vertex $T_2$ given in Figure 3.7. $V_{refnew}$ is given in equation 3.9 from [23].

$$V_{refnew} = V_{ref} - OT_2 \tag{3.9}$$

By using equation 3.9 from [23] has created a scenario of 2-level SVPWM technique now the duty cycle and the six regions can be obtained just like 2-level SVPWM technique.

### 3.2.3 Duty Cycle and Region Calculation

The region of the $V_{refnew}$ 1 to 6 can be calculated like a 2-level SVPWM technique. $V_{n\alpha}$ and $V_{n\beta}$ are real and imaginary components of $V_{refnew}/V_{dc}$. We can find the angle $\theta_{new}$ by equation 3.10.

$$\theta_{new} = \tan^{-1}(\frac{V_{n\beta}}{V_{n\alpha}}) \tag{3.10}$$

In equation 3.10 $\theta$ is $(0 \leq \theta_{new} \leq 2\pi)$ and region can be found using equation 3.11. There are six regions of 60 degrees.

$$reg = \begin{cases} 1 & \text{if } \theta_{new} > 0 \;\&\&\; \theta_{new} \leq \pi/3 \\ 2 & \text{if } \theta_{new} > \pi/3 \;\&\&\; \theta_{new} \leq 2\pi/3 \\ 3 & \text{if } \theta_{new} > 2\pi/3 \;\&\&\; \theta_{new} \leq 3\pi/3 \\ 4 & \text{if } \theta_{new} > 3\pi/3 \;\&\&\; \theta_{new} \leq 4\pi/3 \\ 5 & \text{if } \theta_{new} > 4\pi/3 \;\&\&\; \theta_{new} \leq 5\pi/3 \\ 6 & \text{if } \theta_{new} > 5\pi/3 \;\&\&\; \theta_{new} \leq 2\pi \end{cases} \tag{3.11}$$

After the region is detected the duty cycle can be calculated from equation 3.12 from [23].

$$\begin{cases} d_1 = \frac{2}{\sqrt{3}}[V_{n\alpha}\sin(\frac{reg}{3}\pi) - V_{n\beta}\cos(\frac{reg}{3}\pi)] \\ d_2 = \frac{-2}{\sqrt{3}}[V_{n\alpha}\sin(\frac{reg-1}{3}\pi) - V_{n\beta}\cos(\frac{reg-1}{3}\pi)] \\ d_0 = 1 - d_1 - d_2 \end{cases} \tag{3.12}$$

In equation 3.12 from [23] $d_1$ and $d_2$ are the duty cycle of two active vectors and $d_0$ is the total duty cycle of two zero vectors.

### 3.2.4 Switching States

In [22] a table is given for determining the switching states which has two modes of operation but the implementation of this table is quite complex. In [23] a new table is given which gives the new duty cycles but these duty cycles still has to multiply with the switching states generated by the table given in [22]. Appropriate redundant switching state has to be selected for ascending and descending modes. This study presents a simple way to determine the switching states, equation 3.9 shows the new reference vector $V_{refnew}$ which is inside a 2-level sub hexagon centered at vertex $T_2$, 5-level space vector hexagon is converted in 2-level hexagon centered at vertex $T_2$ whose state has already been found using equation 3.7. The remaining switching states are found by adding the switching state detected at vertex $T_2$ with the switching states of 2-level converter. For example the switching states for two level converter for reg 2 are 000 →110 → 010 → 111. The required switching states for phase a, b and c of the 2-level sub hexagon can be found by

For Phase A

$S_{wa} + 0 \rightarrow S_{wa} + 1 \rightarrow S_{wa} + 0 \rightarrow S_{wa} + 1.$

For Phase B

$S_{wb} + 0 \rightarrow S_{wb} + 1 \rightarrow S_{wb} + 1 \rightarrow S_{wb} + 1.$

For Phase C

$S_{wc} + 0 \rightarrow S_{wc} + 0 \rightarrow S_{wc} + 0 \rightarrow S_{wc} + 1.$

These are the switching states generated for reg 2 of 2-level sub-hexagon. Similarly we can generate the switching states for all 6 regions as shown in the Figure

3.8 and Table 3.1. These switching states have to multiply with the duty cycles generated by equation 3.12 to get the required reference vector.

TABLE 3.1: Method of Generating The Switching States For All Regions

| **Region** | **Phase** | **Generation of switching states** |
|---|---|---|
| 1 | A | $S_{wa}+0 \rightarrow S_{wa}+1 \rightarrow S_{wa}+1 \rightarrow S_{wa}+1$ |
| | B | $S_{wb}+0 \rightarrow S_{wb}+0 \rightarrow S_{wb}+1 \rightarrow S_{wb}+1$ |
| | C | $S_{wc}+0 \rightarrow S_{wc}+0 \rightarrow S_{wc}+0 \rightarrow S_{wc}+1$ |
| 2 | A | $S_{wa}+0 \rightarrow S_{wa}+1 \rightarrow S_{wa}+0 \rightarrow S_{wa}+1$ |
| | B | $S_{wb}+0 \rightarrow S_{wb}+1 \rightarrow S_{wb}+1 \rightarrow S_{wb}+1$ |
| | C | $S_{wc}+0 \rightarrow S_{wc}+0 \rightarrow S_{wc}+0 \rightarrow S_{wc}+1$ |
| 3 | A | $S_{wa}+0 \rightarrow S_{wa}+0 \rightarrow S_{wa}+0 \rightarrow S_{wa}+1$ |
| | B | $S_{wb}+0 \rightarrow S_{wb}+1 \rightarrow S_{wb}+1 \rightarrow S_{wb}+1$ |
| | C | $S_{wc}+0 \rightarrow S_{wc}+0 \rightarrow S_{wc}+1 \rightarrow S_{wc}+1$ |
| 4 | A | $S_{wa}+0 \rightarrow S_{wa}+0 \rightarrow S_{wa}+0 \rightarrow S_{wa}+1$ |
| | B | $S_{wb}+0 \rightarrow S_{wb}+1 \rightarrow S_{wb}+0 \rightarrow S_{wb}+1$ |
| | C | $S_{wc}+0 \rightarrow S_{wc}+1 \rightarrow S_{wc}+1 \rightarrow S_{wc}+1$ |
| 5 | A | $S_{wa}+0 \rightarrow S_{wa}+0 \rightarrow S_{wa}+1 \rightarrow S_{wa}+1$ |
| | B | $S_{wb}+0 \rightarrow S_{wb}+0 \rightarrow S_{wb}+0 \rightarrow S_{wb}+1$ |
| | C | $S_{wc}+0 \rightarrow S_{wc}+1 \rightarrow S_{wc}+1 \rightarrow S_{wc}+1$ |
| 6 | A | $S_{wa}+0 \rightarrow S_{wa}+1 \rightarrow S_{wa}+1 \rightarrow S_{wa}+1$ |
| | B | $S_{wb}+0 \rightarrow S_{wb}+0 \rightarrow S_{wb}+0 \rightarrow S_{wb}+1$ |
| | C | $S_{wc}+0 \rightarrow S_{wc}+1 \rightarrow S_{wc}+0 \rightarrow S_{wc}+1$ |

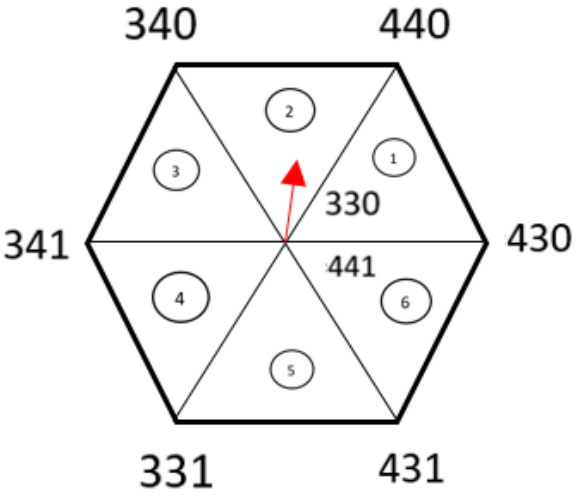



FIGURE 3.8: 2-level Sub Hexagon Containing All Regions and Switching States

For example if $V_{refnew}$ is detected in region 2 the equations to synthesize the reference vector for phase a, b and c is given as. The reference vector is shown in Figure 3.9.

$$V_{an} = [d_0 * (S_{Wa} + 0) + d_1 * (S_{Wa} + 1) + d_2 * (S_{Wa} + 0) + d_0 * (S_{Wa} + 1)]/n - 1 \tag{3.13}$$

$$V_{bn} = [d_0 * (S_{Wb} + 0) + d_1 * (S_{Wb} + 1) + d_2 * (S_{Wb} + 1) + d_0 * (S_{Wb} + 1)]/n - 1 \tag{3.14}$$

$$V_{cn} = [d_0 * (S_{Wc} + 0) + d_1 * (S_{Wc} + 0) + d_2 * (S_{Wc} + 0) + d_0 * (S_{Wc} + 1)]/n - 1 \tag{3.15}$$

It should be noted that the duty cycle of the two zero switching states (330) and (441) are equal which is not in the case of SPWM. This equal distribution of the switching states in the synthesized reference vector causes less switching losses in the SVPWM technique.

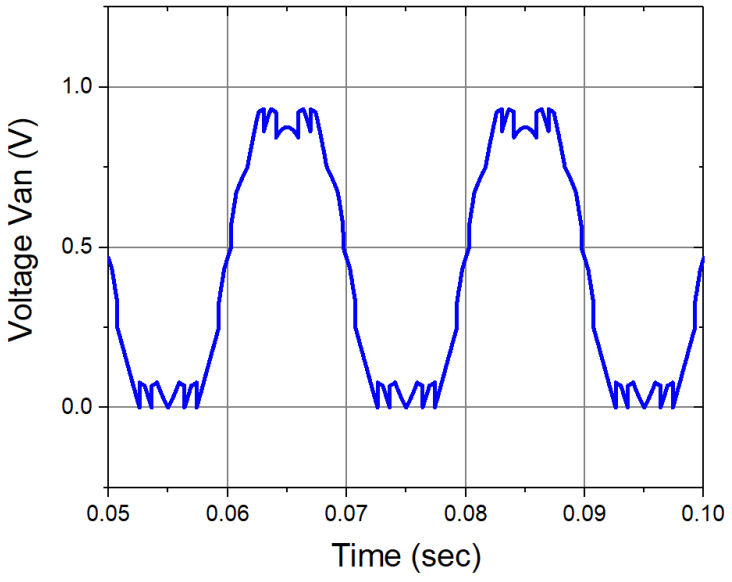



FIGURE 3.9: Synthesized Reference Vector for 5-level Converter, Represents Phase Voltage of 5-level Converter

### 3.2.5 Gate Signal Generation

Gating signals for power electronic switch in the converter is generated by comparing the reference vector generated in the previous section with the symmetric triangular wave as shown in the Figure 3.10. Where $T_s$ is the sampling period. In Figure 3.10 $V_{an}$, $V_{bn}$ and $V_{cn}$ are the reference vector which is synthesized in the previous section. This reference vector represents the phase voltage. These reference vectors are compared with the symmetric triangular wave. When the amplitude of the reference vector is less than that of the triangular wave the gate pulse will be high and when the amplitude of the reference vector is greater than that of triangular wave the gate pulse will be low during a sampling period $T_s$.

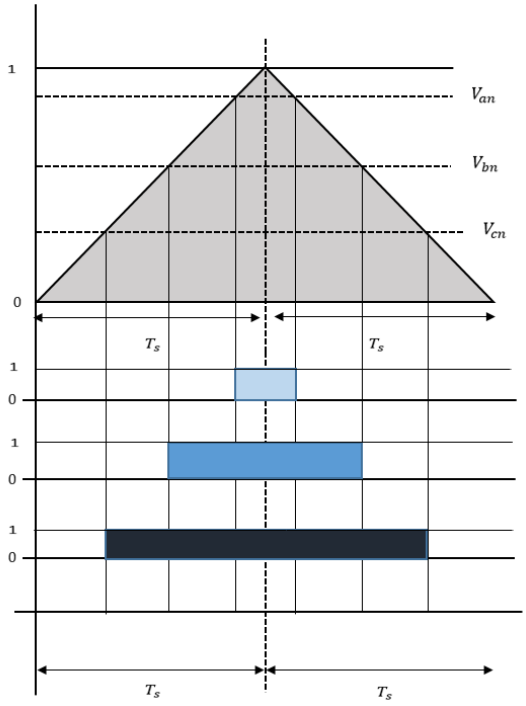



FIGURE 3.10: Method of Generation of Gate Pulses By Comparing Reference Phase Voltages With Symmetrical Triangular Wave

## 3.3 Flow Chart of The Algorithm

The presented SSVPWM algorithm is divided into following steps.The flow chart of the presented SSVPWM technique is given in Figure 3.11.

- First the ABC coordinate system is converted into $\alpha - \beta$ coordinate system. By the conversion of coordinate system we can get the coordinates of the head of the rotating vector.
- The coordinates of the rotating vector can be found by equation 3.5 and 3.6. By these coordinates we can find the location of the head of the rotating vector in space.
- Once the location of the head of the rotating vector is known it always lies in a 2-level sub hexagon inside the 5-level hexagon. We can convert 5-level hexagon into 2-level sub hexagon by equation 3.9.
- There are six regions inside 2-level sub hexagon which can be found using equation 3.11 and the duty cycles can be found using equation 3.12.
- Once the region and the duty cycles are found all the required switching states are generated which are then executed for the duty cycle and region calculated from equation 3.11 and 3.12 to get the required reference vector.
- Gating signals for power electronic switches are generated by comparing the generated reference vector with the symmetric triangular wave.

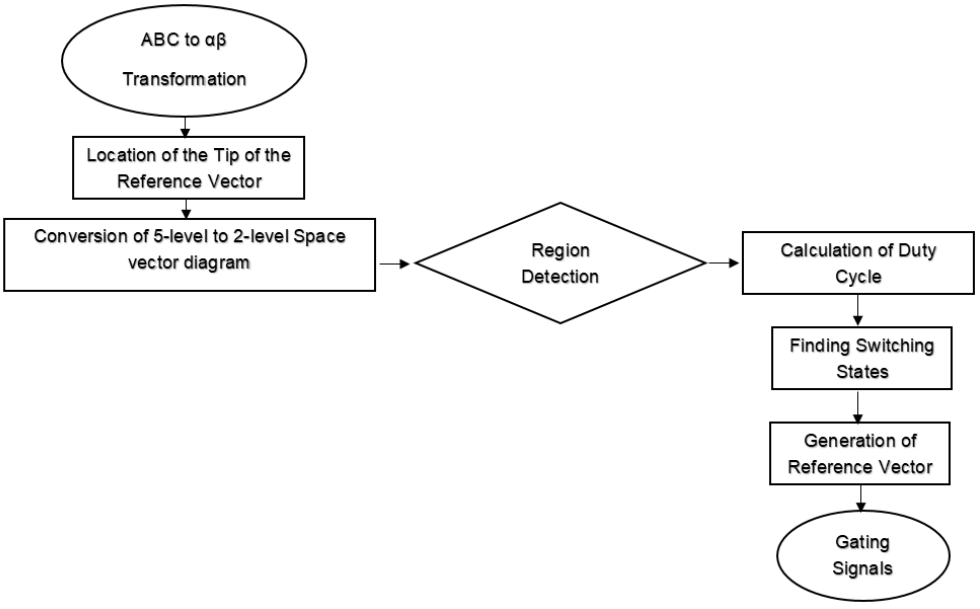



FIGURE 3.11: Flow Chart of The Presented SSVPWM Algorithm

# Chapter 4

# Modular Multilevel Converter

This chapter discusses the advantages of modular multilevel converters, its sub module topologies and basic states of operation of MMC. It also gives the mathematical and simulink modeling of MMC.

## 4.1 Introduction

Previously high voltage direct transmission (HVDC) was achieved with the help of thyristor controlled line commutated converter (LCC) which has certain disadvantages. LCC uses semiconductor devices which uses external voltage for switching, delay power factor and can not be used in a passive system [19].
More recently voltage source converters (VSC) were used which has insulated gate bipolar transistors. The advantage of VSC over LCC is that it uses semiconductor devices which can switch on and off while carrying current. VSC can be used in isolated systems. The disadvantages of VSC are as follows [19].

- With pulse width modulation VSC causes high harmonic content in the output voltage.
- Passive filters are required to remove the harmonic content which are very costly.

- High switching frequency to remove harmonic content in VSC has more power losses.
- DC short circuits are very difficult to limit.

Due to these disadvantages multilevel VSC were used which have their own limitations. Modular multilevel converters (MMC) were introduced by Lesnicar and R. Marquardt as shown in the Figure 4.1. MMC has following advantages [19]. MMC has $N-1$ SMs, 5-level MMC has 4 SMs in an arm as shown in Figure 4.1.

- Complexity does not increase as the number of level increses.
- Reduction of power losses due to low switching frequency.
- Reduction in filtering needs.
- The capacity is distributed among SMs.

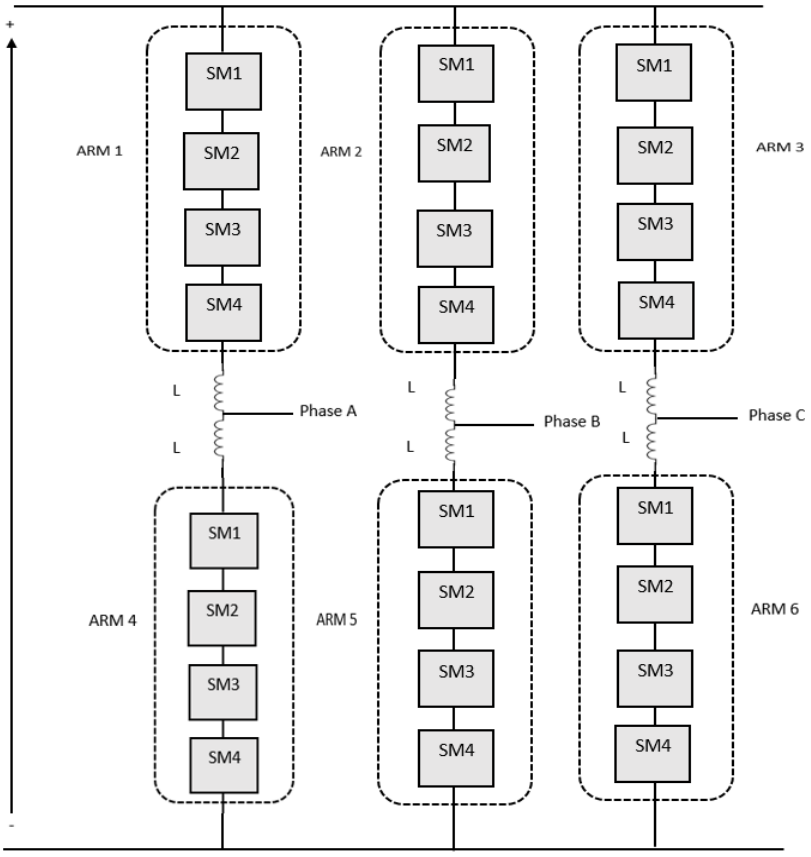



FIGURE 4.1: 5-level Modular Multilevel Converter (MMC)

## 4.2 MMC Sub Module Topologies

### 4.2.1 Half Bridge Topology

The SM has two IGBTs, two antiparallel diodes and a capacitor in half bridge topolgy. The circuit diagram of a half bridge MMC topology is given in the Figure 4.2.

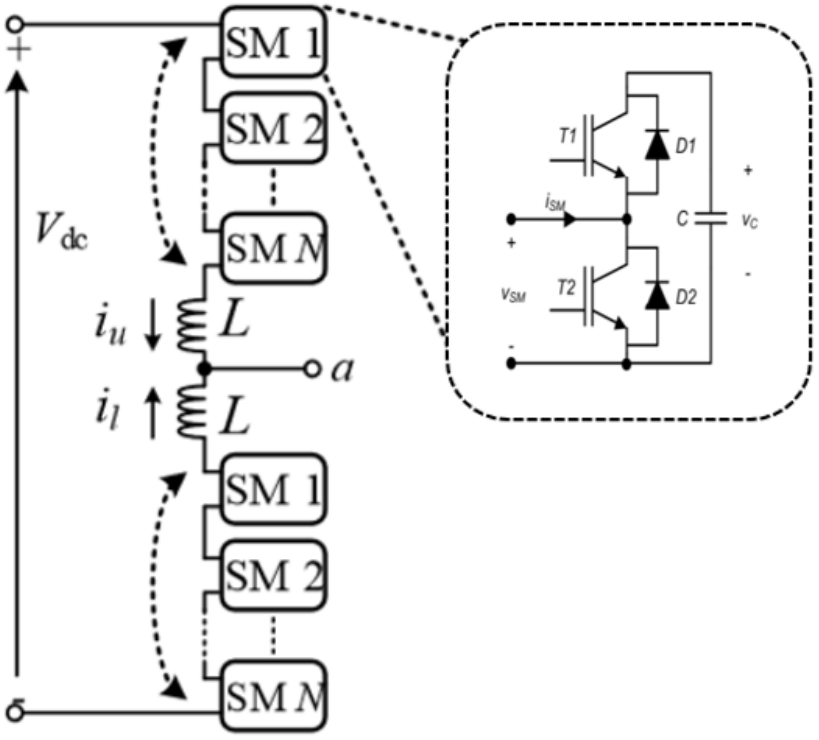
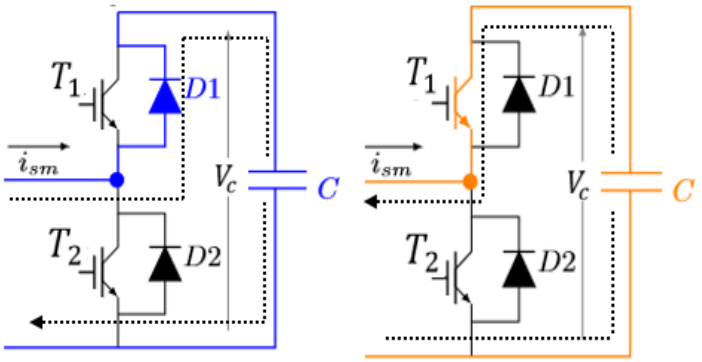


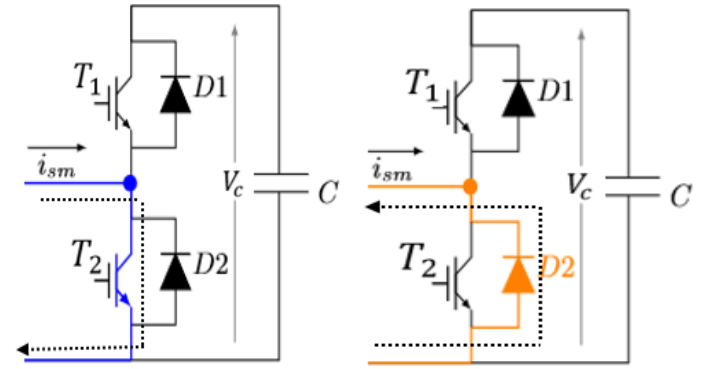

FIGURE 4.2: Half Bridge Topology of Sub Module in MMC

When $T_1$ is ON and $T_2$ is OFF the SM is in ON state. When the SM is ON the $V_{sm}$ is equal to $V_c$. When $T_2$ is ON and $T_1$ is OFF the SM is OFF and the voltage will appear on the output. When the SM is ON the current passes through the capacitor. If the current is in positive direction the capacitor charges and if the current is in the negative direction the capacitor discharges. When both $T_1$ and $T_2$ are ON short circuit occurs [19]. When diode $D_1$ is conducting the current $i_{sm}$ is in positive direction and when $D_2$ is conducting the current $i_{sm}$ will be in negative direction as shown in Figure 4.3.




(a) Sub Module ON Current Is In Positive Direction

(b) Sub Module ON Current Is In Negative Direction




(c) Sub Module OFF Current Is In Positive Direction

(d) Sub Module OFF Current Is In Negative Direction

FIGURE 4.3: Operation of Sub Module and The Direction of Current [24]

### 4.2.2 Full Bridge Topology

There are four IGBTs, four diodes and a capacitor in full bridge topology of a SM. The circuit diagram of the full bridge topology is given in the Figure 4.4. In full bridge topolgy the SM is ON ($V_{SM} = V_c$) when $T_1$ and $T_4$ are ON. The SM is OFF ($V_{SM} = 0$) if $T_1$ and $T_2$ are ON or IGBT $T_3$ and $T_4$ are ON. When $T_2$ and $T_3$ are ON $V_{sm}$ will be equal to $V_c$. When ($V_{SM} = V_c$) depending on the direction of the current the capacitor will charge and discharge if the direction of the current is positive the capacitor will charge and if the current is in negative direction the capacitor will discharge. The full bridge topology has more IGBTs as compared to the half bridge SM topology which causes more losses during switching [24].

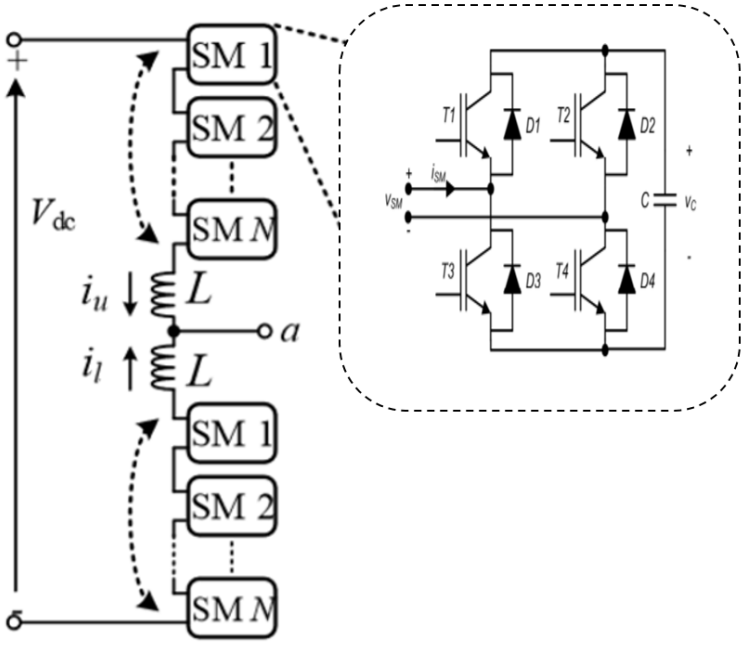



FIGURE 4.4: Full Bridge Topology of a Sub Module In MMC

### 4.2.3 Operation of Modular Multilevel Converter

Sub modules are connected in series, each SM is made up of either half bridge or full bridge topology. Half bridge topology is mostly used. There are N-1 number of sub modules connected in series which makes an arm. A phase leg consists of two arms, upper arm and lower arm as shown in the Figure 4.1. Voltage across the capacitor in a sub module is.

$$V_c = \frac{V_{dc}}{n} \tag{4.1}$$

If the arm contains 4 sub modules the number of levels of the output phase voltage will be 5 and the states of operation of MMC are shown in Table 4.1 [19]. In 5-level MMC there are total 8 sub modules in a leg as shown in the Figure 4.1. The voltage levels for 5-level MMC which are generated when all the states are executed is given in the Figure 4.5.

There are 5 states for 5-level converter which are shown in Table 4.1. These states are executed with the help of PWM techniques to get the phase voltage V which is shown in Figure 4.5.

V has 5 levels which represents the output of 5-level converter. nup and nlow represents the SMs in upper and lower arm respectively.

TABLE 4.1: Operation of MMC During Different States

| **States** | **nup** | **nlow** | **V** |
|---|---|---|---|
| 1 | 4 | 0 | $\frac{-V_{dc}}{2} + \frac{0V_{dc}}{4}$ |
| 2 | 3 | 1 | $\frac{-V_{dc}}{2} + \frac{1V_{dc}}{4}$ |
| 3 | 2 | 2 | $\frac{-V_{dc}}{2} + \frac{2V_{dc}}{4}$ |
| 4 | 1 | 3 | $\frac{-V_{dc}}{2} + \frac{3V_{dc}}{4}$ |
| 5 | 0 | 4 | $\frac{-V_{dc}}{2} + \frac{4V_{dc}}{4}$ |

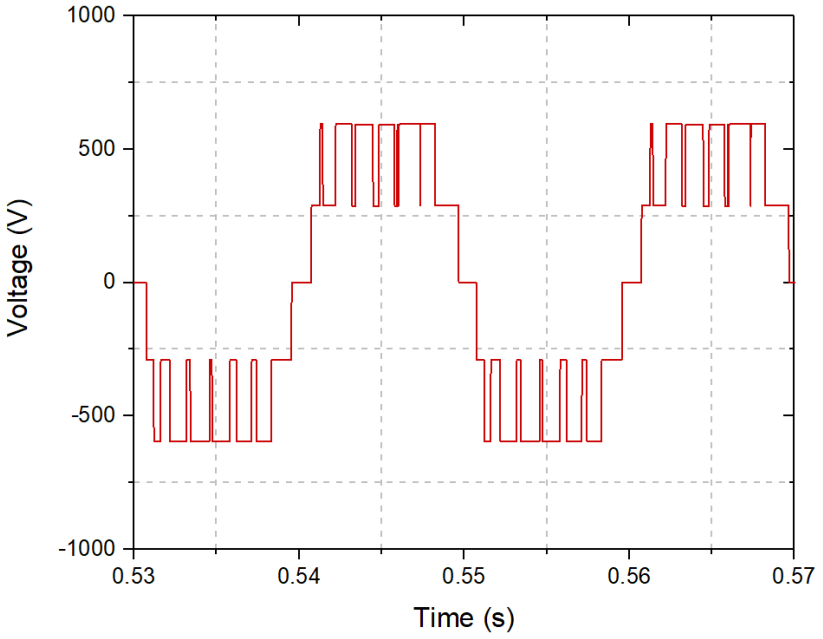



FIGURE 4.5: Voltage Levels for 5-level MMC Which are Generated When All The States Are Executed

State 1

When 4 SMs in the upper arm of the MMC are ON and no SMs in the lower arm of the MMC are ON.

State 2

When 3 SMs in the upper arm of the MMC are ON and 1 SM in the lower arm of the MMC is ON.

State 3

When 2 SMs in the upper arm of the MMC are ON and 2 SMs in the lower arm of the MMC are ON.

State 4

When 1 SM in the upper arm of the MMC is ON and 3 SMs in the lower arm of the MMC are ON.

State 5

When no SMs in the upper arm of the MMC are ON and 4 SMs in the lower arm of the MMC are ON.

## 4.3 Mathematical Modeling of MMC Arm Voltages and Currents

The equivalent circuit diagram of MMC is shown in the Figure 4.6. The $V_{dc}$ is separated into $+V_{dc}/2$ and $-V_{dc}/2$. The input voltage is measured from point "0".

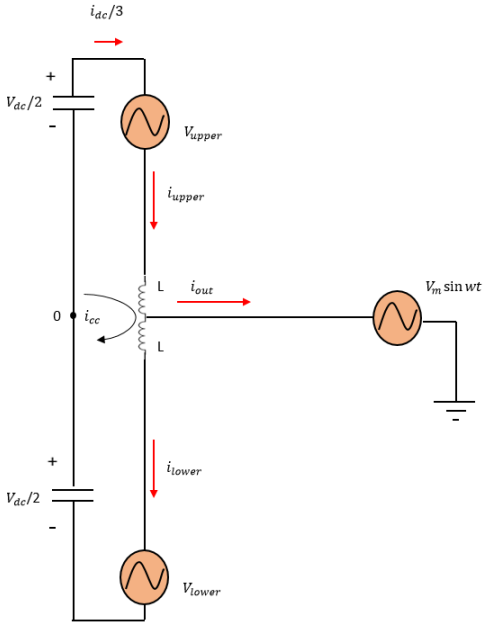



FIGURE 4.6: Equivalent Circuit Diagram of a Single Phase of Modular Multilevel Converter

All the SMs consist of half bridge inverter. So all these SMs are replaced with a

controllable voltage source.

L represent the arm inductance, $i_{upper}$ and $i_{lower}$ represents the current flowing in the upper and lower arms respectively. $i_{cc}$ is the circulating current. Applying Kirchoff's current law (KCL) to find the total current $i_{out}$.

$$i_{out} = i_{upper} - i_{lower} \tag{4.2}$$

The arm currents are given by equation 4.3 and 4.4 from [25].

$$i_{upper} = \frac{i_{dc}}{3} + i_{cc} + \frac{i_{out}}{2} \tag{4.3}$$

$$i_{lower} = \frac{i_{dc}}{3} + i_{cc} - \frac{i_{out}}{2} \tag{4.4}$$

$V_{upper}$ and $V_{lower}$ can be found by applying the Kirchoff's voltage law to upper and lower arm respectively.

$$\frac{V_{dc}}{2} - V_{upper} - L\frac{di}{dt} = V_m \sin(wt) \tag{4.5}$$

Inductor value is very small so we can ignore the inductor drop.

$$V_{upper} = \frac{V_{dc}}{2} - V_m \sin(wt) \tag{4.6}$$

Similarly we can find $V_{lower}$ by equation 4.7.

$$V_{lower} = \frac{V_{dc}}{2} + V_m \sin(wt) \tag{4.7}$$

## 4.4 Simulink Modeling of 5-level MMC

The presented SSVPWM technique is programmed in MATLAB function block. SSVPWM is applied to 5-level MMC. The Simulink model for SSVPWM based 5-level MMC is given in Figure 4.7. In this section modeling of 5-level MMC block

in Figure 4.7 is discussed. $V_{dc}$ is separated into $+\frac{V_{dc}}{2}$ and $-\frac{V_{dc}}{2}$. It is applied to 5-level MMC block. Inside 5-level MMC block a three phase 5-level MMC is implemented as shown in Figure 4.8.

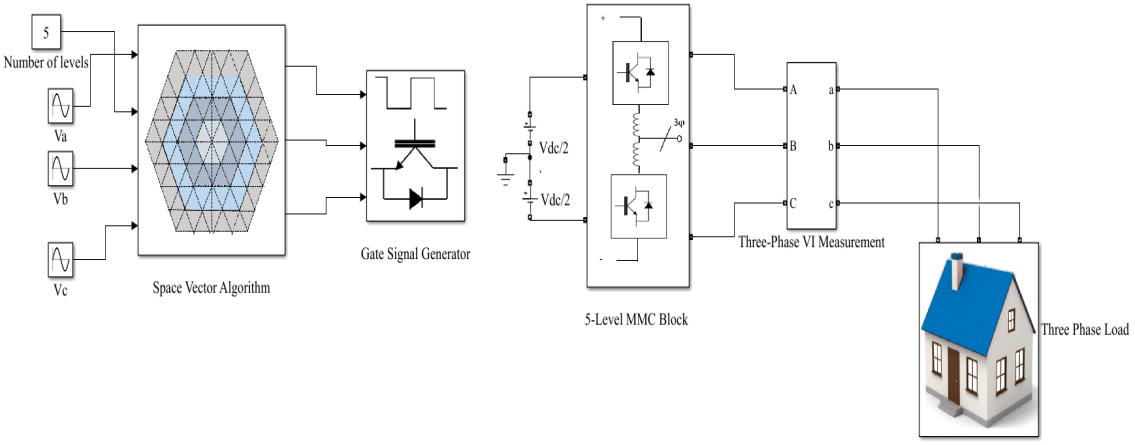



FIGURE 4.7: Simulink Model for SSVPWM Based 5-level MMC

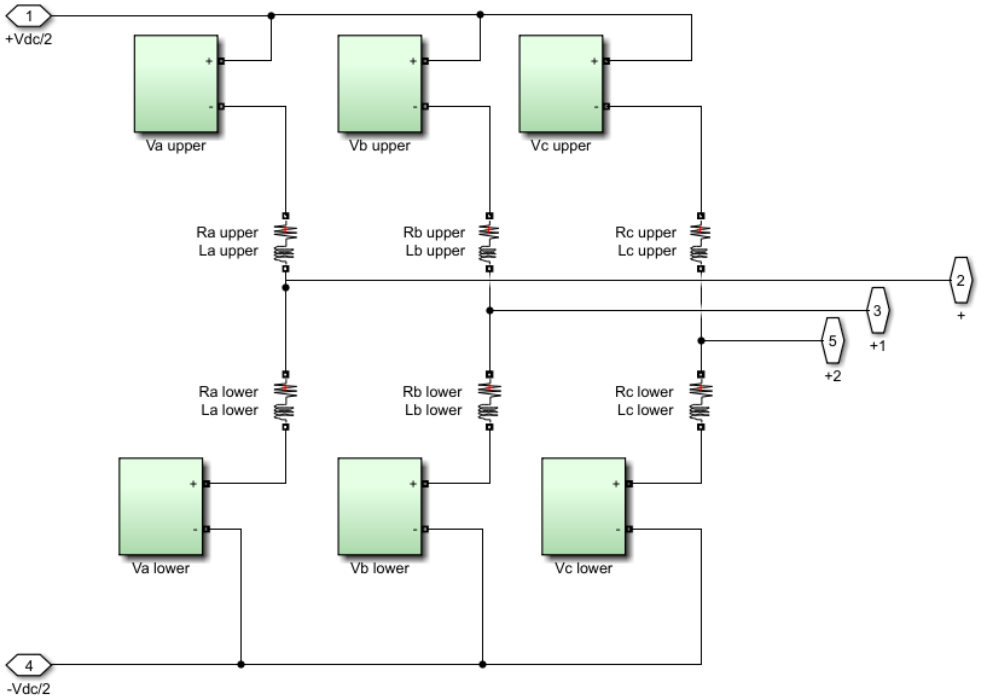



FIGURE 4.8: Simulink Model for Three Phase 5-level MMC

Figure 4.8 shows the simulink model for three phase 5-level MMC. There are three legs, one leg for each phase a,b and c. Each leg contains two arms upper arm and

lower arm. $V_iupper$ and $V_ilower$ where $i$ represents the three phases a,b and c. The model parameters are shown in the Table 4.2.

TABLE 4.2: Simulation Parameters of 5-level MMC

| **Parameter** | **Symbol** | **Value** |
|---|---|---|
| Input Voltage | $V_{dc}$ | 1200 V |
| Fundamental Frequency | $f$ | 50 Hz |
| Switching Frequency | $f_{sw}$ | 1500 Hz |
| Modulation Index | m | 0.9 |
| Load | $L_0$ | 1600 W |
| Arm Inductance | $L_{arm}$ | 0.03 H |
| Arm Resistance | $R_{arm}$ | 1 ohm |
| Number of SMs in an arm | N | 4 |
| Levels in Output Voltage | N+1 | 5 |

$V_iupper$ and $V_ilower$ block contains series connected sub modules here i represents the three phases a,b and c. Since this is a 5-level MMC so the number of SMs connected in series in an arm are 4 as shown in the Figure 4.9.

Input DC voltage of the converter is 1200 V. Switching frequency is the rate at which switch turns on and off. Switching frequency is 1500 Hz.

1.6 kW load is connected to the converter. Arm inductance and resistance are kept 0.03 H and 1 ohm respectively.

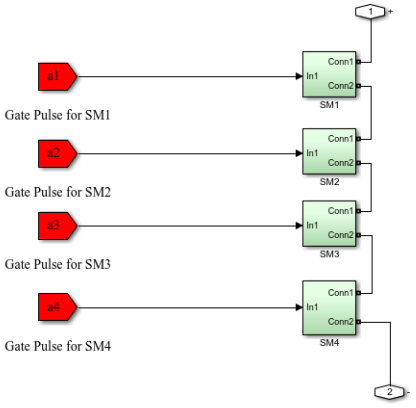



FIGURE 4.9: Simulink Model for One Arm of 5-level MMC

Each SM in the arm contains a half bridge topology which has two IGBTs $T_1$, $T_2$ and a capacitor as shown in Figure 4.10.

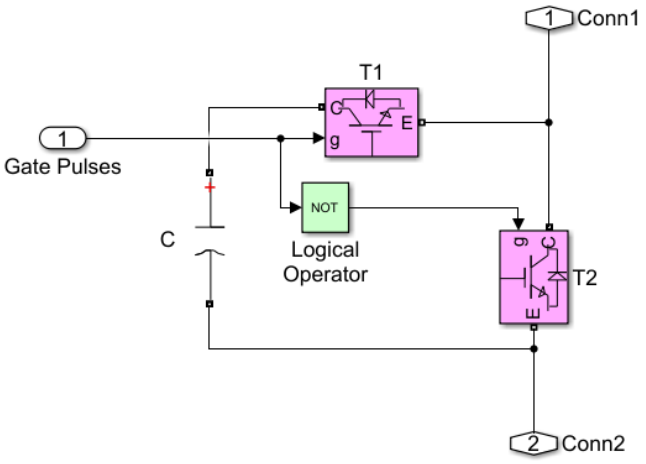



FIGURE 4.10: Simulink Model for Half Bridge Topolgy Inside SM

The gate pulses are given to the SM in such a way that when the gate pulse which is applied on IGBT $T_1$ is high, the gate pulse applied on the IGBT $T_2$ should be low. When the gate pulse which is applied on IGBT $T_1$ is low, the gate pulse applied on the IGBT $T_2$ should be high. This is achieved by using the logical operator NOT in the SM.

# Chapter 5

# Simulation and Results

This chapter contains MATLAB/SIMULINK model of 2-level VSI, 5-level MMC and 21-level MMC and their output line voltages. It also discusses the results of harmonic distortion and switching losses between SPWM and SSVPWM technique. Both SPWM and SSVPWM techniques are compared and analyzed on the basis of THD and switching losses. A switching loss algorithm is implemented in MATLAB/SIMULINK and it is applied to 2-level VSI and 5-level MMC.

## 5.1 Matlab/Simulink Model for SSVPWM Based 2-level VSI

The SSVPWM and SPWM techniques are applied to 2-level VSI, 5-level MMC and 21-level MMC. MATLAB/SIMULINK model for SSVPWM based 2-level VSI is given in Figure 5.1.

The 2-level VSI model has the DC voltage of 400V, fundamental frequency of 50Hz. Switching frequency and modulation index is kept 1500Hz and 0.9 respectively. The load which is connected to the 2-level VSI is 50W.

The parameters of the 2-level VSI model is summarized in the Table 5.1. The line voltages of the 2-level VSI using SSVPWM technique and SPWM is given in the Figure 5.2 and Figure 5.3.

TABLE 5.1: Simulation Parameters of 2-level VSI

| **Parameter** | **Symbol** | **Value** |
|---|---|---|
| Input Voltage | $V_{dc}$ | 400 V |
| Fundamental Frequency | $f$ | 50 Hz |
| Switching Frequency | $f_{sw}$ | 1500 Hz |
| Modulation Index | m | 0.9 |
| Load | $L_0$ | 50 W |

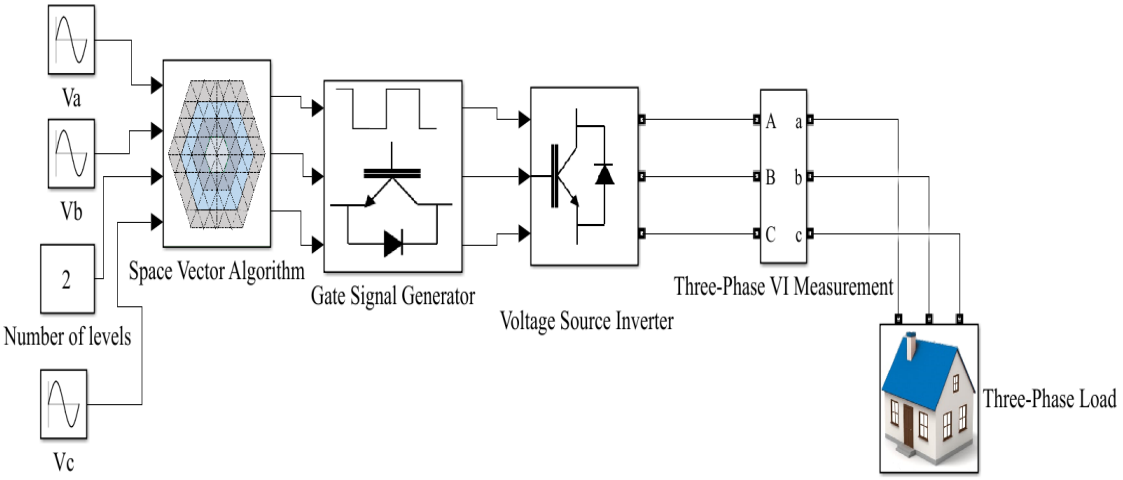



FIGURE 5.1: MATLAB/SIMULINK Model for 2-level SSVPWM Based VSI

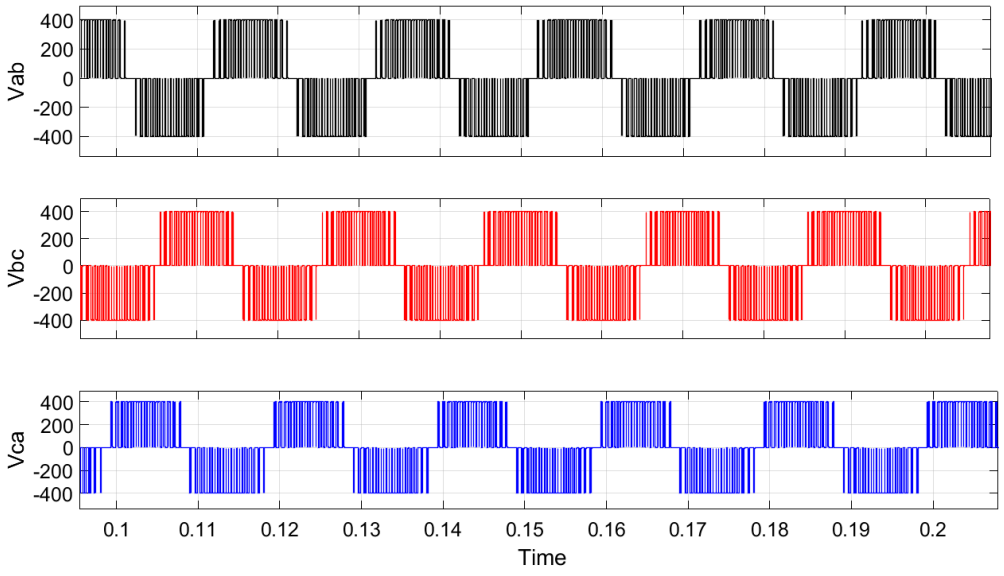



FIGURE 5.2: Line Voltages of 2-level VSI Using SSVPWM

Figure 5.2 shows the line voltages $V_{ab}$, $V_{bc}$ and $V_{ca}$ of the 2-level VSI. The line voltage is measured between two lines. $V_{ab}$ is measured between lines a and b, Similarly $V_{bc}$ is measured between lines b and c. Line voltage $V_{ca}$ is measured between line c and a. Figure 5.3 shows line voltages of 2-level VSI using SPWM technique.

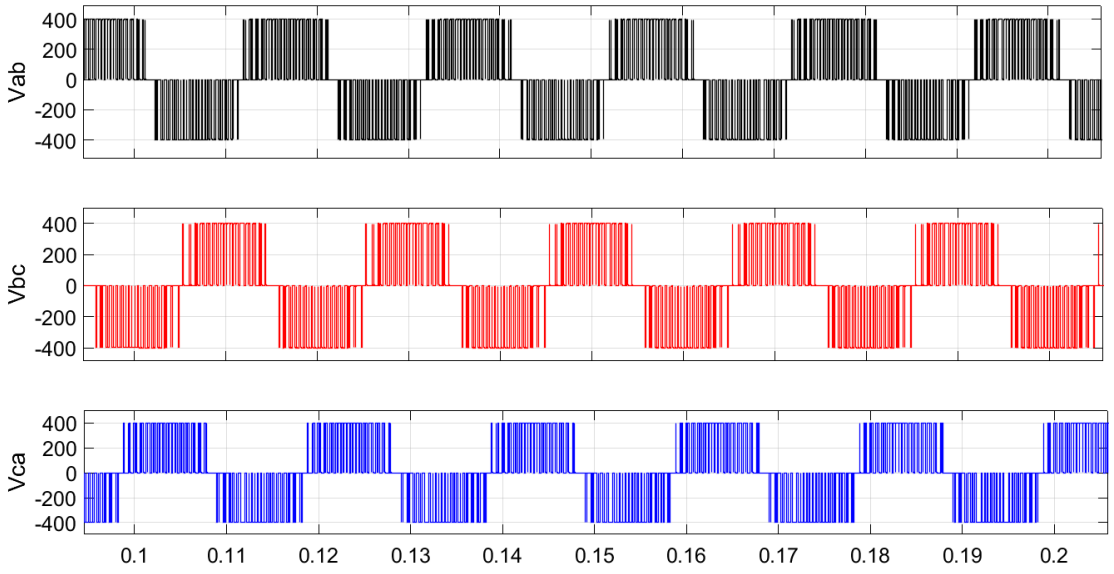



FIGURE 5.3: Line Voltages of 2-level VSI Using SPWM

### 5.1.1 Harmonic Analysis of 2-level VSI Using Both SPWM and SSVPWM

Harmonic analysis for both SPWM and SSVPWM techniques are done using Power Gui tool in MATLAB/SIMULINK. FFT analysis is performed on one cycle of $V_{ab}$ of the 2-level VSI for both SSVPWM and SPWM techniques.

Harmonics are the integer multiples of fundamental frequency, harmonics upto 10kHz are analyzed in Figure 5.4 and Figure 5.5. On x-axis harmonics on frequencies upto 10kHz is given and y-axis gives the magnitude in percentage of these harmonics which are present in fundamental waveform. Figure 5.4 shows the harmonic spectrum of 2-level VSI using SPWM technique. Harmonic spectrum of 2-level VSI gives the maximum amplitude at harmonic order 59 and 61 which is 30.5%. The THD of 2-level VSI using SPWM is 80.37%.

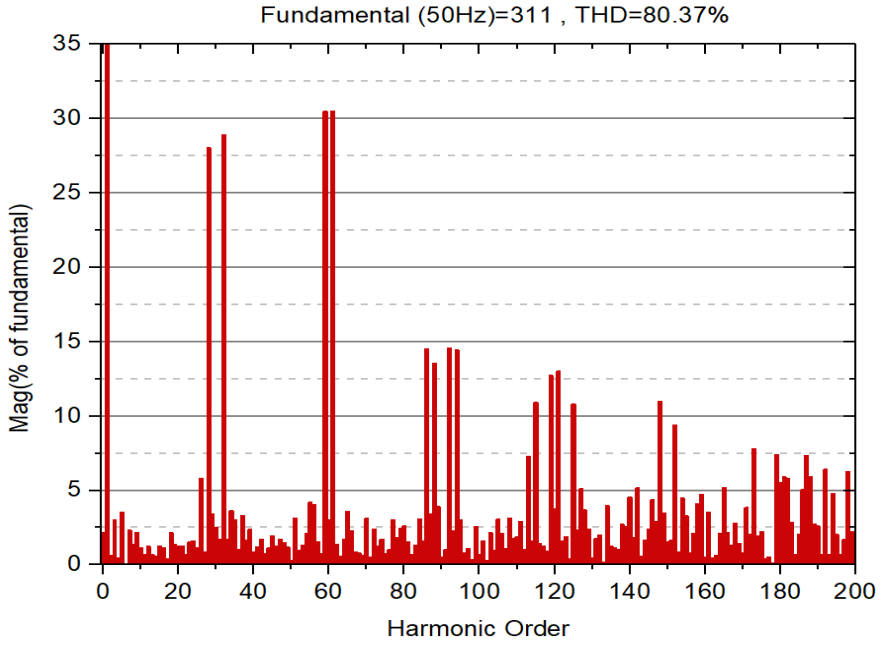



FIGURE 5.4: FFT Analysis of Line Voltage Vab for 2-level VSI Using SPWM Technique

Figure 5.5 shows the harmonic spectrum of 2-level VSI using SSVPWM technique. Harmonic spectrum of 2-level VSI using SSVPWM gives the maximum amplitude at harmonic order 61 which is 23.08%. The THD of 2-level VSI using SSVPWM is 67.91%.

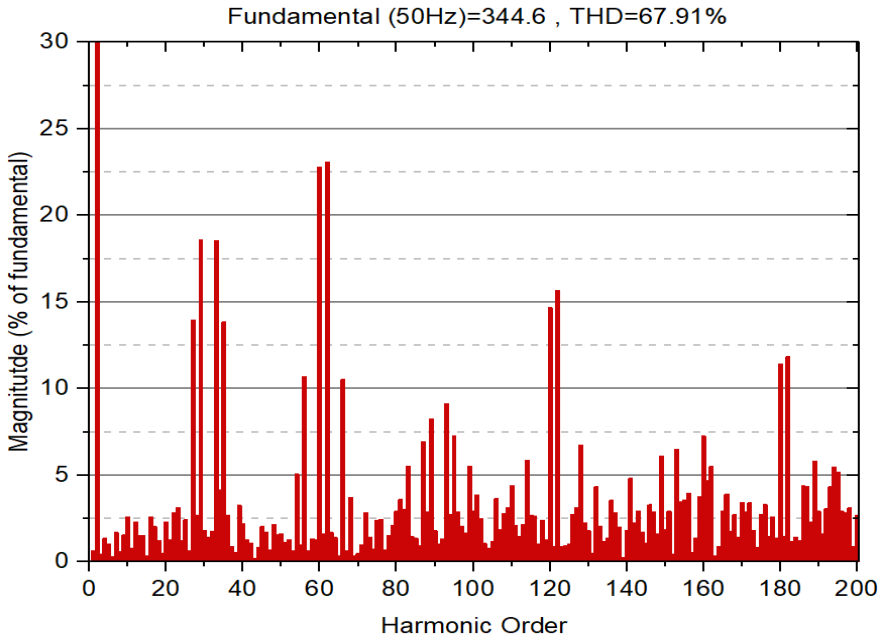



FIGURE 5.5: FFT Analysis of Line Voltage Vab for 2-level VSI Using SSVPWM Technique

## 5.2 Matlab/Simulink Model for SSVPWM Based 5-level MMC

Although the THD obtained from SSVPWM is less than SPWM technique in 2-level VSI but still the harmonic distortion is to high and can harm the system and cause problems so to reduce these harmonics filters are required which are costly. Increasing switching frequency can cause switching losses so multilevel converters are used. Modular multilevel converters (MMC) are more promising than other topologies as discussed earlier. So both PWM techniques are applied to 5-level and 21-level MMC and THD results are compared. The 5-level MMC model has the DC voltage of 1200V, fundamental frequency of 50Hz. Switching frequency and modulation index is kept 1500Hz and 0.9 respectively. The load which is connected to the 5-level MMC is 1600W. Table 5.2 shows the parameters of the 5-level MMC. Figure 5.6 shows the MATLAB/Simulink model of 5-level MMC.

TABLE 5.2: Simulation Parameters of 5-level MMC

| Parameter | Symbol | Value |
|---|---|---|
| Input Voltage | $V_{dc}$ | 1200 V |
| Fundamental Frequency | $f$ | 50 Hz |
| Switching Frequency | $f_{sw}$ | 1500 Hz |
| Modulation Index | m | 0.9 |
| Load | $L_0$ | 1600 W |

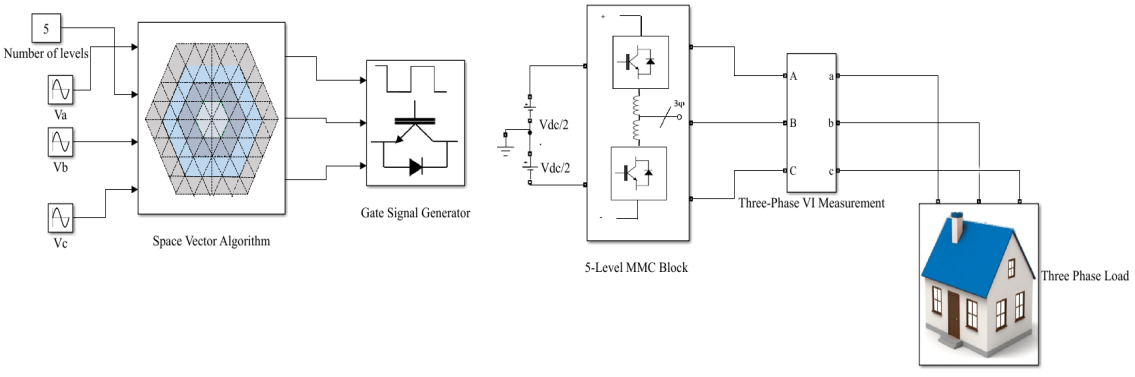



FIGURE 5.6: MATLAB/SIMULINK Model for 5-level SSVPWM Based MMC

The SSVPWM discussed in chapter 3 is applied to 5-level MMC the output line voltages $V_{ab}$, $V_{bc}$ and $V_{ca}$ are measured which are given in Figure 5.7.

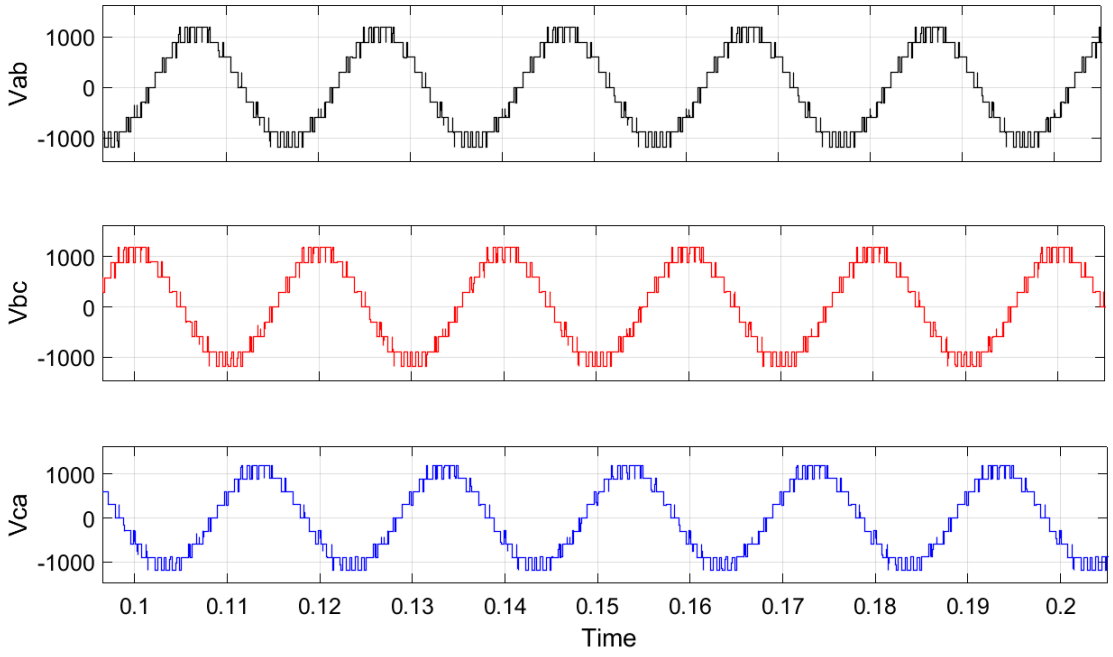



FIGURE 5.7: Line Voltages of 5-level MMC Using SSVPWM

SPWM technique is also applied to 5-level MMC. The output line voltages $V_{ab}$, $V_{bc}$ and $V_{ca}$ using SPWM technique is given in Figure 5.8.

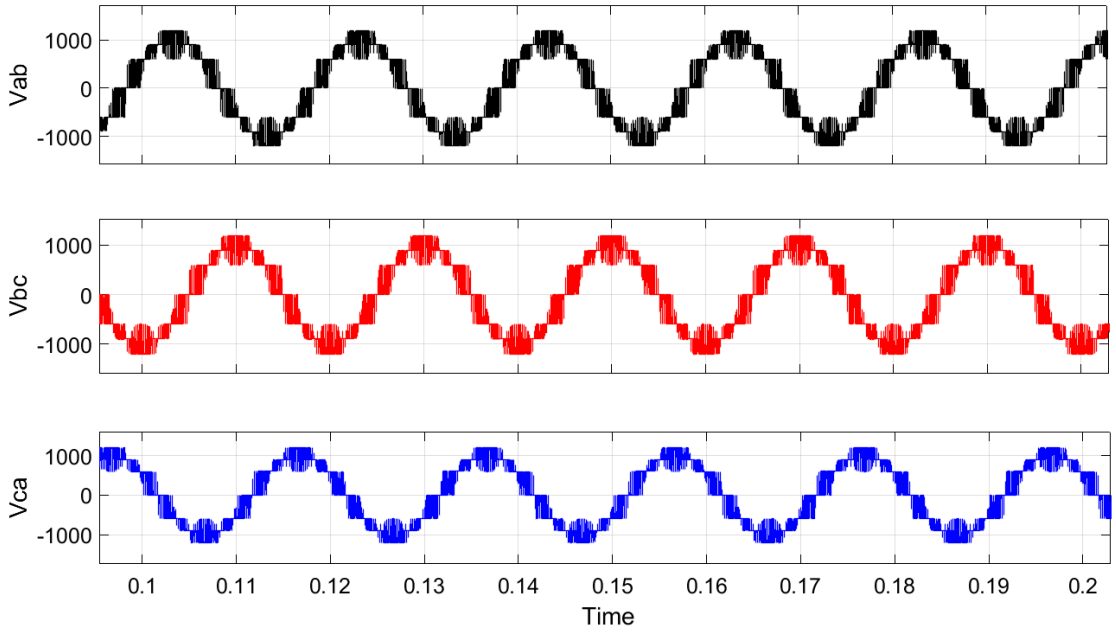



FIGURE 5.8: Line Voltages of 5-level MMC Using SPWM

### 5.2.1 Harmonic Analysis of 5-level MMC Using Both SPWM and SSVPWM

Both SPWM and SSVPWM techniques are applied to 5-level MMC and the harmonic analysis of the out put $V_{ab}$ is performed for one cycle upto the harmonics with frequencies 10kHz.

The harmonic spectrum of 5-level MMC using SPWM is shown in the Figure 5.9. Harmonic spectrum of 5-level MMC using SPWM technique gives the maximum amplitude at harmonic order 115 which is 11.72%. The THD of 5-level MMC using SPWM technique is 23.53%.

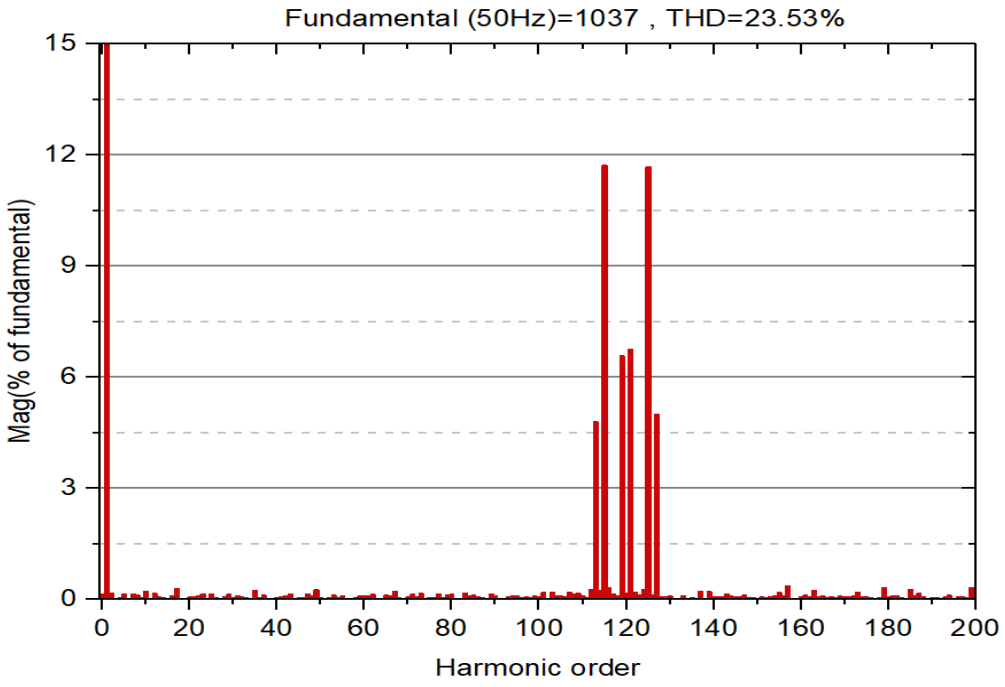



FIGURE 5.9: FFT Analysis of Line Voltage Vab for 5-level MMC Using SPWM Technique

The harmonic spectrum of 5-level MMC using SSVPWM is shown in the Figure 5.10. Harmonic spectrum of 5-level MMC using SSVPWM technique gives the maximum amplitude at harmonic order 31 which is 5.95%. The THD of 5-level MMC using SSVPWM technique is 15.09%. The percentage of THD obtained for 5-level MMC using SSVPWM technique is less than that of SPWM technique.

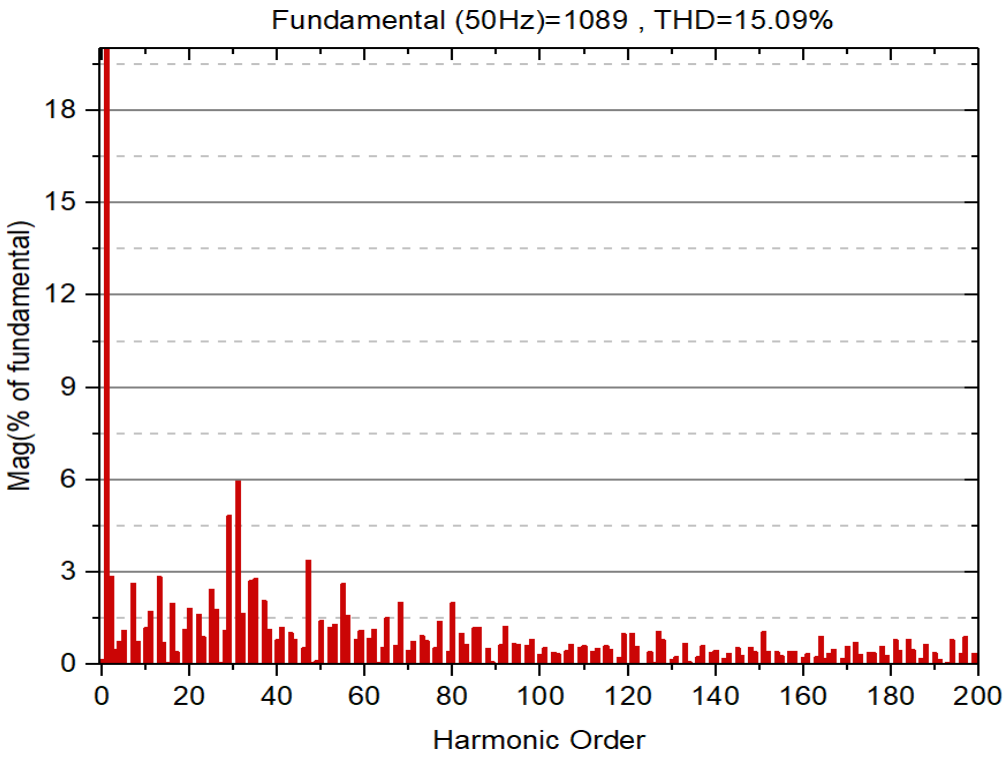



FIGURE 5.10: FFT Analysis of Line Voltage Vab for 5-level MMC Using SSVPWM Technique

## 5.3 Matlab/Simulink Model for SSVPWM Based 21-level MMC

The SSVPWM technique is also applied to 21-level MMC. The SIMULINK model is given in the Figure 5.11 and the model parameters are given in the Table 5.3. The line voltages for 21-level MMC is shown in the Figure 5.12.

TABLE 5.3: Simulation Parameters for 21-level MMC

| Parameter | Symbol | Value |
|---|---|---|
| Input Voltage | $V_{dc}$ | 100 kV |
| Fundamental Frequency | $f$ | 50 Hz |
| Switching Frequency | $f_{sw}$ | 1500 Hz |
| Modulation Index | m | 0.9 |

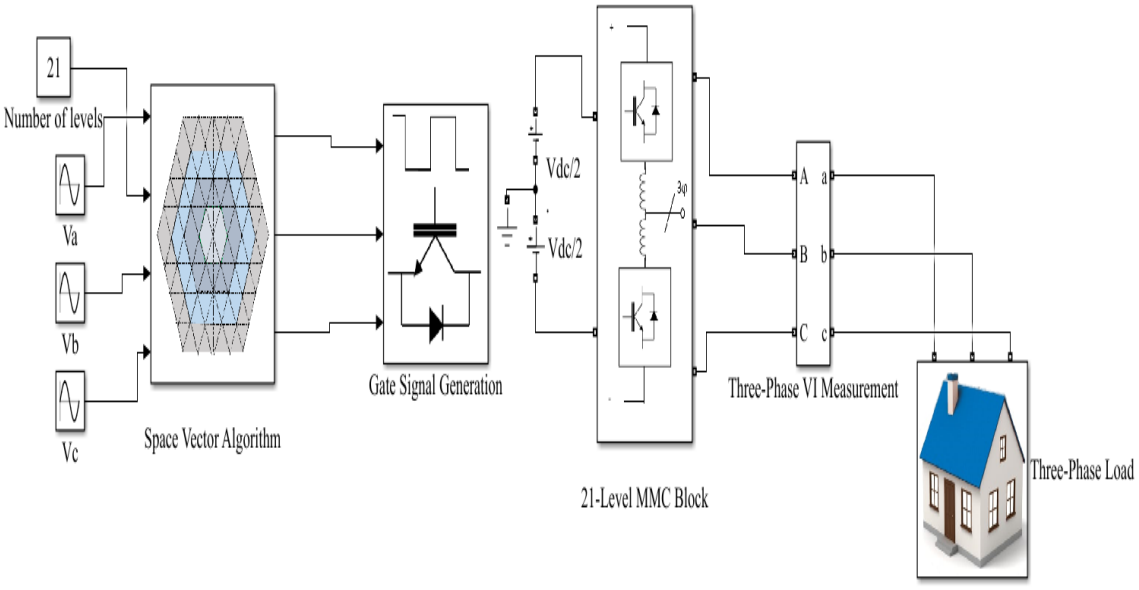



FIGURE 5.11: MATLAB/SIMULINK Model for 21-level SSVPWM Based MMC

The SSVPWM technique is also applied to 21-level MMC the output line voltages $V_{ab}$, $V_{bc}$ and $V_{ca}$ are measured which are given in Figure 5.12.

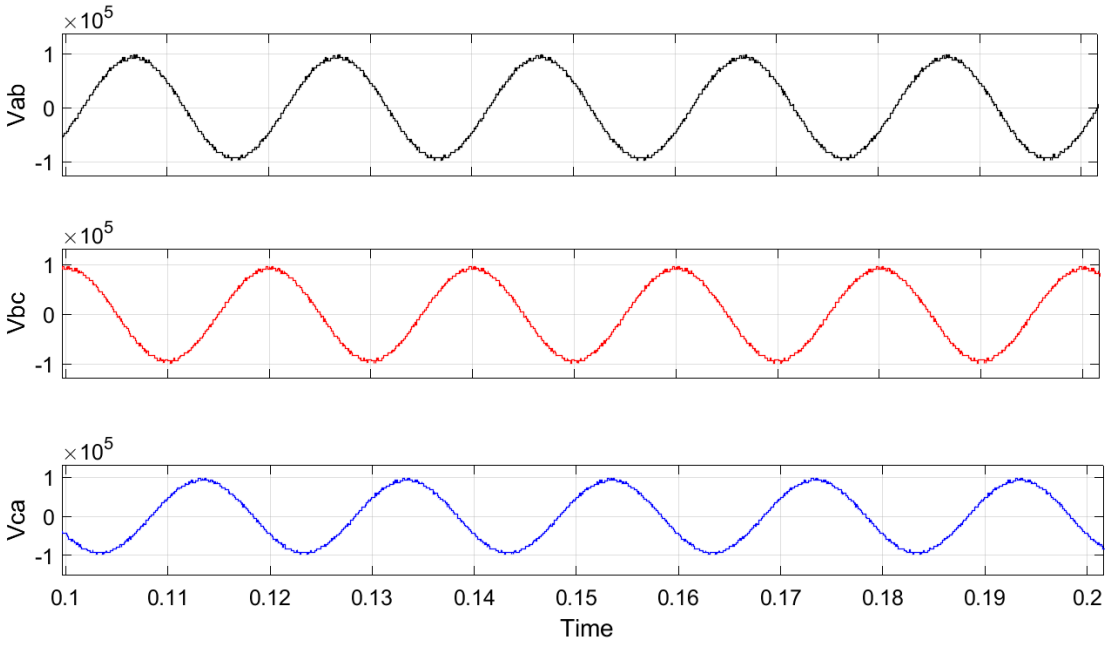



FIGURE 5.12: Line Voltages of 21-level MMC Using SSVPWM

The line voltages $V_{ab}$, $V_{bc}$ and $V_{ca}$ using SPWM technique is given in Figure 5.13

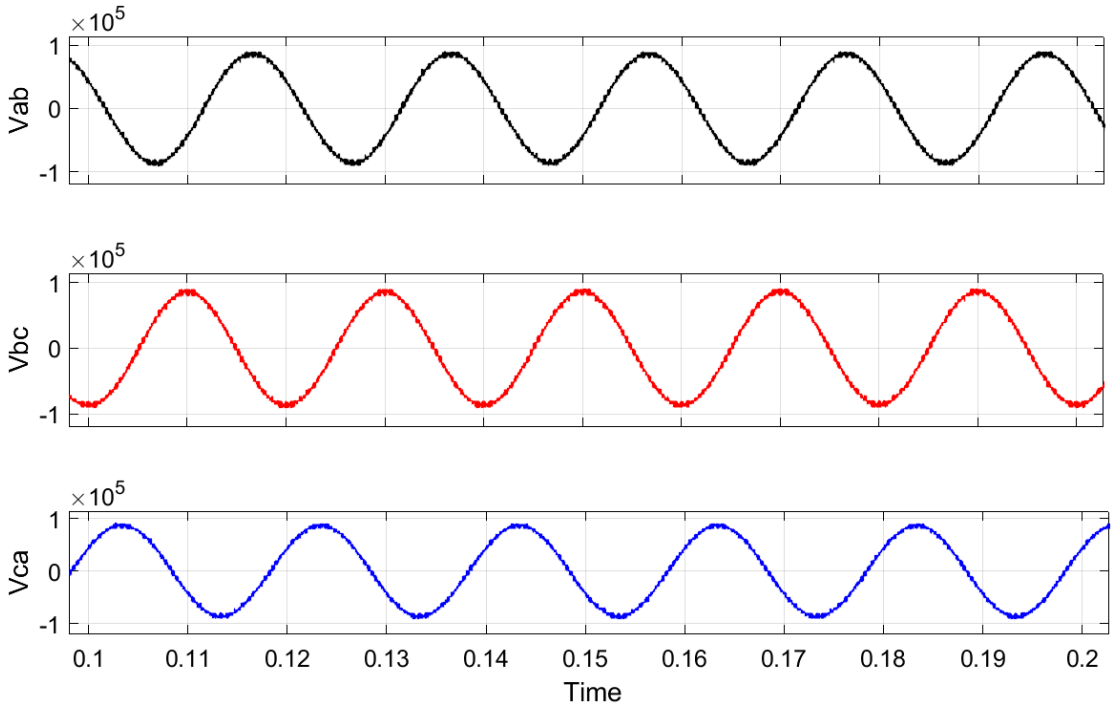



FIGURE 5.13: Line Voltages of 21-level MMC Using SPWM

### 5.3.1 Harmonic Analysis of 21-level MMC Using Both SPWM and SSVPWM

Both SPWM and SSVPWM techniques are also applied to 21-level MMC and the harmonic analysis of the out put $V_{ab}$ is performed for one cycle upto the harmonics with frequencies 1kHz.

The harmonic spectrum of 21-level MMC using SPWM is shown in the Figure 5.14. Harmonic spectrum of 21-level MMC using SPWM technique gives the maximum amplitude at harmonic order 2 which is 4.2%. The THD of 21-level MMC using SPWM technique is 5.92%.

The harmonic spectrum of 21-level MMC using SSVPWM is shown in the Figure 5.15. Harmonic spectrum of 21-level MMC using SSVPWM technique gives the maximum amplitude at harmonic order 16 which is 0.6%. The THD of 21-level MMC using SPWM technique is 3.35%.

The percentage THD obtained from 21-level MMC using SSVPWM technique is less than that of SPWM technique.

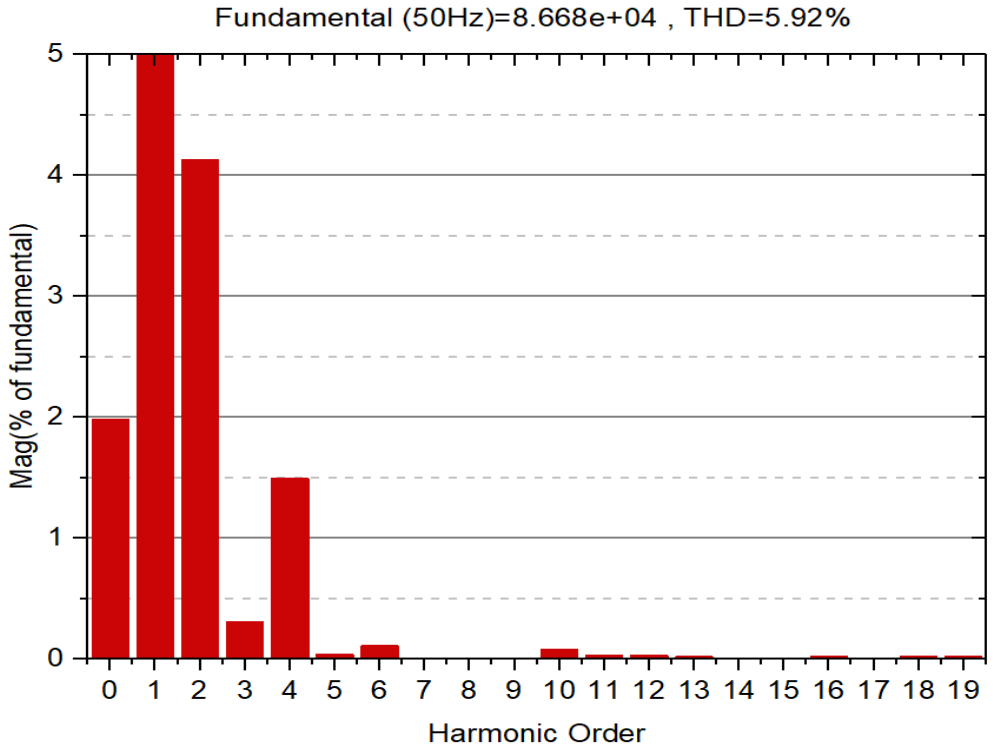



FIGURE 5.14: FFT Analysis of Line Voltage Vab for 21-level MMC Using SPWM Technique

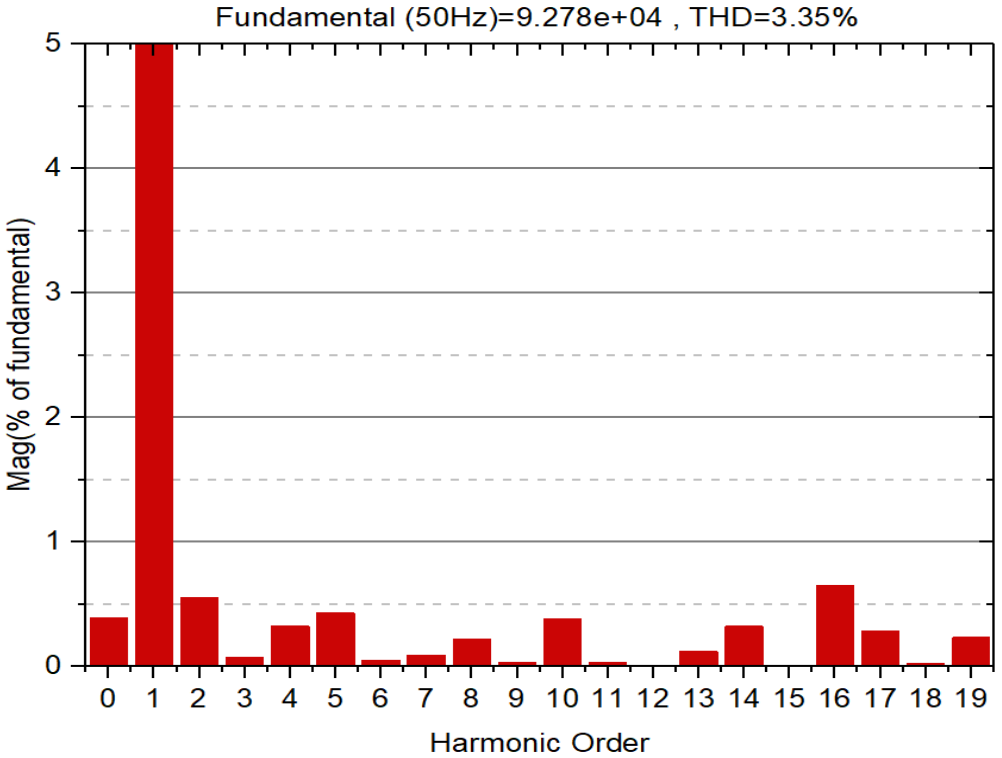



FIGURE 5.15: FFT Analysis of Line Voltage Vab for 21-level MMC Using SSVPWM Technique

## 5.4 Discussion on Harmonic Distortion Results

The presented improved SSVPWM technique is applied to 2-level VSI, 5-level MMC and 21-level MMC and a comparison is done between the SSVPWM and SPWM on the basis of THD. A trend of THD using SSVPWM and SPWM is given in the Figure 5.16.

Figure 5.16 shows that the THD in 2-level VSI is 67.91% using SSVPWM and 80.37% using SPWM technique. Although the THD obtained from SSVPWM is less than that of THD obtained from SPWM technique but still it is very high and can damage the equipment. Filters are required which deviates the certain harmonics from their original path to reduce the THD but they are costly and other disadvantages of filters are mentioned in Chapter 2. Increasing the switching frequency also can reduce the THD in 2-level VSI but increasing switching frequency causes switching losses so multilevel converters are used. Both PWM techniques are applied to 5-level MMC and 21-level MMC. The THD in 5-level and 21-level MMC using SSVPWM is less than that of THD obtained from SPWM technique. The results shows that the harmonic performance of SSVPWM is better than that of SPWM.

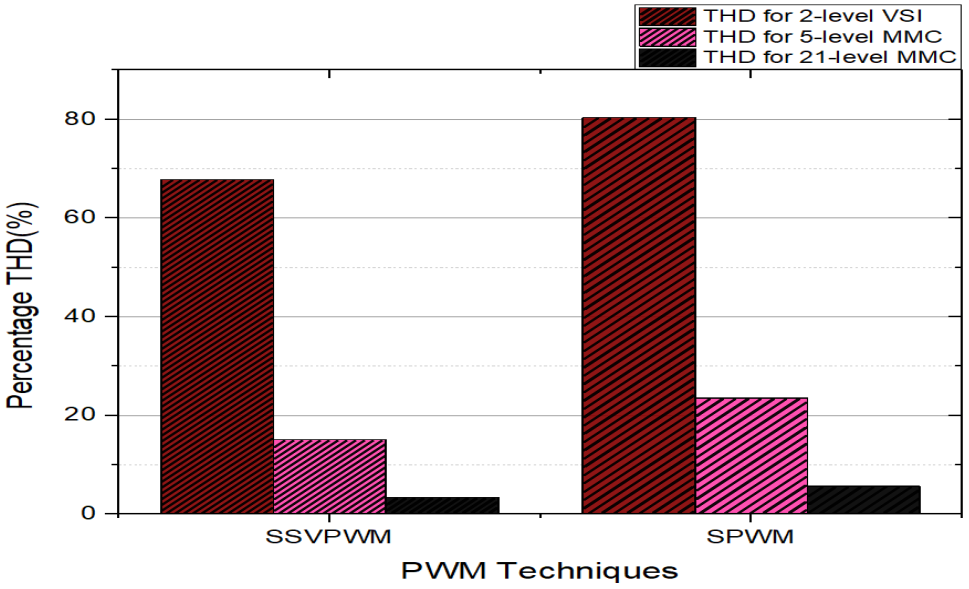



FIGURE 5.16: Comparison of SSVPWM and SPWM On The Basis of THD for 2-level VSI, 5-level MMC and 21-level MMC

## 5.5 Switching Loss Algorithm and Results

In order to calculate the switching loss in a semiconductor device we first have to choose the device which has the right voltage and current rating. For 2-level VSI SK60GAR123 from Semikron whose rated values are given in the Table 5.4 [26].

TABLE 5.4: Datasheet Parameters for Switching Losses for Semikron SK60GAR123 [26]

| **Parameter** | **Symbol** | **Value** |
|---|---|---|
| Reference Current | $I_{cnom}$ | 50 A |
| Reference Voltage | $V_{ccnom}$ | 600 V |
| Blocking Voltage | $V_{CES}$ | 1200 V |
| Turn On Energy | $E_{on}$ | 9.9 $e^{-3}$ J |
| Turn Off Energy | $E_{off}$ | 5.3 $e^{-3}$ J |

Where $I_{cnom}$ and $V_{ccnom}$ is the reference current and voltage taken from the datasheet. $V_{CES}$ is the blocking voltage value is specified in datasheet. $E_{on}$ and $E_{off}$ are energy dissipated while turning on and off the switch. Switching energy dissipations are approximated as linear function of the collector current, which means these energies are proportional to the current [26].

$$E_{on}(I_c) = E_{on}(I_{cnom}).(\frac{I_c}{I_{cnom}}).(\frac{V_{cc}}{V_{ccnom}})^{K_v} \tag{5.1}$$

$$E_{off}(I_c) = E_{off}(I_{cnom}).(\frac{I_c}{I_{cnom}}).(\frac{V_{cc}}{V_{ccnom}})^{K_v} \tag{5.2}$$

In equation 5.1 and 5.2 from [26] $V_{cc}$ and $I_c$ are the actual values obtained from the switch during simulation. $K_v$ is the exponent of the voltage dependencies. The value $K_v$ for 1200V IGBT is 1.4.

However the turn on energy $E_{on}$ and turn off energy $E_{off}$ is given in the data sheet. In order to calculate the switching losses we have to find the current and voltage at that switching time. When the gate pulse transitions from low to high

the current passing through the IGBT increases however the voltage does not fall immediately it takes a little time to fall. When current reaches its max value $I_{DS}$ the voltage starts to drop and reaches to zero this forms a triangle. The triangle shows the power dissipated during turn on and turn off period of the switch and the area under the triangle represents the turn on energy $E_{on}$ as shown in the Figure 5.17.

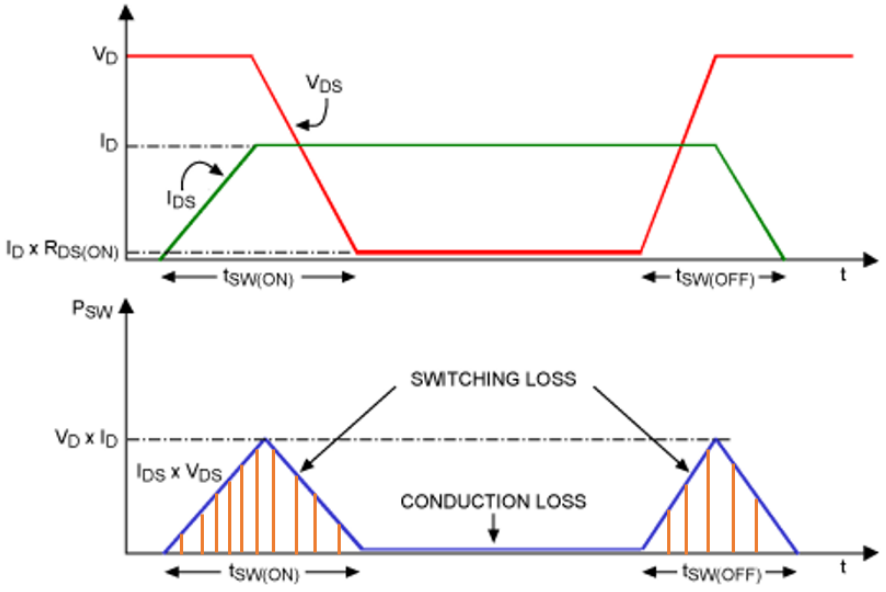



FIGURE 5.17: Switching Losses During Switching of Power Electronic Switch [27]

Figure 5.18 shows the MATLAB block for switching loss algorithm. In this block voltmeter is connected across the switch to measure the voltage across the switch and ampere meter is connected in series to get the current passing through the switch during the transitioning of the gate pulse. Hit crossing block is used to detect the rising and falling edge of the current and voltage at the right switching point to calculate the power loss during switching at that point. Memory block is used that holds and delays the current during when the gate pulse transitions from high to low it also holds and delays the voltage when gate pulse transitions from low to high.

This switching loss algorithm is connected to the IGBT of the 2-level VSI and 5-level MMC both with SPWM and SSVPWM and switching analysis is done.

Figure 5.19 shows the power loss during switching in a period. There are more power losses in SPWM technique as compared to SSVPWM at the switching frequency of 1.5 kHz.

Figure 5.19 shows the switching losses in a single SM of MMC in a period with the switching frequency of 1.5 kHz. Figure 5.19 shows there are less switching losses in SSVPWM technique as compared to SPWM.

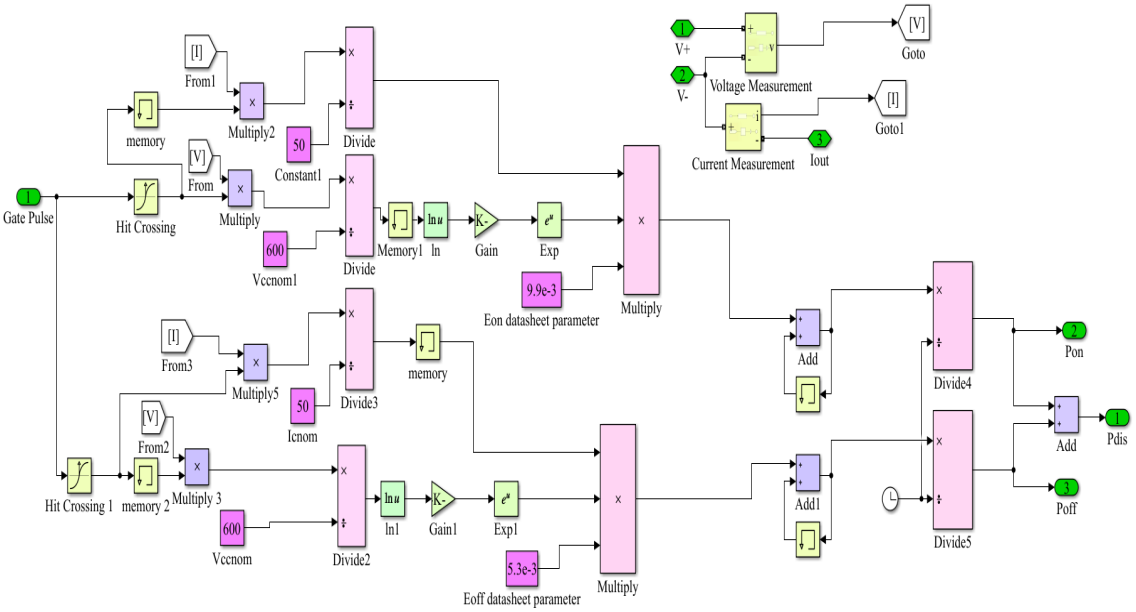



FIGURE 5.18: Switching Loss MATLAB/SIMULINK Algorithm

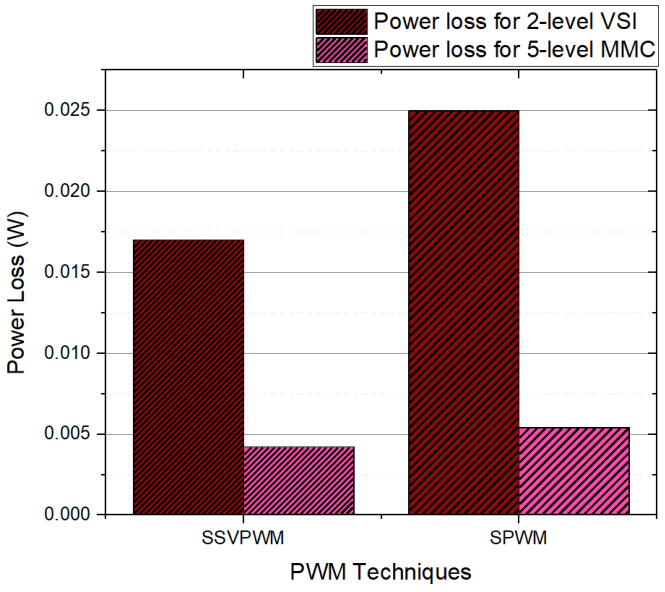



FIGURE 5.19: Power Loss During Switching of 2-level VSI and 5-level MMC In A Period Using Both SSVPWM and SPWM Technique

# Chapter 6

# Conclusion and Future Work

This chapter starts with conclusions drawn from the proposed study and what advancements can be made in the future is discussed in the future work section.

## 6.1 Conclusion

This study presented an algorithm which simplifies the SVPWM technique for multilevel converters. This SSVPWM technique is compared with the conventional SPWM technique. The presented SSVPWM technique is implemented on 2-level VSI, 5-level MMC and 21-level MMC and compared with sinusoidal PWM on the basis of harmonics in the output and losses during switching in an inverter. SSVPWM technique is applied and harmonic analysis is done using Power Gui tool in MATLAB/SIMULINK and the results shows that the THD obtained from SSVPWM is less than SPWM technique in any number of converter.
Switching loss algorithm is also developed in MATLAB/SIMULINK which measures the power losses when switch transition from off to on and on to off state. This switching loss algorithm is connected with 2-level VSI, 5-level. The switching losses are measured using both SSVPWM and SPWM technique. The results form Chapter 5 shows that the SSVPWM technique gives less power loss in switches as compared to SPWM.

From the results shown in Chapter 5 it can be concluded that SSVPWM is much better technique than SPWM technique as it gives less THD and less losses during switching.

## 6.2 Future Work

In the presented study this simplified space vector modulation technique is implemented on 2-level VSI, 5-level MMC and 21-level MMC at different load conditions. Switching loss and harmonic analysis is done. The presented study is applied on the standalone inverter (inverter not tied to the grid). Also the presented technique is applied in MATLAB/SIMULINK.

In future it is proposed that this SSVPWM is implemented on grid tied inverter. So in case of excess power from renewable sources can be supplied to the utility grid with less harmonics and switching losses. As SSVPWM is a digital technique this algorithm can be implemented using micro controller or FPGA and is recommended to implement to the actual physical inverter. Space vector technique can also be used in capacitor balancing in modular multilevel converters.

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