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Design and Analysis of Three-Phase 100 kVA, 20 kHz Solid-State Transformer

by

Irej Mahmood Baig

A thesis submitted in partial fulfillment for the
degree of Master of Science

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To my Family for their unbound affection

CERTIFICATE OF APPROVAL

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(Irej Mahmood Baig)

Abstract

It is anticipated that the most suitable alternative of conventional transformers in the coming future will be solid-state transformers (SST), owing to its numerous advantages, which have extensively been reported in the recent literature. SST can operate at a much higher frequency and voltages, as compared to conventional transformers, consequently results in reduced size of the transformer. Literature review suggests that the researchers have mostly concentrated on the designs of individual stages of SST, and missing a collective work required to demonstrate the whole SST design and analysis. In previous literature, lack of intentions has also been given to the harmonic reduction strategies. In this thesis, the design and analysis of a three-phase 11 kV/415V, 100 kVA SST operated at 20 kHz frequency,has been presented for the electric power distribution system. Shunt active power filter is used to improve the stability and reduce the THD, along with multi-stage dual active bridge (DAB) converters and sinusoidal pulse width modulation (SPWM) inverter. A mathematical model of SST has also been developed, based on analytical calculations, and has been implemented in MATLAB as well. The proposed methodology reduces the overall size and offers precise power flow control. Additionally, can also maintain better power quality, high power factor, and very low total harmonic distortion (THD) of current. Our simulation results verify the design, showing an excellent power factor and performance by a reasonable reduction in THD, from 130.09% to 1.2%.

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Abbreviations

AC	Alternating current
CPTs	Conventional power transformers
DC	Direct current
DHB	Dual half-bridge
DAB	Dual active bridge
D	Duty cycle
ESP	Electric power system
MFT	Medium-frequency transformer
MLT	Mean length of a turn
NLL	Non-linear load
PECs	Power electronic converters
SST	Solid state transformer
SAPF	Shunt active power filter
SPWM	Sinusoidal pulse width modulation
THD	Total harmonic distortion
T	Period of excitation waveform
VSI	Voltage source inverter
VT	Total Volume of transformer

Symbols

A_c	Effective cross section of the core
A_p	Area product
B_{sat}	Saturation flux density
B_o	Optimum flux density
B_{max}	Maximum flux density
h_c	Heat transfer coefficient
i_s	Supply current
i_l	Load current
i_c	Compensation current
K_c	Coefficient of the Steinmetz equation
K_a, K_b , K_w	Cores dimensional coefficients
K_v	Waveform factor
k_f	Stacking factor
k_u	Window utilization factor
l_m	Core Mean length
N_p	Primary number of turns
N_s	Secondary number of turns
V_p	Transformer primary voltage
V_s	Transformer Secondary voltage
V_c	Core volum
V_m	Winding volume
w_a	Window area
ΔT	Temperature rise

$\sum VA$	Total transformer power rating
ρ_w	Wire resistivity
ΔB	Peak to peak flux density
α, β	Coefficient of the Steinmetz equation

Chapter 1

Introduction

The power generation network has three major components categorized as power generation, transmission, and power distribution. Among them, the power transformer plays a vital role. Power transformer step-up voltages at the generation side at high efficiency as well as provide long-distance transmissions. The voltages step down at the substation, that is further utilized for industrial as well as domestic purposes, via a distribution system. Many enhancements have been implemented to improve the performance of a conventional power transformer. Nevertheless, a conventional power transformer (CPT) still exhibits many drawbacks; for example, large size, heavy-weight, high cost, de-rating due to harmonics, poor power quality [1] and poor voltage regulation [2].

Nowadays, power generation via renewable energy resources [3] has become a popular source for generating electricity. The integration of a CPT in a smart grid [4] is also challenging, i.e. reactive power control, integration Storage and DC-distribution. A possible solution to overcome all these challenges and drawbacks is a solid-state transformer (SST) also called the power electronic transformer. The solid-state transformer has some advantages over conventional power transformer which are,

- Lighter weight and smaller in size [5, 6].

- Harmonic elimination [6].
- Active and reactive power control [7].
- Voltage regulation and voltage Sag compensation [8].
- Power factor correction.

Although SST has many advantages over a conventional power transformer, still SST technology is not mature enough to be implemented in our grid system. In this chapter, the introduction of SST and topologies will be discussed.

1.1 Background

A device that transfers electrical energy from one circuit to another circuit through magnetic coupling without any motion between its parts is known as Transformer. A transformer is usually used to increase or decrease the voltage levels among its circuits. It consists of two or in some cases more than two coupled windings or coils and a magnetic core. When alternating current is applied at the primary side of the transformer, it produces magnetic flux, due to mutual induction; this alternating flux will induce an EMF in the secondary winding, which results in current flow in the secondary winding.

Power quality is one of the most significant concerns in the power generation network (i.e. voltage Sag and swell), to overcome these issues, smart-grid is a possible solution, that operates in a way to ease or avoid problems related to power quality [9, 10].

The solid-state transformer (SST) is an integral part of smart grids. SST not only helps to handle electricity routing but also provides advantages when utilized in a distribution grid. For example, it reduces the high current offered by the short circuit voltage dip and reactive power. But a trade-off between these advantages and the cost is required. One more thing that is of concerned while designing the SST is its complexity [11–13].

SST has low cost as compared to the conventional transformer, as SST designed with high power and voltage semiconductors [5, 6]. Due to switching losses in the semiconductor, the efficiency of SST is lower as compared to the conventional transformer. Therefore, we need techniques that will reduce the switching losses of semiconductors. These techniques are zero voltage switching or zero current switching. To reduce or eliminate the switching losses, resonant switching techniques are implemented by zero voltage or zero current switching.

The reliability of SST should be considered while designing SST, as it is not as much reliable as compared to the conventional transformer due to its complex and complicated design. Therefore, we need improvement in the design to make it less complicated. Over the past decade, extensive research showed that SST is an adequate possible solution that will replace the low-frequency bulky transformer [14–19].

Power electronic devices are available in the market, which has much fewer switching losses and possess high power and frequency at a low price. Subsequently, for a cost-effective and more reliable design, these switching devices must be used in the SST design. In that way, SST can be used instead of a conventional power transformer [20].

With immense advancements regarding electronic power device technology, their competencies and advantages have also played a critical role in the notable research related to the development of SST [21].

1.2 Solid-State Transformer

The "solid-state transformer" technology was first brought to discussion during the 1970s. In which a design was proposed, that stepped-up and stepped-down the applied voltages as a conventional transformer. The design was the same as that of the conventional transformer, with AC as input and output. Another method was proposed in the same year, which has an AC-AC converter that operates at

high frequency. That art-of-the-work enlightened the idea of a basic solid-state transformer with an AC-AC converter [22].

Later on, extensive work has been done on SST proposing different design methodologies, control strategies, topologies, and their operation [23].

During the past few years, SST technology has been progressing rapidly, and it has also been reported that this technology is the best replacement for a conventional low-frequency transformer in the modern power generation system. SST design is compatible with all voltage levels (i.e. High, medium, and low) at any side of the transformer (a primary and secondary side). Centralized power generation network with SST shown in figure 1.1.

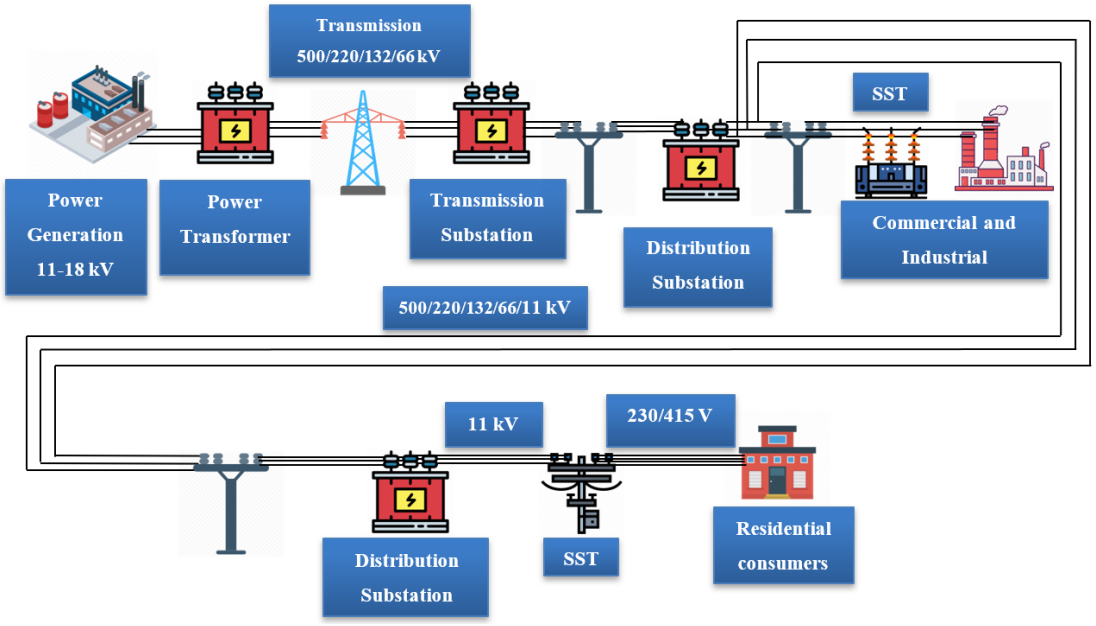

FIGURE 1.1: Centralized Power Generation Network With SST.

Pakistans generating electric power is 11-18 kV. To transmit power from generating units to consumers, a power transformer is usually employed that steps up the voltage up to 500/220/132/66 kV. At distribution substation, transformer steps down the voltages back to 11 kV, from that point, pole-mounted transformers are used to further drop the voltages up to 230/415 V for industrial and residential consumption.

Numerous SST designs have been introduced based on isolated AC-AC conversion,

which might be able to substitute the CPT in the distribution system. A few of them have been suggested in some cited literature [21, 24, 25].

The primary purpose of SST is to attain the voltage transformation, which is done by low to medium-frequency isolation and reduced weight and volume of SST as compared to the same rated conventional power transformer.

The basic structure of an SST is shown in figure 1.2.

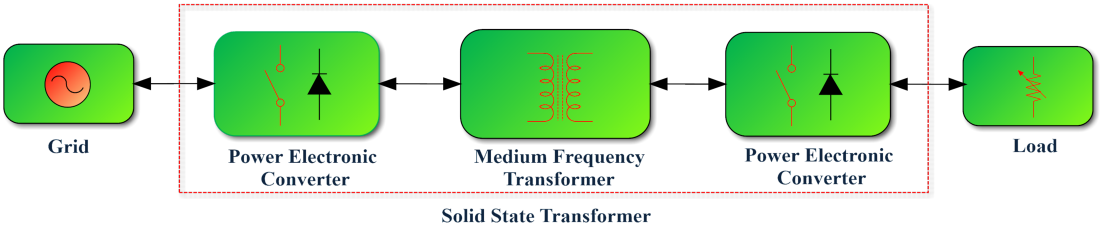

FIGURE 1.2: Basic SST Diagram.

In the basic structure of the SST, medium-frequency transformer (MFT) is used to achieve isolation. The grid voltage is applied at power electronic-based converters (PEBC).

PEBCs are used to transform a grid voltage into medium-frequency AC voltage so that it can be applied at the primary side of the MFT. While at the secondary side of the MFT, a reverse procedure is adopted so that AC is obtained for the load.

1.2.1 Solid-State Transformer Topologies

According to [25] solid-state transformer has been classified into three significant topologies, which are

1. SST with single-stage
2. SST with two-stages
3. SST with three-stages

1.2.1.1 Single-Stage SST

The main functionality of single-stage SST (shown in figure 1.3) is based on a transformer that has medium-frequency isolation, which can convert AC (Alternating current) at a medium voltage to low voltage AC without using a DC link (Direct current). A DC link is a link that provides the connection between the rectifier and inverter.

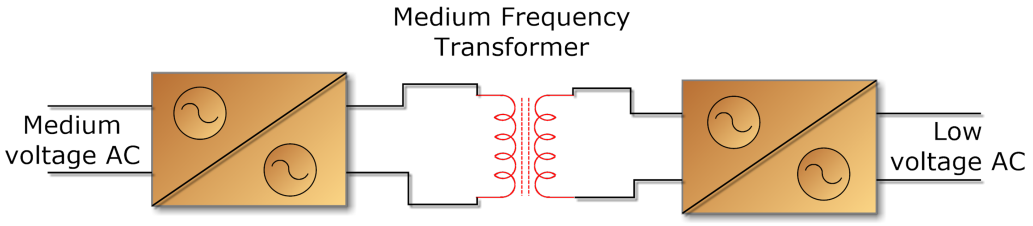

FIGURE 1.3: Single-Stage SST.

1.2.1.2 Two-Stage SST

The second topology of SST has two stages, shown in figure 1.4. In the first stage medium voltage, AC is converted to low voltage DC which is further converted into low voltage AC at a second stage called the inverter stage. This topology uses a DC link at a low voltage side.

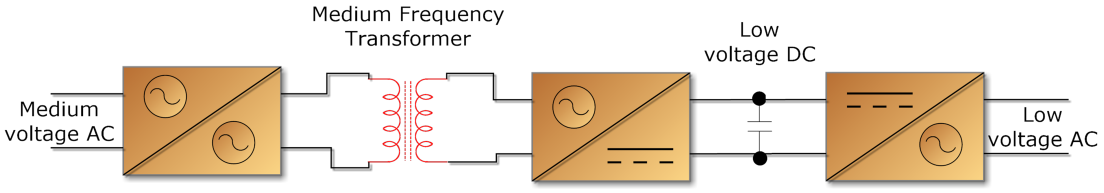

FIGURE 1.4: Two-Stage SST With DC-link.

1.2.1.3 Three-Stage SST

The third topology of SST has three stages, shown in 1.5. The first stage acts as a rectifier, the second as a DC-DC converter, and the third stage as an inverter. At the first stage medium voltage, AC is converted into medium voltage DC, at the

second stage medium to low voltage DC-DC converter is used that converts the medium voltage DC into low voltage DC. In the third and the final stage, a low voltage inverter is used to convert the low voltage DC back to low voltage AC.

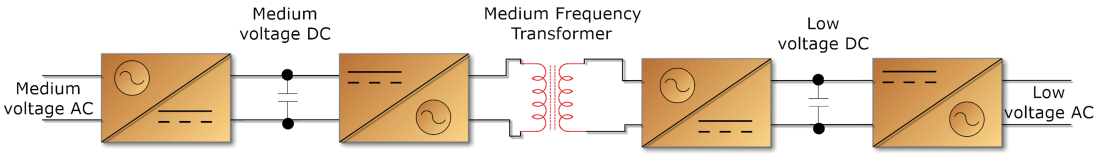

FIGURE 1.5: Three-Stage SST.

Due to flexibility in design and the chance of performance improvement at all stages, SST with a three-stage topology has the best potential to replace the conventional power transformer [20, 21].

1.3 Harmonics In Power System

The occurrence of non-linear currents and voltages in power distribution systems has recently increased due to the availability of inexpensive and reliable power converters. The existence of harmonics in electrical systems results due to distorted and deviation of current and voltage from the sinusoidal waveform.

Several non-linear power electrical devices caused non-linear currents and voltages when used in the power distribution system. Devices that can generate non-linear currents include transformers, induction motors, and power electronics devices (i.e., rectifiers, inverters).

Harmonics affect the performance of the power supply system. The main disadvantages are the maximum likelihood of resonance, an overload of the neutral conductor, increased losses in electrical machines, electromagnetic interference in communication systems, and overheating.

By using filters, harmonics content from the system can reduce; different methods are available for this purpose. These filters can be a passive filter or an active filter.

1.3.1 Harmonics Mitigation

By using filters, harmonics content from the system can reduce; different methods are available for this purpose. These filters can be a passive filter or an active filter. When passive elements are used to make the filter, then such a filter is called a passive filter, i.e. the inductor and capacitors. In contrast, analogue electronic filters are mostly active filters, which are primarily being used in high voltage supply applications.

1.4 Power Converters

Due to the great possibilities of power electronic converters interfacing between components and voltage levels in the power grid, power electronic converters are regarded as important components for SST. One of the most critical requirements for connecting two voltage levels in any design of a distribution system is galvanic isolation. A transformer is a component that enables galvanic isolation by transferring energy between two voltage levels through the electromagnetic field of a transformer without any electrical connection.

An SST comprises a combination of power electronic converters medium-frequency transformers. With SST in the distribution system, the various voltage levels are galvanically isolated using a medium-frequency transformer of the SST configuration, which considerably reduces the size and weight of the converter compared to conventional transformers having the same voltage and nominal power.

1.5 Motivation

Even though conventional transformers are very efficient, they still have many drawbacks, i.e. they are bulky, the voltage drop under load, problems related to the power quality, and sensitivity to harmonics. To overcome these problems, an alternative device was required, which should also offer bidirectional power

flow, reactive power compensation, volume and weight reduction, as well as the harmonic reduction. The above functionalities can be attained by instigating the idea of an SST.

SSTs have been recommended for several applications such as train traction, electric vehicle charging systems, offshore wind farms, and tidal power plants. Due to continuous improvements in the field of power semiconductor devices and more efficient converter topologies, more research has recently been devoted to the implementation of SST in distribution systems and the intelligent power supply systems.

To overcome future problems related to the power supply systems and the recent focus on SST applications in power distribution systems, the motivation for this study is therefore to propose a three-stage SST topology based on the multi-level structure of the converter.

1.6 Thesis Overview And Structure

This thesis comprises six chapters, distributed as follows:

In **Chapter 1**, an introduction covering background, SST technologies, Harmonic mitigation, power converters, and thesis overview

Chapter 2 covers the extensive literature review on the stages and design of a solid-state transformer, various strategies for controlling an active power filter, and an isolated DC-DC converter. Literature research is deeply organized so that each part is discussed separately.

Chapter 3 covers the three-stage of SST. This chapter is divided into four parts. First part is mathematical model of SST, in which voltage equations of all three stages (AC-DC rectifier, DC-DC converter, and DC-AC inverter stage) are demonstrated. The second part is AC-DC controlled rectifier, the third part is DC-DC converter, in which the DC-DC converter stage is illustrated. DC-DC converter

stage is based on a multi-level dual active bridge and medium frequency transformer. Furthermore, this chapter also focuses on the design of a medium frequency transformer. The third and final stage DC-AC inverter of SST is presented. DC-AC inverter is based on a three-phase voltage source inverter. And the methodology used to design an inverter is based on sinusoidal pulse width modulation.

In **Chapter 4**, the harmonic mitigation technique is presented, which is one of the main objectives of SST. The method used for harmonic mitigation is based on Shunt active power filtering. The two main parts of SAPF, reference current generation (based on p-q theory) and current injection control techniques (based on hysteresis current control) are discussed.

Chapter 5 presents the results accomplished through the simulation of the proposed design.

Chapter 6 The overall conclusion and the recommended future work of our thesis are discussed in this chapter.

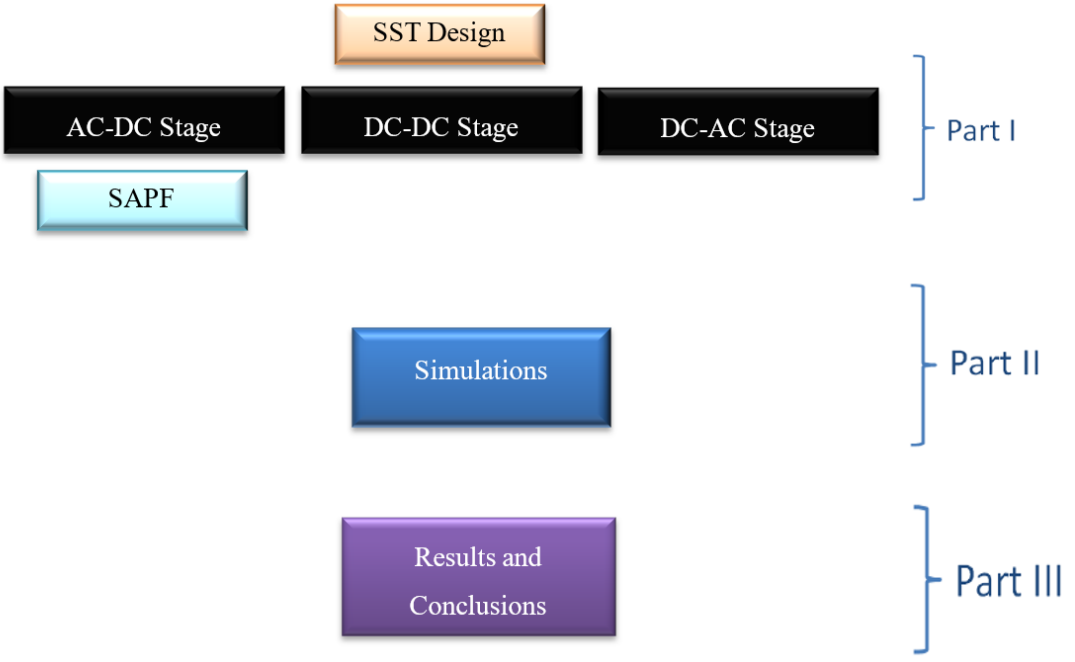

FIGURE 1.6: Thesis Overview.

1.7 Summary

In this chapter, the Solid-state transformer (SST) introduction has been covered. It is also suggested that SST will offer the best possible solution to replace conventional transformer due to many advantages. An overview of SST topologies is also carried out, in which three-stage SST is considered as the most acceptable among them due to its design flexibility and performance. Power quality and its issues were also pointed out, in which harmonics represent the major problem. Afterwards, an overview of the power inverter devices is presented.

Chapter 2

Literature Review

2.1 Introduction

In this chapter, detail previous research work that has been done on the solid-state transformer and its stages, have been provided with references. This chapter is divided into four sections. In the first section detail, a general literature review of SST is explained.

In the second section, the first stage of SST, which is an AC-DC rectifier, is discussed. DC-DC converter and its techniques are investigated in the third section. While in the fourth and final section of this chapter, previous research work on DC-AC inverter is presented.

2.1.1 Solid-State Transformer

Six topologies that are used for the implementation of SST have been introduced and compared in reference [26]. These comparisons are not only based on regular transformer performance but also include some extra characteristics (which are voltage regulation and reactive power) that help in implementing of SST. The comparison and simulation results show that SST with three stages is the most suitable topology. Because of its control and other design parameters.

A control scheme for power electronic transformer, based on its operation has been established in reference [27]. The transformer has a control input stage that controls the independent output stage, with the high-frequency link, results in power factor correction, reduced harmonic injection, and voltage sags.

Detail review on SST previous research work has been introduced in reference [28] the research work is based on technologies that are used in SST and have very significant for their development. It covers high voltage devices, converters, and high frequency required for transformers development. The research also provides the SST applications used in the power distribution system.

The startup scheme for three-stage SST at high frequency has been discussed in reference [29]. A comprehensive analysis of the current of the DC-DC converter transformer during SST startup showed that the key solution for suppressing the transformer current is to minimize the voltage difference between the primary and secondary side of the transformer during the transition. Consequently, due to the large voltage difference, the step-by-step process will result in a high transformer current as the DC-DC converter is activated after the rectifier starts up.

The architecture of an electronic transformer (SST) in which harmonics are removed by using power factor correction is explained in detail [30]. The proposed architecture has neither used oil nor any other liquid as dielectrics. According to design, faults are controlled in a way that they didn't affect the distribution system. The design is then simulated, and the result shows that the transformer is self-protected and improved in power quality when compared to the conventional transformer. The problem with the design is that it's not only costly but also has less efficient. Therefor needs to improve semiconductor switching for cost-effective design.

A review based on SST that covers the research work on SST [31]. A complete list of references is provided, which are based on SST, its application, design, control strategies, modelling, testing, and topologies. It also includes the tables on which prototypes and their models are implemented using real-time simulation platforms and tools. It also points out some issues related to SST, which have low

efficiency, a large number of semiconductor devices used, switching loss, filters, and reliability. It is suggested that a three-stage SST configuration is the best possible solution for the optimal design of SST.

SST uses and topologies, along with Pros and Cons, are reviewed in reference [32]. It also covers the analysis of these topologies concerning new demand and usage of SST when integrated with renewable energy-based technologies. The analysis is based on four properties which include the strengths of SST, i.e. its size and power factor correction, its weakness, i.e. high cost and reliability, its opportunities, i.e. integration with renewable energy and its possible threats, i.e. cost. The review also includes the SST integrate with grid-connected wind turbines.

Conventional transformer, when operating at low frequency, became larger in size and expensive. The use of an electronic transformer at high frequency can overcome these problems without altering its conventional behaviour, i.e. Input and output [33]. Static converters at both ends of the transformer (i.e. at primary and secondary side) along with magnetic core are used. The design has the same conventional core, which is of grain-oriented silicon steel. To overcome losses snubber circuits along with capacitors filter are used, which follow a four-step switching strategy. Experimental results show that an electronic transformer has high power at high frequency.

An SST and its topologies are explained in detail [34]. These topologies based on static converter along with magnetic circuits are linked with the primary and secondary side of the transformer. The aim is to propose the design of SST, which is smaller in size, has improved voltage regulation, efficiency, and reduced losses produce in transformers. The proposed design, when operating at a high-frequency process three-time more power as compared to low frequency.

Different type of auxiliary power supplies (APS) used for SST is introduced in [35]. The main focus is on two APS, which are medium voltage and low voltage per module. A static converter that has high voltage gain is used at a medium voltage side while any static converter can be used at a low voltage side. The use

of two APS per module results in more reliable SST when compare to one APS per module. Power factor correction is also utilized in this technique.

Different topologies of SST are discussed in [36]. These topologies are classified based on power electronic devices, high frequency, losses, size, and cost. These topologies are based on a dual active bridge (DAB) and boost converters technologies. The result shows that SST with boost converter shows the highest efficiency but with more power electronic devices. It also proposed the design equations and calculation of current values for boost converter when used with SST.

The medium frequency transformer detail design parameter for their used in SST is explained in [37]. The design is based on a water-cooled transformer that has a high power density. The proposed transformer is a sub-part of a DC-DC converter. The design is also proved with the help of the experiment. In this design water cooling system has aluminium plates that are used to assert pressure in the core and winding of the transformer; which results in transfer through heat skins. These results are verified by using the finite element method (FEM) simulation, which shows that this design not only cools the transformer but also reduces the eddy current losses.

Solid-state transformer previous research work is reviewed [38], the research is divided into three major categories which are medium-frequency transformer, AC-AC converter, and SST applications. All these categories are explained in detail in different sections..

Medium frequency SST efficiency and power are improved by investigating two different available cores and copper materials [39]. It also includes practical aspects of designing SST while using different cores and materials (Ferrite and Nano-crystalline) and provides an optimal solution that also contains a cooling system. The proposed analysis is called Pareto front analysis. The result shows that a transformer with Nano-crystalline has higher losses as compared to Ferrite.

Different type of techniques used for solid stage transformer has been discussed [40]. Most of the SSTs are not able to connect with the DC grid as they are

compactable with high voltage DC (HVDC). It focused on modular technique with a multi-level converter which is based on High voltage AC and DC and also on low voltage AC and DC. Due to its compatibility HVAC, the proposed SST easily connects with the DC grid.

SST with multiple cores PCB layout designs is proposed in [41]. The converter used in the proposed is Dual active bride. The purpose design is to get the bidirectional power flow and for switching devices to achieve zero voltage switching. For the transformer, high efficiency at high frequency, a predicted method is introduced.

A cost-effective solution for SST, which uses AC-AC buck-boost converter is proposed in [42]. The converter used in a way that it efficiently used semiconductors devices and chopped AC links so that the transformer magnetic core size was reduced. The converter used only six devices for three-phase AC systems results in a reduction of the size of the transformer as well as cost. The converter used in the design is suitable for low power applications. The design needs for improvement in converter design, which can be done by using a dynamic model based on state-space averaging techniques. On a system in which periodic waveform is used.

A new design is proposed for SST by comparing a conventional transformer with different models of SSTs [43].The main focuses are to introduce two topologies, one in which the core size and weight of the transformer kept constant while change the operating frequency to double. While in the 2nd case, the operating frequency kept constant and reduced the size of the core. The result shows that option 1 is far better than 2nd one, due to low voltage drop, cost, and much better power efficiency. The proposed design has one issue, which is humming noise, which results due to keeping a core size constant while operating at high frequency.

Active power electronic transformer with improved power performance, when used at high voltage, is introduced [44]. It has three stages with controllable input and output. The module works on a single phase and provides galvanic isolation. So that if there is any voltage fluctuation appears on the input side will not have any effect on its output. The same is true if any disturbance happens at the output side.

2.1.2 SAPF And AC-DC Rectifier Stage

A review based research publications on active filters (AF) discussed in [45]. This review is based on configurations of the active filter along with other control techniques, components selections, and their uses. The focus is to provide complete research to overcome the power quality issues using AF. The configuration based on harmonic removal, compensating reactive power, and distorted current.

DC link voltage control techniques as a reactive current component are presented in [46]. These techniques are compared with the conventional method in which dc-link voltage control is used as an active component. The method used in these techniques is based on the PWM method. When the PWM method with dc-link voltage control as a reactive current component used as a startup process for LC coupling hybrid active power filter it is noticed both dynamic reactive power compensation, as well as the self-charging process, are achieved.

A shunt active power filters techniques which are based on a scheme called fast response one cycle control presented in [47]. The improved method for one cycle control strategy is explained in detail, along with its disadvantages. A triangular waveform is used in a design strategy along with a sensor to monitor current and voltage. Due to fast response, it has improved response for non-linear loads for eliminating harmonic contents. Through simulation results, it is shown that performance and cost of design significantly enhanced when compared with conventional strategies.

A scheme is proposed to eliminate the switching losses in [48]. To do this, the technique used is based on hysteresis band current control but has switching losses as it operating at the high switching frequency. To overcome switching losses of converter that is based on a hybrid active power filter a system is introduced called adaptive fuzzy hysteresis band control, in which the fuzzy hysteresis band is developed by formalized the relationship between frequency and current harmonics.

A method is proposed to compute the upper as well as lower hysteresis bandwidth [49]. The methodology used to control the current is adjacent to the current error

zero-crossing time that computes the result when half the current error period is passed. This methodology does not depend on load parameters therefor stable switching frequency can be achieved. This methodology is implemented on hardware which consists of an inverter that has three levels H-bridge. The advantage of this strategy is that it overcomes the dead time effects without effecting different parameters, i.e. bandwidth limits, current error, and switching states.

Two techniques are explained that are used to generate the reference current to eliminate the harmonic contents [50]. These are instantaneous reactive power (IRP) and synchronous reference frame (SRF) and for shunt active power filter. In IRP theory, there is no need to remove the AC component as this theory does not require a filter. For this reason, it is used in both states, i.e. steady and transient state. The result shows that a later technique SRF has better performance in terms of reducing harmonic contents form the system.

A method is proposed to design the controller for fundamental as well as for harmonic contents, and the controller is based on an array resonant current to decrease computational effort and act as a fundamental reference frame [51]. The technique used to implement the controller, is pole-zero cancellation, to provide transfer function with much better frequency response. For this, two design methodologies are proposed. Both techniques are designed in such a way that the overall current controller is considered as a superposition of entire individual harmonic controllers.

A shunt active power filter with a vector operation technique to overcome the switching losses is introduced [52]. The method used for this technique is based on a converter with sliding mode control. To do this two-dimensional frame is used for voltage and current along with a modular and sliding mode controller. The sliding mode controller is designed in a way that provides the sinusoidal wave in which grid voltage and current are in phase, has a fast transient response, eliminates device losses, and able to track the current.

A controller that has a fast response of tracking and accurate current and injects the harmonic current into the grid is presented [53]. The method is based on

adaptive fractional fuzzy, and the controller is based on the sliding mode technique. The fuzzy system, when used with adaptive law, helps to find unknown controller parameters. The proposed design is implemented on hardware, and real-time performance is verified the result shows that when compared with the conventional fuzzy system, it has more reliable performance, improved THD, and comparatively fewer errors when tacking with more steady DC voltage.

An improved method for a predictive control algorithm in terms of waveforms harmonic spectrum is introduced [54]. The improved modulated algorithm is based on the cost function and eliminates the ripple current. The controller used in this method is a single loop with self-synchronizing with a grid and has modulated output but still provides better dynamic performance. To remove the harmonic content from an active shunt filter, a reactive power compensation technique is used. When compared with the classic algorithm, experimental results show that the modulated predictive control algorithm has better control for the active filtering system.

A design is suggested that control the harmonic produce in electric systems [55]. This consists of both types of loads, i.e. linear and non-linear. The recommended design controls the distorted current and voltage waveform and reduces the interference that appears at the source and load's side. The design models with steady-state limitations and power quality issues are also presented.

2.1.2.1 Reference Current Generation

In SAPF for reference current generation, a comparison of three control strategies (IRP, SRF, and DFT) is proposed in [56]. At different load conditions performance, these strategies are evaluated, which is based on THD in steady as well as in the transient state. Among them, DFT shows the best performance both in steady and transient states.

For reference current generation in SAPF, a comparative study is carried in [57]. The comparison is made between p-q and d-q theories, which are based on THD,

Power factor, and reactive power. Result suggests that d-q theory has better performance as compare to p-q theory.

For optimal reference current generation in SAPF, a new algorithm is introduced in [58]. This algorithm is based on Fourier series expansion, in which fundamental and harmonic currents are extracted. The simulation result shows that this algorithm has generated an optimum reference current.

In SAPF for reference current generation, a recursive discrete Fourier transform-based method is introduced in [59]. For the change in input frequency, the proposed method accurately extracts the reference current, without effective system performance. The proposed method is justified with the help of simulation results.

For reference current generation in SAPF, conventional methods for reference current generation are reviewed in detail along with their advantages and disadvantages [60]. These methods are divided into three groups which are time domain, frequency domain, and other methods. In time-domain, p-q and d-q theories are used for reference current generation. While in frequency domain FFT, recursive DFT, short-time Fourier transforms, and wavelet methods are used. Other methods, i.e. adaptive filtering and evolutionary computing, are also introduced.

2.1.2.2 Current Injection Techniques

Due to the presence of non-linear loads, current harmonics are generated which need to be eliminated. One method that uses for such a process is SAPF. Current injection is a technique that involves in SAPF design and is used to mitigate the current harmonics by injecting reference current equal and opposite current in the system parallel to the load, which results in making supply current wave shape pure sinusoidal. In three-phase SAPF, for current injection, different control strategies comparison has been made in [61]. These are delta modulation control, one cycle control, and hysteresis current control. The performance of these techniques depends on, how efficiently current is injected into the system and by calculating the THD.

A control algorithm based on a digital prediction of current injection, in SAPF, has been proposed in [62]. When there is a change in voltage source and load current has variation, the proposed method in a stationary state allows precise compensation, using the FIR controller. The proposed design when the simulated result shows improved behaviour.

2.1.3 DC-DC Converter Stage

A medium voltage intelligent universal transformer with its circuit and multi-level converter is introduced in [63]. The transformer will isolate the disturbance caused on both sides (Load side or Input side) due to its intelligent circuit. Therefore transformer performance and quality are improved. The experiment result shows that the output of the transformer is not affected by any kind of disturbance produced by the load. Also, it generates an excellent sinusoidal waveform.

Five levels DC-DC converter to reduce losses that are produced by SiC devices are presented in [64]. The primary purpose of this is to get a soft turn ON. This is done by using three flying capacitors and run on a high frequency. Control logic is also used so that loss in the duty cycle can be compromised. The overall advantage of this converter is that the performance of SST is significantly improved.

A design in which a dual half-bridge (DAB) DC-DC converter is used is proposed in [65]. The design consists of multiple DC-DC converters in series operate at low voltage and high frequency in a way that switches losses will be minimal. In this design, planar transformer coils are closed inside the PCB layers to reduce the core loss and gain high power density.

An improved design of the DHB converter is proposed in [66]. In which adaptive inductor is used along with phase shit DHB. In this design, the inductor controls the phase shit as well as achieved the zero voltage switching when operated at high frequency. An experiment shows that this design has improved efficiency when used with both heavy and light loads.

Multi-level inverter techniques and their control methodologies are introduced in [67]. This includes diode and capacitor clamped and cascaded multi-level inverter. The control scheme is based on PWM, removal of harmonics, and modulation, i.e. vector space modulation. The purpose of this research work is to give an idea of the selection of which technique and control scheme favours the most. These methodologies and techniques didn't include high voltage and high power semiconductor devices, high-speed DSPs, and thermal management.

Transformer design in which high power DC-DC converter is used is presented in [68]. The purpose of this design is to overcome three significant issues that are facing when developing the transformer. These are voltage spike along with losses caused by semiconductor devices, transformer winding loss, and the problem caused by rectifier diode, i.e. voltage fluctuation. An improved snubber circuit is used as a solution to voltage fluctuation, voltage spike, and switching loss.

Detail applications of the DC-DC converter, which has series input and parallel output are explained in [69]. This converter is based on the current mode and used a shared bus commercial off the shelf architecture for the DC-DC converter. In this architecture higher side voltages (which are at the input of the system) are converted into lower voltage (on output). So, the efficiency of the DC-DC converter increased. It also explains in detail the topologies used for architecture to control the voltage distribution. The final architecture still has a problem while controlling the control distribution, which affects the converter performance hence increased the power consumption.

The synthesis model of DC-DC converter running on medium voltage (4-40 kV) with low voltage PWM and high-frequency converters is explained in [70]. The model of converter simple in design and has high redundancy when compared with previous models. All simulations are done when the converter is used in closed-loop operation.

Overview of different topologies of power converter along with analysis of sinusoidal PWM inverter is covered in [71]. There is also a comparison between different types of PWM and sinusoidal PWM techniques. Sinusoidal PWM hardware is

also implemented, and it's shown that the total harmonic distortion of this type of inverter is decreased when the modulating index is increased. .

Comparison of full-bridge DC-DC converter with half-bridge DC-DC converter types on the biases of high power and voltage is explained in [72]. The main focus is on high voltage IGBT when used in full-bridge and film capacitor when used in half-bridge. The result shows that a full bridge will significantly reduce the switching loss while in half-bridge, more controllability and protection are achieved.

Power electronic transformer with improved efficiency and power factor has been introduced in [73]. The converter used in this topology is, boost DC-DC converter to reduce the harmonic performing active power factor correction. To get high performance in DC-DC converter an isolated switch in introduce in the boost converter. There is also a change in PWM at the output by some additional logics. The simulation result shows that this design has achieved high efficiency and power performance. This topology used variable hysteresis control for which it has to be run on variable switching frequency which results in distortion at input current.

A design in which a combined full-wave inverter, with converters at both sides of the transformer, is suggested [74]. At input PWM based converter is used, and acts as a low pass filter. The output converter used in this design is a matrix converter, and it's based on space vector PWM aim to eliminate harmonics produced at the output. The main advantage of this design is that it uses less number of converters as compare to other topologies. Also, there is no DC-link capacitor used in the design. The purpose of this is to get better power factor correction. As this design is based on space vector modulation, so more switching devices are required as compared to conventional PWM.

SST performance analysis which is based on the modular converter so that losses due to conduction, will be minimized [75]. For this, a dual active bridge along with a full-bridge inverter is used. The topology used includes a multi-level cascade H-bridge at the converter end, and DAB is at the DC-DC stage. A table with a

manufacturing design condition is compared with hypothetical values and tries to make the algorithm that finds the lowest conduction losses at every stage.

Introduce PWM inverter with neutral point clamped, and it compares with three other inverters [76]. The experimental result shows that NPC PWM inverter has less number of harmonic and has improved in performance and efficiency. It also suggests that there is a need to remove 11^{th} and 13^{th} harmonic contact. NPC PWM technique uses in series phase shift multiple inverters to eliminate these harmonics.
For the medium-voltage converter used in SST, the three levels NPC converter is the best possible solution [77]. The design consists of three stages of SST, which are AC-DC (medium level voltage), DC-DC (galvanic isolation), and DC-AC (Low-level voltage) converters. This multi-level voltage, methodologies are used with a medium-level voltage range.
In this design at the AC-DC converter stage flying capacitors are replaced by neutral point clamped (three levels).

A full-bridge is used to maintain the AC voltage, while in DC-DC converter half-bridge is used to reduce the output voltage. To reduce the switching losses, two methods are proposed, and their result is compared, these are Dual active bridge and series resonant converter. And the result shows that DAB, when used in multi-level voltages, has advantages over SRC. This three-level DAB, when used with half-bridge, will result in high DC gain. The proposed design is more complicated when compared to a conventional transformer.

An improved design of high-frequency transformer with DC-DC converters is in series with the input and parallel with output for SST [78]. The main purpose of this design is to overcomer switch losses when SST is operated at high frequency. For this Phase shift, half-bridge is used along with zero voltage switching.

Another advantage of this design is that it has bidirectional power flow. To make it more energy-efficient adaptive inductor is used in PSDHB. The overall design has low current stress, high power density, less core and winding losses, and less switching losses.

A new technique to design the SST, which is based on a non-linear 2Fuzzy neutral system is presented [79]. This research mainly focused on different stages (3 stages) of SST, which includes their control parameters, of its input, isolation, and output stages. For this type 2 and type 1 fuzzy neutral system used along with a PI controller is used. The design is then simulated, and the result shows that more stable performance when this design is used with SST, because of its ability to perform much better in an environment when there is a disturbance in input and output stages as well as uncertainties.

The sliding mode control method to enhance SST performance is presented in [80]. To do this design is proposed, which has DC-link so that current and voltage on primary and secondary sides can be controlled by using PWM. When this design is compared with other design which uses PI controller and linear quadratic regulator, results shows that the power factor correction, stability, and overall dynamic performance of SST has improved when it's used with SMC. Also, the result indicates that SMC is far faster than the PI controller and LQR. When compared with the PI controller and LQR, SMC is challenging to implement.

Detail advantages of using a half-bridge DC-DC converter when used with the single-phase inverter explained [81]. The main advantage of HBD is to provide the required isolation between source and load. Another benefit of using HBD is that is used less number to devices, so result reduces in size of the converter and also reduce the switches loses. In other HBD leading cause of the problem is capacitor voltage fluctuation, which is overcome by using a phase shift control method (by controlling switching timing).

A theoretical model of a variable inductor with a double E type core is explained [82]. The model structure is in the way that there is no mutual coupling between the main transformer winding and the variable inductor. The main scope of this research is that, to make a variable inductor in a way that is can control the current and later used as a resonant inductor when operated at high frequency.

A prototype design for medium frequency SST in which leakage inductance of the transformer is reduced is introduced [83]. It's also explained the methodology

which does not depend on the dimension of the core. Detail Litz wire transformer, and try to eliminate losses by reducing the diameter as well as numbers of stands in winding; aiming to occupy the space in insulation is introduced [84]. To do this method is introducing that finds the best possible solution to reduce the eddy current losses. This needs the trade-off between DC resistance and space in insulation.

Detail principles of the DAB model when they are in steady-state as well as proposed the design based on how the converter able to control the reactive current and switching of power devices is introduced [85]. With this model, one can easily determine the switching frequency and phase shift that occur in bridges. The model is based on non-reactive elements, first-order dynamics, and has low switching losses.

2.1.4 DC-AC Inverter Stage

A new technique and design model to control PWM inverter are presented in [86]. The proposed design controls the zero steady-state output voltage error by controlling the output voltage of the controller. The design is based on a digital resonant circuit which has minimum or no losses.

Boost DC-AC inverter design strategy is introduced in [87]. The design consists of two boost inverters. The proposed design follows the double loop regulation scheme, which controls the boost converts. The experimental result shows that the proposed design is not only fast and more reliable but has not much effect on the source and load variations.

An improved technique of switch-mode bidirectional DC-AC inverter in terms of performance is introduced in [88]. The configuration used in this technique is based on a buck converter. In this technique to get better performance, non-linear control is combined with a bidirectional power circuit. The proposed inverter stabilized its output voltage if variation appears at input voltage and output current. The

other advantage of this inverter is to reduce the distortion that occurs at the zero-crossing point.

A new methodology for full-bridge DC-AC inverter is introduced in [89]. In this methodology, the full-bridge inverter output voltage is controlled by connecting the switch at the lower arm of the full-bridge switch. This is done the increasing or decreasing output voltage of the bride at the lower arm; which is controlled by the switch at the lower arm of the full-bridge that controls the inverter output. At the output of inverter a pure sinusoidal waveform is obtained; which is done by operating the inverter with switching square wave and controlling the lower arm of a switch by applying the sinusoidal PWM signal. The experimental result shows that the inverter has less THD.

A proposed methodology to control the DC-AC inverter frequency, which is based on the sliding mode control technique is introduced in [90]. In this technique for power converter switching devices, a three-phase load is used based on SMC design. The design overcome two significant issues that are appearing in SMC to improve efficiency and minimizing the heat losses of the entire system. To overcome the power dissipation in the power converter, the hysteresis loop switching frequency is minimized. To improve the efficiency of system hysteresis loop switching frequency width is limited at admissible value.

An inverter design is proposed for photovoltaic modules [91]. In this design, a small film capacitor is used instead of a large electrolytic capacitor to improve the lifetime of an inverter. The design also improved in circuitry, controllability, and power processing. The inverter has two stages for power processing which are DC-DC and DC-AC. One used for removal voltage ripple due to high DC bus and boost PV panel voltage dual active bridge is used. To inject the sinusoidal current into the grid 2nd stage is used. To control the DC bus high ripples, the feed-forward controller is also presented.

Design issues of DC-DC converter when used to drive the inverter is introduced in [92]. The proposed design overcome these issues which appear due to the higher switching frequency of the inverter as compared to the DC-DC DAB converter;

and PI controller limitations due to its low switching frequency. To overcome these limitations, two designs are presented without adding a large DC bus capacitor. One of them uses inverter information of feed-forward and bandstop filter, while the second uses the resonant controller in a feedback loop. The experimental result shows that both designs have reduced the ripples generation and improves the power factor.

A prototype design of Cuk inverter based on the sliding mode control technique to replace buck base SMPS is presented in [93]. The design has improved the closed-loop design version of the classic Cuk inverter, which very difficult to design and control, needs large capacitors, and has stability issues. Cuk inverter based on the sliding mode control technique enables the passive element selection using only one reference signal state while considering the ripple and reliability conditions. As a result, a small and reliable capacitor can be used.

A new technique of grid-tie inverter is presented in [94]. In this technique, SST has to stages for a photovoltaic system. To get the maximum power point tracking for PV cell DHB converter used at the first stage. The second stage to get a sinusoidal current waveform at an output and for steady DC bus voltage, a grid-tie inverter is used.

A design and control strategies of isolated grid-tie PV inverter is proposed in [95]. The design is based on a structure that is pre-level high-frequency isolation, due to which DC-DC converter efficiency increased and size reduction. This converter includes the Cuk circuit, full and flies back half-bridge, and included forward transformation. The inverter used the MOs tube instead of IGBT to control the PWM signal and because of higher sampling and switching frequency, which helps to eliminate output ripple current. The deadbeat control method is used in inverter design instead of a PI controller, which provides better dynamic performance.

A design that overcomes the effects of input current distortion produce at the output of SST is proposed in [96]. The method of a control system is such a way that the current loop has a faster response than the voltage control loop. The design control system is based on a current and voltage control loop that uses

the PI controller that controls the current of an active rectifier and produces the output voltage closed to a reference value. The value of PI has no set value as it depends on the connected plant. Therefore values of both will be selected to requirements.

A detailed three-level PWM inverter and propose the method to reduce the common-mode voltage that by PWM inverter is explained in [97]. This method follows the space vector and switches state relationships and improved the common-mode voltage. An improved vector reference is generated, which is combined with zero and medium voltage vector, along with an advanced space vector modulation scheme.

A prototype of the double loop regulation system to control the boost inverters is introduced in [98]. In this control, the strategy has an inductor current loop which acts as an inner loop, and output voltage control act as an outer loop. To handle the variable operational point of boost inverter both inner and outer loop includes many compensations, and overcome the disturbances produced by inner as well as outer loop, attain high performance, and handle other transient conditions. To get a higher performance boost, inverters are also included feed-forward regulation. The result shows that the proposed system is far better than sliding mode control; SMC can't handle transient conditions.

2.2 Problem Statement

The literature review suggests that the researchers have mostly concentrated on the designs of individual stages of SST, and missing a collective work required to demonstrate the whole SST design and analysis. In previous literature, a lack of intentions has also been given to the harmonic reduction strategies.

In this thesis, the design and analysis of a three-phase 11 kV/415V, 100 kVA SST operated at 20 kHz frequency, has been presented for the electric power distribution system. Shunt active power filter is used to improve the stability and reduce the THD, along with multistage dual active bridge (DAB) converters and sinusoidal

pulse width modulation (SPWM) inverter. A mathematical model of SST has also been developed, based on analytical calculations, and has been implemented in MATLAB as well.

2.3 Research Methodology

The above-cited challenges have been resolved in this thesis. The main issues associated with a conventional power transformer are its enormous size and harmonic content. To reduce the size of the transformer the design of a medium frequency transformer has been developed, in which the core material, core losses, winding characteristics, efficiency and temperature of the transformer are considered. All of these parameters have also been utilized in the simulations.

For harmonic mitigation, the shunt active power filter technique is employed, shunt active power filter has two main parts reference current generation and current injection. For reference current generation instantaneous reactive power theory is used, due to its accuracy and simplicity. For current injection hysteresis current controller is used.

The three-stage solid-state transform has been taken under consideration due to flexibility in design and the chance of performance improvement at all stages. For simulation verification, Matlab software has been used.

Chapter 3

Solid-State Transformer : SST

3.1 Introduction

In this chapter three-stage, SST and its mathematical model are discussed in detail. The three-stages are AC-DC, DC-DC and DC-AC stages respectively. The first stage is AC-DC rectifier stage, in which controlled rectifier is used. AC-DC rectifier acts as a non-linear load and distorts the sinusoidal shape of source current, caused harmonic in the system. therefore, Active power filter techniques are used to mitigate the harmonics which are discussed in chapter 4. In the second stage is a DC-DC converter in which DAB is used. DAB consists of three parts. In the first part, DC-AC PWM inverter is used, in second stage MFT is used and in the third and final part, AC-DC rectifier is used. In the third and final stage of SST, and DC-AC low-frequency inverter is used.

This chapter is divided into four parts. The first part is based on a mathematical model of SST. In which voltage and current equations of SST are defines. The second part is AC-DC controlled rectifier which is also called the input stage of SST, the third part is the DC-DC converter which is also called the isolation stage, the third stage is the most important stage in which transformer design is done using different equations and in the final part is DC-AC inverter which is also called output stage of SST.

3.2 Mathematical Model Of SST : Part 1

To evaluate the mathematical model of SST, three-stage SST considers, with first stage act as an input stage in which a rectifier is used, seconds stage act as isolation and third stage act as an output stage, in which an inverter is used.
Circuit diagram of three-phase three-stage SST is shown in figure 3.1 [79, 80, 99].

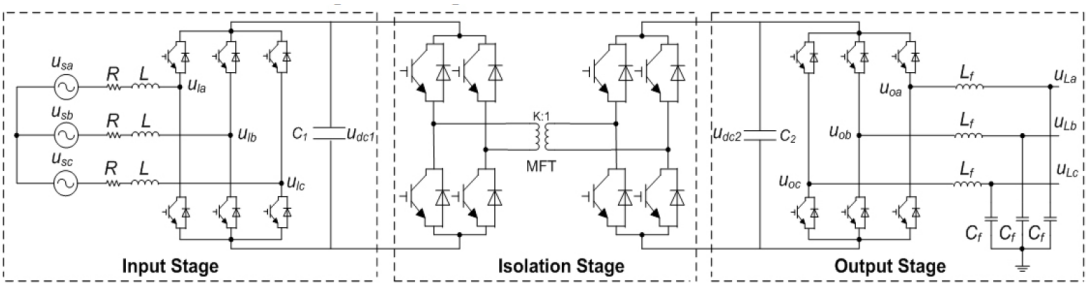

FIGURE 3.1: Circuit Diagram Of The Three-Phase Three-Stage SST [80].

In the first stage, three-phase supply voltage (11 kV) is converted into equivalent DC voltage.
The second stage isolation stage in which DAB is used, in which two brides are used at both primary and secondary side of MFT. At the primary side of MFT, the DC voltage obtained from the input stage is transformed into medium frequency square wave. At the secondary of MFT, a rectifier is used, that convert the medium frequency square wave into equivalent DC voltage.
In the third and final stage an inverter is used, that converter medium frequency DC voltage into low-frequency AC voltage.

The voltage equations of three state SST are given in 3.1-3.3 [79, 80, 99] can be written by using a simplified form of a three-phase solid-state circuit diagram as shown in figure 3.2

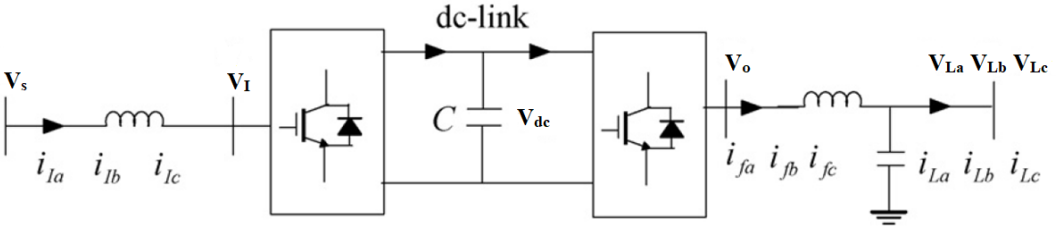

FIGURE 3.2: Simplified Form Of A Three-Phase Solid-State Circuit Diagram.

$$\begin{bmatrix} V_a(t) \\ V_b(t) \\ V_c(t) \end{bmatrix} = \sqrt{2}V_s \begin{bmatrix} \sin\omega t \\ \sin(\omega t - 120) \\ \sin(\omega t + 120) \end{bmatrix} \tag{3.1}$$

$$\begin{bmatrix} V_{la}(t) \\ V_{lb}(t) \\ V_{lc}(t) \end{bmatrix} = m_1 V_{dc} \begin{bmatrix} \sin(\omega t - \theta_1) \\ \sin(\omega t - 120 - \theta_1) \\ \sin(\omega t + 120 - \theta_1) \end{bmatrix} \tag{3.2}$$

$$\begin{bmatrix} V_{oa}(t) \\ V_{ob}(t) \\ V_{oc}(t) \end{bmatrix} = m_2 V_{dc} \begin{bmatrix} \sin(\omega t - \theta_2) \\ \sin(\omega t - 120 - \theta_2) \\ \sin(\omega t + 120 - \theta_2) \end{bmatrix} \tag{3.3}$$

The above equations are transformed into the differential equations are given below

$$L\frac{d}{dt}\begin{bmatrix} i_{la}(t) \\ i_{lb}(t) \\ i_{lc}(t) \end{bmatrix} = \begin{bmatrix} V_{sa}(t) \\ V_{sb}(t) \\ V_{sc}(t) \end{bmatrix} - \begin{bmatrix} V_{la}(t) \\ V_{lb}(t) \\ V_{lc}(t) \end{bmatrix} - R\begin{bmatrix} i_{la}(t) \\ i_{lb}(t) \\ i_{lc}(t) \end{bmatrix} \tag{3.4}$$

$$L_f\frac{d}{dt}\begin{bmatrix} i_{fa}(t) \\ i_{fb}(t) \\ i_{fc}(t) \end{bmatrix} = \frac{1}{k}\begin{bmatrix} V_{oa}(t) \\ V_{ob}(t) \\ V_{oc}(t) \end{bmatrix} - \begin{bmatrix} V_{La}(t) \\ V_{Lb}(t) \\ V_{Lc}(t) \end{bmatrix} \tag{3.5}$$

$$C_f\frac{d}{dt}\begin{bmatrix} V_{La}(t) \\ V_{Lb}(t) \\ V_{Lc}(t) \end{bmatrix} = \begin{bmatrix} i_{fa}(t) \\ i_{fb}(t) \\ i_{fc}(t) \end{bmatrix} - \begin{bmatrix} i_{La}(t) \\ i_{Lb}(t) \\ i_{Lc}(t) \end{bmatrix} \tag{3.6}$$

$$\frac{d}{dt}(\frac{1}{2}C_{dc}^2(t)) = \begin{bmatrix} V_{la}(t) & V_{lb}(t) & V_{lc}(t) \end{bmatrix} \begin{bmatrix} i_{la}(t) \\ i_{lb}(t) \\ i_{lc}(t) \end{bmatrix} - \frac{1}{k} \begin{bmatrix} V_{oa}(t) & V_{ob}(t) & V_{oc}(t) \end{bmatrix} \begin{bmatrix} i_{fa}(t) \\ i_{fb}(t) \\ i_{fc}(t) \end{bmatrix} \tag{3.7}$$

Where,

V_a, V_b, and V_c are supply voltages.

V_{La}, V_{Lb} and V_{Lc} are output voltages.

V_{oa}, V_{ob}, and V_{oc} output stage voltages.

V_{la}, V_{lb} and V_{lc} are input stage voltages.

V_{dc} input state dc voltage

m_1 and m_2 exhibit the amplitude modulating indexes of PWM rectifier and inverter respectively.

θ_1 and θ_2 are modulation angles of PWM rectifier and inverter respectively.

All the above equations are in a stationary reference frame and exhibit dynamic model. To attain the time-invariant equations, these equations are needed to transform into a rotating reference frame. Which can be done by using Park transformation. Which are given by equations 3.8-3.13 [79, 80, 99].

$$\frac{d}{dt} \begin{bmatrix} i_{ld}(t) \\ i_{lq}(t) \end{bmatrix} = -\frac{R}{L} \begin{bmatrix} i_{ld} \\ i_{lq} \end{bmatrix} - \omega \begin{bmatrix} i_{ld} \\ -i_{lq} \end{bmatrix} + \frac{m_1}{L} V_{dc} \begin{bmatrix} \sin\theta_1 \\ \cos\theta_1 \end{bmatrix} + \frac{\sqrt{2}}{L} \begin{bmatrix} 0 \\ V_s \end{bmatrix} \tag{3.8}$$

$$\frac{d}{dt} \begin{bmatrix} V_{dc} \end{bmatrix} = \frac{3m_1}{2C} \begin{bmatrix} i_{ld} \sin\theta_1 \\ -i_{lq} \cos\theta_1 \end{bmatrix} + \frac{3m_2}{2kC} \begin{bmatrix} i_{fd} \sin\theta_2 \\ -i_{fq} \cos\theta_2 \end{bmatrix} \tag{3.9}$$

$$\frac{d}{dt} \begin{bmatrix} V_{Ld} \\ V_{Lq} \end{bmatrix} = \frac{1}{C_f} \begin{bmatrix} i_{fd} \\ i_{fq} \end{bmatrix} - \frac{1}{C_f} \begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} - \omega \begin{bmatrix} V_{Ld} \\ -V_{Lq} \end{bmatrix} \tag{3.10}$$

$$\frac{d}{dt}\begin{bmatrix} i_{fd} \\ i_{fq} \end{bmatrix} = \omega \begin{bmatrix} -i_{fq} \\ i_{fd} \end{bmatrix} + \frac{m_2 \sin\theta_2}{kL_f} \begin{bmatrix} -V_{dc} \\ V_{dc} \end{bmatrix} - \frac{1}{L_f} \begin{bmatrix} V_{Ld} \\ V_{Lq} \end{bmatrix} \tag{3.11}$$

$$\left[[i_{ld} \quad i_{lq} \quad i_{lo}]^T \right] = \left[K[i_{la} \quad i_{lb} \quad i_{lc}]^T [i_{fd} \quad i_{fq} \quad i_{fo}]^T \right] = \left[K[i_{fa} \quad i_{fb} \quad i_{fc}]^T \right] \tag{3.12}$$

$$\left[[i_{Ld} \quad i_{Lq} \quad i_{Lo}]^T \right] = \left[K[i_{La} \quad i_{Lb} \quad i_{Lc}]^T [V_{Ld} \quad V_{Lq} \quad V_{Lo}]^T \right] = \left[K[V_{La} \quad V_{Lb} \quad V_{Lc}]^T \right] \tag{3.13}$$

To represent the Parks transformation equation, the equation is symbolized as K as given in equation 3.14.

$$K = \frac{2}{3} \begin{bmatrix} \cos\omega t & \cos(\omega t - 120) & \cos(\omega t + 120) \\ \sin\omega t & \sin(\omega t - 120) & \sin(\omega t + 120) \\ \frac{3}{2} & \frac{3}{2} & \frac{3}{2} \end{bmatrix} \tag{3.14}$$

3.3 AC-DC Controlled Rectifier : Part 2

The first stage of SST is three-phase high voltage and low frequency AC-DC rectifier. The circuit diagram of AC-DC rectifier is shown in figure 3.3 [100].

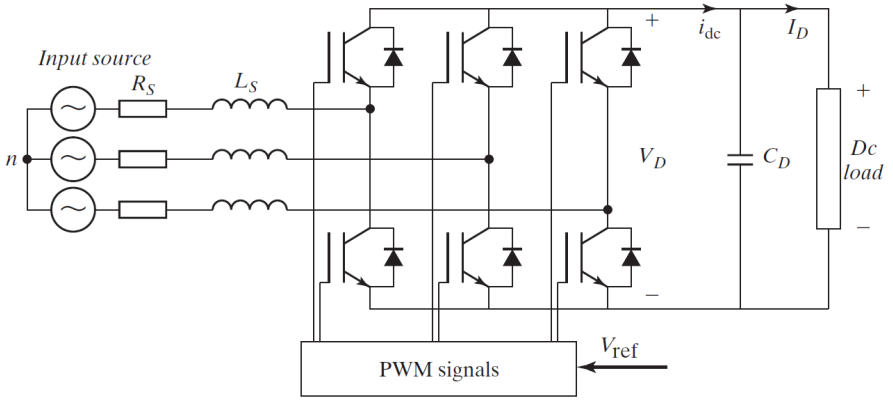

FIGURE 3.3: AC-DC Rectifier Circuit Diagram [100].

The dc-link voltage is maintained at the desired reference value by using a feedback control loop. It is measured and compared with a reference V_{ref}. The error signal switches ON and OFF the six switching devices of the rectifier. The power flow from and to the AC source can be controlled according to the dc-link voltage requirements. The voltage V_D is measured at the dc-side capacitor C_D. Controlling the dc-link voltage so that the current flow is reversed at the dc-link can control the power reversal.

In the rectifier mode of operation, the current ID is positive, and the capacitor C_D is discharged through the dc load, and the error signal demands the control circuit for more power from the AC supply. The control circuit takes the power from the supply by generating the appropriate PWM signals for the switching devices. More current flows from the AC to the DC side, and the capacitor voltage is recovered.

In the inverter mode of operation, I_D becomes negative and the capacitor C_D is overcharged. The error signal demands the control to discharge the capacitor and return power to the AC mains.

Due to this, the current waveforms try to maintain the sinusoidal, that result in reducing the harmonics in the system.

3.4 DC-DC Converter : Part 3

The DC-DC converter must provide the highest possible efficiency, which can only be possible by efficiently handling the energy transfer. Such DC-DC converter must also be able to provide soft-switching without adding any auxiliary components, bi-directional power from input to output and there should be a need for a transformer either motivated by a need for galvanic isolation or if there's a high conversion ratio required, so that the transformer helps to utilize the semiconductor devices better.

All these can be achieved by using a Dual active bridge which briefly explains in this chapter along with a medium frequency transformer (MFT).

The MFT (frequency ranges from 1 to 100 kHz) [39], which is part of the DC-DC converter will help to achieve the main advantage, by reducing the core size, which eventually reduces the overall volume of a transformer.

3.5 Dual Active Bridge (DAB): Design Challenge

The converter must be capable of providing galvanic isolation between the input and output states through a medium-frequency transformer with the required voltage conversion ratio as per the application. The converter must also operate at high efficiency through inherent soft-switching methods like zero voltage switching (ZVS) or zero current switching (ZCS), via input and output with or without the requirement of additional parasitic components.

In the DAB, two full bridges are connected by a medium frequency transformer, as shown in figure 3.4. All switches operate at a constant duty ratio of 50%. The modulation of the switches produces medium-frequency square waves across the primary and the secondary. These square waves are phase-shifted concerning each other. This leads to power transfer from the leading leg to the lagging leg, depending on the phase of the bridges.

The transformer provides the required galvanic isolation and the voltage conversion ratio. The major advantage of this topology is that due to natural lagging current in one of the bridges, the inductor stored energy passes zero voltage switching of the lagging bridge switches and some switches of the leading bridge during the dead time of the switches without any additional passing components [101–107].

One of the essential parameters of DAB is the transformer turns ratio. The turns ratio is selected according to the application. In this design, the transformer turns ratio is chosen to step down an AC voltage from 10 kV to 450 V,which gives us a factor 23:1.

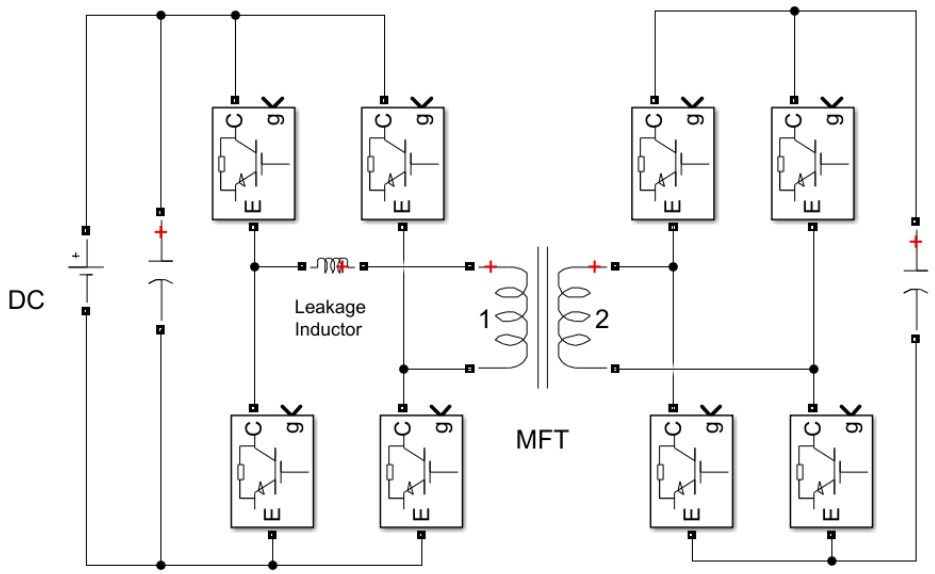

FIGURE 3.4: DAB Circuit Diagram.

3.6 Medium Frequency Transformer

Transformer design considerations should be explored to attain the high performance and power density that is desirable in the SST and to control difficulties in operating at Medium frequencies. Therefore, the core theme of this chapter provides design considerations for medium transformers to lay the foundations for a transformer design method.

To achieve the above goal, this chapter describes the properties of the magnetic core that determines the core material selection criteria, and the analysis of the transformer windings under medium-frequency effects that lead to recommendations for wire selection..

3.6.1 Magnetic Core Properties

The choice of the core material has vital importance for the construction of the transformer, as this affects costs, efficiency, performance, and volume [108–110]. Therefore, it is essential to understand magnetic material properties. For a particular application, in general, four properties of core material are considered. These

are core loss density, relative permeability, saturation flux density, and Curie temperature [111, 112]. Amorphous, Ferrite, Nano-crystalline, and Silicon steel are the core magnetic materials that are generally considered for medium frequency, high power transformers [25, 109, 111, 112].

Comparisons of selected magnetic materials concerning the above properties are listed in Table 3.1 [108, 109].

TABLE 3.1: Magnetic Material Properties Comparison

Properties	Amorphous	Ferrite	Nano-crystalline	Silicon steel
Core loss density (W/kg)	<40	<418	<48	<4400
Relative permeability	10-150 k	2 k	20 k	16 k
Saturation flux density (T)	1.56	0.47	1.2	1.53
Curie temperature(°C)	399	220	600	730

The amorphous material has earned great significance in higher-frequency, high-performance applications, mostly because of its high saturation flux density (1.56 T), reasonable cost, and also a much lower core loss density compared to standard silicon steel. Amorphous material, therefore, offers a right balance between cost, efficiency, and power density [25, 110–112].

Due to relatively low cost and core loss density, in medium-frequency applications, the most commonly used magnetic material is Ferrite. Still, it has one draw bag, which is its low saturation flux density nearly equal to 0.4 T [113]. Therefore when used for high-performance applications, Ferrite material based transformers become heavy and bulky.

In high-performance applications, Standard silicon steel material (SSM) is quite suitable due to its high saturation flux density approximately equal to 1.5 T, high Curie temperature, and increased permeability [25, 114]. The major disadvantage of SSM is its high-density core losses during operation at high frequencies due to eddy current losses.

When comparing the efficiency and power density, the Nano-crystalline material exhibits the best performance, due to its high saturation flux density (1.2 T)

along with the lowest core loss density [114]. However, Nano-crystalline material has significantly high costs. Besides, the standard form of Nano-crystalline core is toroidal tape-wound which limits the design of the transformer [111, 112].

In conclusion, cores made of amorphous or Nano-crystalline material are best suited for the SST applications. Though, the ultimate choice is determined on the criteria of the designer when cogitating the compromise between cost, efficiency, performance, and volume.

3.6.2 Core Losses In Transformer

In Magnetic material, core losses are generally included hysteresis losses and eddy current losses [112]. The reorientation of magnetic domains associated with hysteresis loss. When on magnetic material, a magnetic field Intensity H is applied; it follows the route (1) in figure 3.4 Till it reach the saturation flux density B_{sat}.

The magnetic material will follow the route (2) when the field decreases. Magnetic material maintains a small portion of the magnetization when the field becomes zero, known as remanence flux density B_r. To bring the flux density to zero a coercive field, H_c has to be applied. The material saturates again (in the opposite direction) if the field continues to rise in a negative direction. In this case, the material will follow the route (3) and closes the hysteresis loop.

In magnetic material energy is required to reorient the domains, whenever a magnetic field changes direction [108, 112, 115]. This energy results as a hysteresis loss, which is proportional to the hysteresis loop area shown in figure 3.5.

Eddy current loss is another type of core loss that occurs in the magnetic core due to the induced voltage, in a similar manner as voltage induced through the windings, as described by the Faraday law. Reduce the losses due to eddy current, the responsible paths for the current flow through the core should be minimized [115]. To do so, laminations are employed for the magnetic core, which reduced the current's path (1).

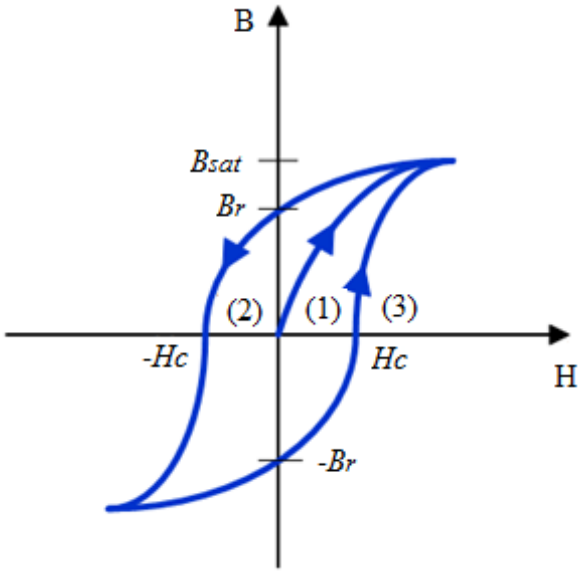

FIGURE 3.5: Hysteresis Loss [112].

3.7 Medium-Frequency Effects In Transformer Windings

Winding loss is generally because of the DC resistance related to the windings [108, 109]. Effects of medium frequency in the winding, which are the leading cause of AC loss, consist of skin effects and the proximity effect as depicted in figure 3.5, and are discussed in this section. The skin effect and the proximity effect lead to an increase in the losses in the conductors due to the non-uniform current distribution in the conductors. These effects are a direct consequence of Faraday's law, according to which eddy currents are induced to oppose the flux generated by alternating currents in the windings.

The DC resistance R_{dc} of windings associated with a particular conductor carrying either a direct current or an alternating current having low frequency can be evaluated as follow.

$$R_{dc} = \frac{N\rho MLT}{A_w} \tag{3.15}$$

Where the area of the conductor is represented by A_w, while the mean length of turn is denoted by MLT, the number of turns of the winding is represented

by N and ρ signifies the conductor's specific resistance, therefore to calculate the winding loss,R_{dc}, and square of current are multiplied.

Generally, to calculate the losses in a winding, the DC resistance of the conductor is taken into account. Due to current flows only in the circumference of the wire and not over the entire surface of the conductor which results in increases in resistance of the conductor at high frequency. Hence, the conductor's effective area decreases; consequently, the AC resistance R_{AC} ascends [116].

This phenomenon is called the skin effect illustrated in figure 3.6.

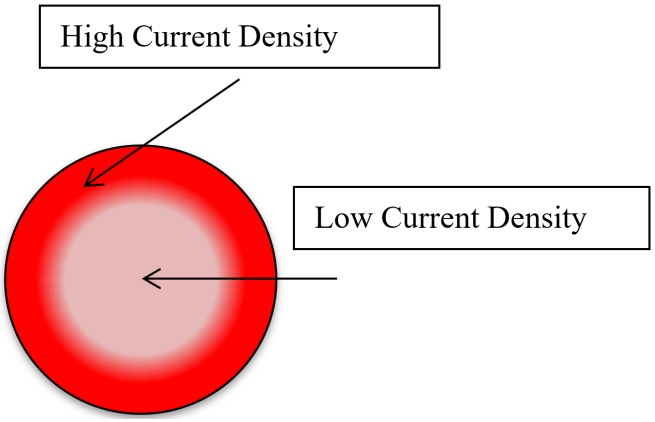

FIGURE 3.6: Skin Effect.

In the case of skin effect, the term skin depth (symbol) can be defined as equivalent conductors thickness having resistance equals to that of a solid conductor under skin effect. Skin depth can be calculated with the help of the given formula [108, 109, 116].

$$\delta = \frac{1}{\sqrt{\pi f \mu_o \sigma}} \tag{3.16}$$

Whereas;

f = Operating frequency
σ = Specific conductivity of the conductor material
μ_o = Permeability of the free space

The skin effect is associated with the individual/single a conductor; high-frequency effects arise when there are multiple intertwined conductors.

This phenomenon is regarded as the proximity effect, as demonstrated in figure 3.7. Resistance to alternating current ascends due to the interaction among the opposite conductor's magnetic field, which is near with each other (i.e. the flow of current is in the opposite direction). Such interaction results in the confinement of each conductor are current into a smaller region.

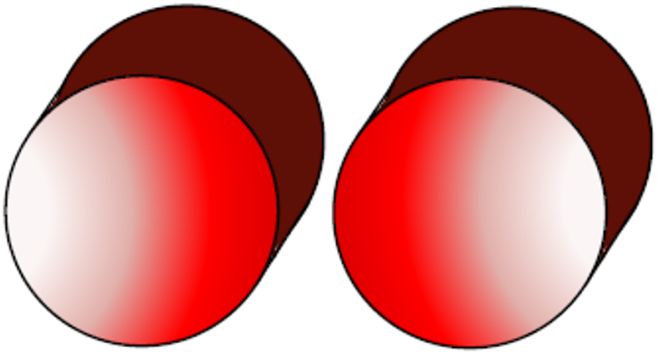

FIGURE 3.7: Proximity Effect.

To minimize the skin effect as well as the proximity associated with the windings, generally, stranded wires having insulated conductors are utilized, which is referred to as the Litz wire [108, 109].

This suggests the adoption of the foil plates for the same purpose, but such a technique may not be the best option regarding medium-performance applications because the plate's width may be too big [116]. Therefore, the Litz wire is strictly recommended for the SST's applications.

TABLE 3.2: Skin Depth Of Copper Litz Wire For Different Frequencies

Frequency	Skin depth (δ) (mm)
10 kHz	0.66
20 kHz	0.46
50 kHz	0.30
100 kHz	0.21

Table 3.2 shows the skin depth values at different frequencies, from the table it is clear that at high-frequency skin depth is decreased, so the frequency selection is very critical as the components selection at the higher frequencies become different.

3.8 Design Methodology

3.8.1 Medium Frequency Transformer Design Methodology

One of the main components of an SST is medium-frequency transformers. To get maximum efficiency and power density from the transformer, a few requirements must be considered while designing a transformer [117–121]. In this section, the basic methodology of the transformer will be presented.

3.8.1.1 System Specification

The first step of the MF design methodology is to specify the system specifications. I.e. Primary and secondary voltages, Output power, expected efficiency, temperature rise, duty cycle, and operating frequency. In this thesis, the proposed design as the following specifications given in the table.

TABLE 3.3: System Specification

Parameter	Value
Primary Voltage	15 kV
Secondary Voltage	450 V
Output power	100 kVA
Expected efficiency	98%
Temperature rise (ΔT)	70^{o}C
Duty cycle (D)	50%
Frequency (f)	20 kHz

3.8.1.2 Material Properties

For the selection of the core material, specific properties of the material illustrated in chapter 3 must be taken under consideration. Based on the core materials, saturation flux density (B_{sat}) as well as the coefficients K, alpha, beta (Steinmetz coefficients) is taken according to the data advised by the manufacturers.

3.8.1.3 Flux Density Optimization

One of the most important properties related to the MF transformers for SST is the high efficiency, because the overall system losses, contrasting a conventional transformer, including losses in the transformer and losses in the power converter. Therefore, the design process of the transformer should be accompanied by criteria for optimizing the flux density, as described in [108].

There are two principles regarding the optimization criteria; the core loss (p_{cu}) and the winding loss (p_{fe}). The losses in the winding as given by the following equation are inversely proportional to the associated flux density B as well as the square of the frequency.

$$p_{cu} \propto \frac{1}{f^2 B^2} \tag{3.17}$$

And conferring to the Steinmetz equation, core losses are directly proportional to the associated flux density B and the frequency f.

$$p_{fe} \propto f^{\alpha} B^{\beta} \tag{3.18}$$

These principles are represented in figure 3.8.

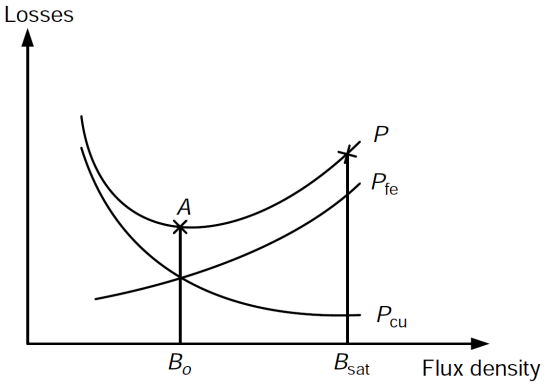

FIGURE 3.8: Flux Density Vs Losses [108].

Based on the above data, optimum flux density (B_o) can be found by using equation 3.9 [108].

$$B_o = \left[\frac{[h_c k_\alpha \Delta T]^{\frac{2}{3}}}{2^{\frac{2}{3}}[\rho_w k_w k_u]^{\frac{1}{12}}[k_c K_c f^{\alpha}]^{\frac{7}{12}}}\right]\left[\left[\frac{K_v f k_f k_u}{\sum VA}\right]^{\frac{1}{6}}\right] \tag{3.19}$$

B_o in the core is not limited by B_{sat}; the relation between them is given in the figure 3.9. Based on this designer can change B_o to increase the power density, by keeping in view that will be effect efficiency.

Where p_{fe} is core loss, p_{cu} is winding loss and optimum design is at A, h_c is heat transfer coefficient and typically taking 10 W/m^2 ^oC, k_a, k_c, and k_w, are cores dimensional coefficients.

Generally, the dimensionless coefficient k_a, k_c, and k_w values are 40, 5.6, and 10, respectively [109, 110]. ΔT is temperature rise, K_v the waveform factor, whose value if 4.44 for a sinusoidal waveform and 4 for a square waveform [108, 110, 120], f is transformer frequency, k_f is the stacking factor, and recommend value is 0.95, the value of the window utilization factor k_u varies in between 0.2 to 0.8; however, the recommended value is taken as 0.4, ρ_w is the wire resistivity, and ΣVA is the total transformer power rating.

3.8.1.4 Core Dimensions

Based on area product A_p, core size is selected. The area product is the relationship between the cross-sectional area of a core and window area. This can be seen from the datasheet of the manufacturers

$$A_p = \left[\frac{\sqrt{2} \sum VA}{K_v f B_o k_f K_t \sqrt{k_u \Delta T}} \right]^{\frac{8}{7}} \tag{3.20}$$

Where K_t is found by using equation 3.21 [118, 121].

$$K_t = \sqrt{\frac{h_c k_\alpha}{\rho_w k_w}} \tag{3.21}$$

After calculating the A_p, the core with a larger A_p as compared to the calculated one, must be selected using the manufactures datasheet . If calculated A_p is larger than the value given in the datasheet, then to obtain the required A_p stacked cores can be used.

3.8.1.5 Winding Characteristics: Wire Size

After core selection, the designer can select wire, bare area of primary and secondary, which is based on current density j_o expression given in equation 3.22, which depends on winding temperature rise and A_p.

The influence of the medium frequency on the windings is taken into account with the Litz wire; the skin depth is therefore calculated from equation 3.23. Equation (3.22) gives the stands that the selected wire should have. Now based on this from the manufacture datasheet, a wire gauge can be selected.

$$J_o = K_t \sqrt{\frac{\Delta T}{2k_u}} \frac{1}{\sqrt{A_p}} \tag{3.22}$$

Later, the necessary strand's number along with the essential overall wire area as well as the adopted area of the strands is calculated based on the skin depth.

$$\delta = \frac{6.62}{\sqrt{f}} K \tag{3.23}$$

Where K is a coefficient of skin depth, by using the equation, the maximum area that Litz wire stands should have can be found.

$$D_{depth} = 2\delta$$

$$MaximumAllowableArea = \frac{(\pi)(D_{depth})^2}{4}$$

Primary and secondary turns can be expressed by using Faraday law as

$$N_p = \frac{V_p}{K_v B_{max} A_c f}$$

$$B_{max} = 2B_o$$

$$N_s = N_p \frac{V_s}{V_p}$$

Where A_c is the cross-section area of core.

3.8.1.6 Volume Calculation

In some cases, the priority may be to achieve a high power density; in other cases, the efficiency may be of high importance as compared to the power density.

Therefore, this calculation is important to estimate the volume of the transformer. The design engineer then able to access whether the outcome is appropriate or not. To calculate the core volume as well as the volume of the windings, the following equations can be used

$$V_c = l_m A_c$$

$$V_w = MLTw_\alpha$$

Where the mean length associated with the core is denoted by the l_m while the mean length associated with a turn is represented by MLT.

Where l_m and MLT can be found using a datasheet.

3.8.1.7 Losses Calculations

Winding or copper losses is inversely proportional to the square of flux density as well as the square of the frequency, as per equation 3.24.

$$P_{cu} = \rho_w V_w k_u \left[\frac{\Delta VA}{K_v f B_{max} k_f k_u A_p} \right] \tag{3.24}$$

Core Losses:

For core losses, the iGSE method is used [117, 118, 121], given by equations 3.25.

$$P_v = k_i |\Delta B|^\beta \frac{1}{T^\alpha} \left[D^{1-\alpha} + (1-D)^{1-\alpha} \right] \tag{3.25}$$

where k_i is found by using following equation

$$k_i = \frac{K_c}{2^{\beta-1}\pi^{\alpha-1}(1.1044 + \frac{6.8244}{\alpha+1.354})}$$

The total loss is made up of the combined core and winding losses.

3.9 Proposed Design

Proposed calculated medium frequency transformer design data (using above equations 3.15-3.25) is given in the table below.
The table shows the following specification along with their rating. All the cited specification are designed via an accurate manufacturing datasheet.

TABLE 3.4: Proposed Medium Frequency Transformer Design Parameters

Specification	**Rating/values**
Transformer power rating	100 kVA
Primary voltage (V_p)	15 kV
Secondary voltage (V_s)	450 V
Transformer frequency	20 kHz
Primary current	6 A
Secondary current	128 A
Window utilization factor	0.4
Material properties	Amorphous 2605SA1, two core stack for AMCC-1000
Wire size (Litz wire)	AWG # 18
Minimum primary Strains	5
Minimum secondary Strains	93
No. of primary turns	100
No. of secondary turns	5
Total loss (Copper + Core)	332.6158 W
Ambient temperature	30°C
Temperature rise	70°C
Efficiency	98%

3.10 DC-AC Inverter : Part 4

The third and final stage of SST is a three-phase DC-AC inverter. Ideally, the output of inverter should be sinusoidal; however, in practice, the output of the inverter is not only non-sinusoidal but also contains harmonics. For low and medium power applications square wave voltages are acceptable. While in case of higher power applications, low distorted sinusoidal voltages are desired. The square wave voltage inverter has some drawbacks i.e. the magnitude of fundamental voltage is constant and the output consists of low order harmonics. That makes them complex and expensive, as to eliminate the harmonics large size of inductor and capacitor required. Both these problems can be solved by using sinusoidal pulse width modulation or SPWM.

SPWM are easy to implement and has two major advantages. One of them is controlled output voltage magnitude and in other, harmonics are pushed around multiples of switching frequency, therefore lower harmonics are disappearing in the output voltage. Also, higher-order harmonics can be easily removed by using low size inductor and capacitor.

In this chapter brief introduction of a three-phase voltage SPWM inverter, triggered by a gate pulse along with an LC filter has been presented. The filter generates a sinusoidal three-phase voltage at the inverter output with a harmonic distortion of almost zero. In SPWM, the method involves comparing three-phase reference modulation signals with a common triangular carrier wave to generate pulses for three phases.

3.11 Pluse Width Modulation (PWM)

In PWM technology, time period modulation generates pulses with constant amplitude, but with different duty cycles. This modulation is achieved by using a reference and a carrier signal. Based on the comparator logic, the corresponding

signals are generated, when the carrier and reference signals are fed to a comparator. The output signal is the desired reference wave, which can be a square or sinusoidal wave. On the other hand, the carrier wave is usually a saw-tooth or triangle wave with a frequency considerably greater than the reference signal. To eliminate the higher-order harmonics a series inductor is used. The selected range of lower harmonics can be reduced by appropriately selecting the number of pulses per half cycle. PWM techniques are divided into three major techniques which are

- Single-pulse.
- Multiple pulse and
- Sinusoidal.

In this research, only the SPWM technique is discussed.

3.12 Sinusoidal Pulse Width Modulation (SPWM)

With sinusoidal PWM, the width of each pulse changes in proportion to the amplitude of the sinusoidal wave, which is estimated in the center of the same pulse. Which result not only reduced the distortion factor but also significantly reduce the lower order harmonics. By comparing a triangular carrier wave having frequency f_r with a sinusoidal reference wave having frequency f_c, gating signals can be generated as shown in figure 3.9. Output frequency fo of an inverter is determined by F_r, and Modulation index (Ar/Ac) can be controlled with the help of its amplitude A_r. In this way output voltage V_o(RMS) can be controlled. A comparator is used to compare the reference signalV_r (which has the desired frequency) with the high-frequency carrier V_c. The output will be low if the sine wave has a lower magnitude and will be high if the sine wave magnitude is higher. The output of the comparator is processed in the trigger pulse generator so that the output voltage waveform has a pulse width corresponding to the pulse width of the comparator.

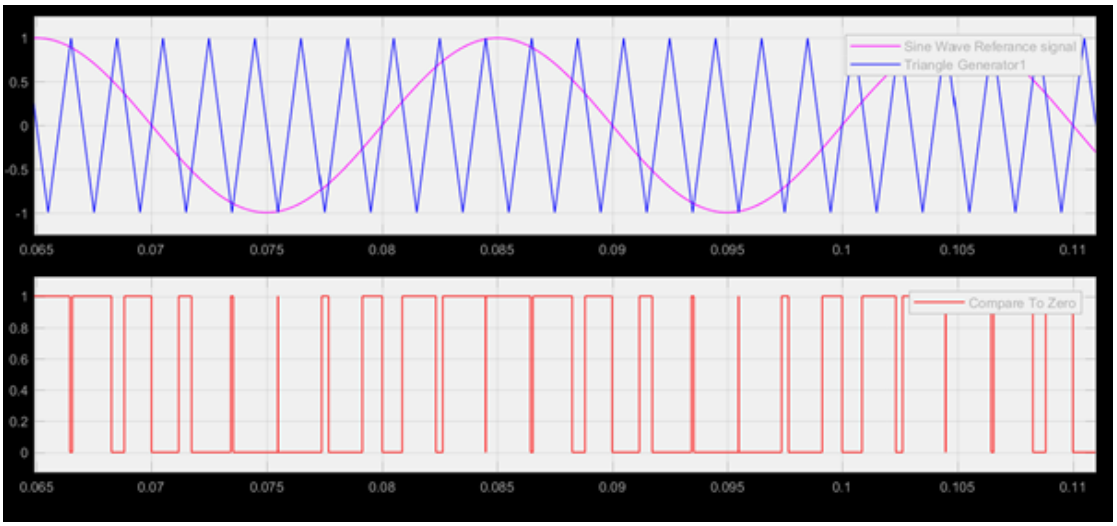

FIGURE 3.9: Sinusoidal PWM.

3.13 Switching Techniques

The inverter uses two types of switching techniques to provide gate signals to switches, one is unipolar and other is Bipolar voltage switching. A switching is said to be in unipolar control mode if the SPWM wave remains only in polar range. I.e. triangular carrier wave is in the range of +Ve or -Ve polarity. On the other hand, if the triangular carrier wave remains in between positive and negative polarity i.e. in a continuous range, then the resulting SPWM wave will be in between +Ve and Ve changes. Such a switching technique is called bipolar control.

This is shown in the figures 3.10 and 3.11.

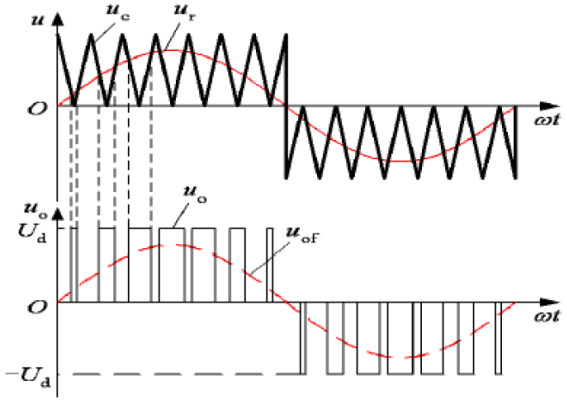

FIGURE 3.10: Uni-polar Control Technique [122].

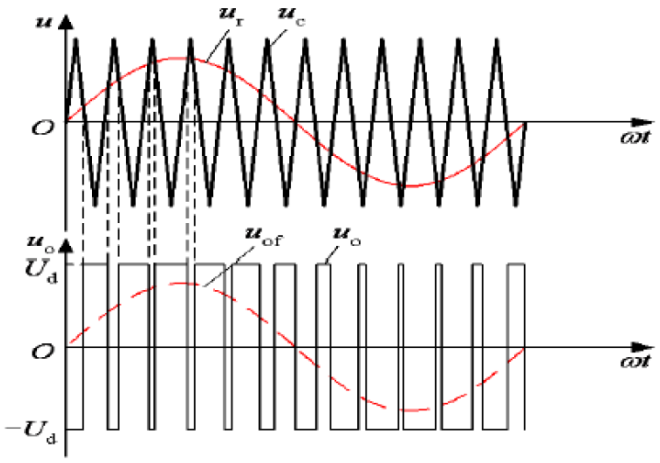

FIGURE 3.11: Bi-polar Control Technique [122].

3.14 Three-Phase Inverter: SPWM

In many industrial applications, three-phase inverters are used to deliver the variable frequency. In a three-phase inverter, SPWM deploys to control the inverter voltage. The corresponding gating signals of a three-phase inverter are illustrated in Figure 3.12. In Three-Phase SPWM the three reference sine waves (U, V, W) with compared with the triangular carrier wave, which is shifted 120^o with each other[122].

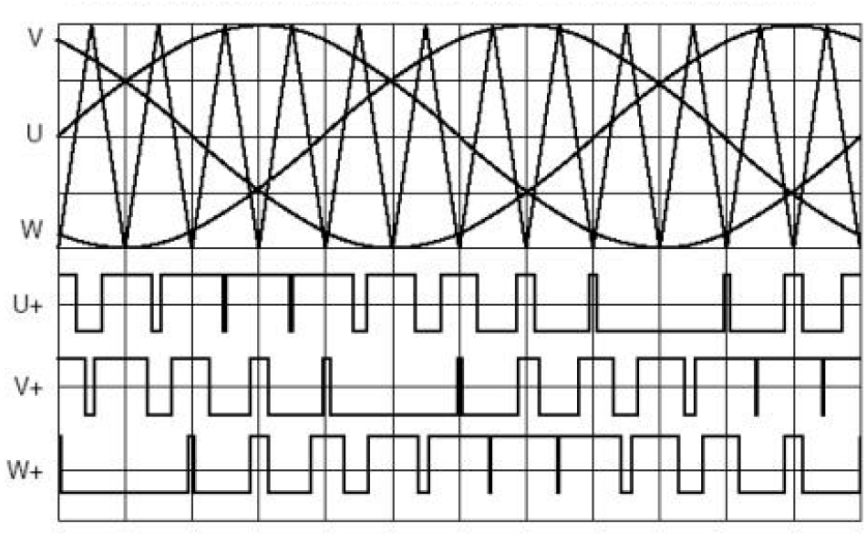

FIGURE 3.12: Switching Gate Pulses Of SPWM [122].

The Standard circuit of the three-phase inverter with six IGBTs that act as controlled switches is shown in figure 3.13. In this model, the desired output voltage

can be regulated, and the line currents can be sinusoidal with a power factor of unity.

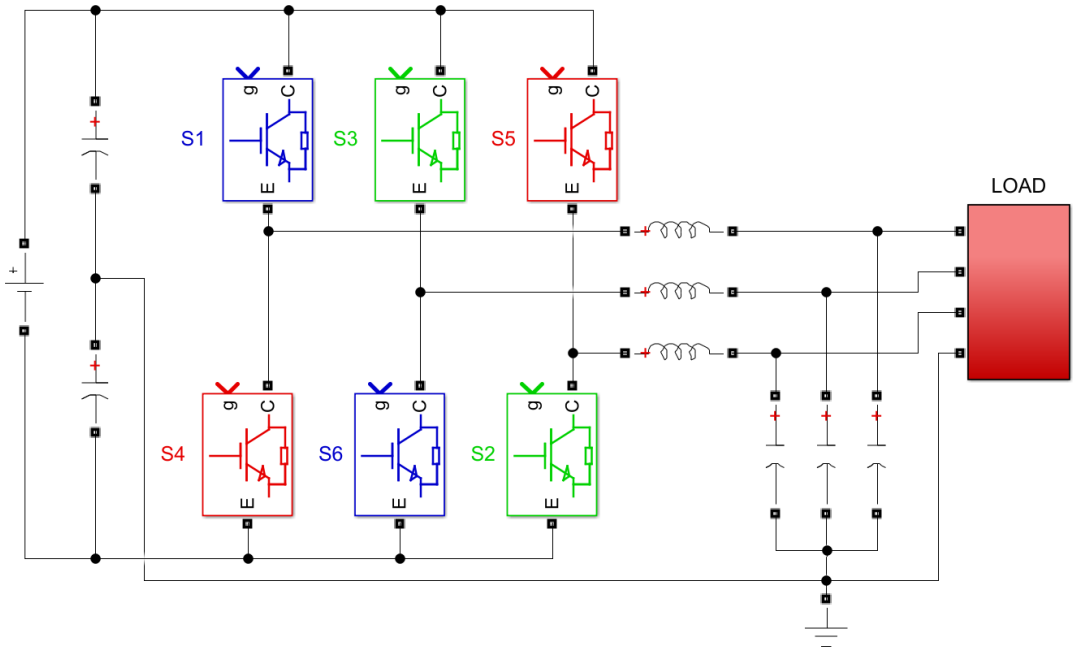

FIGURE 3.13: Three-Phase Inverter: Basic Circuit.

The inverter is fed with dc voltage (output of the second stage of an SST) and has three phase-legs each containing two IGBTs. To avoid the short circuit and undetermined line voltages and states, in each leg, the upper and lower switches cannot be closed simultaneously, so that their ON and OFF states are not same in order.

In the SPWM control, the inverter switches are controlled by comparing the sine wave and the triangle wave. The sine wave determines the desired fundamental frequency at the inverter output and the triangle wave determines the inverter switching frequency. Each transistor conducts for 180^o. At any instant of time, three of transistor remains ON. When S1 is ON, the A terminal is connected to the positive terminal of the DC supply voltage. When S4 is ON, the A terminal is connected to the negative terminal of the input voltage. There are six modes of operation and each mode operates for a period of 60^o.

Inverse gate signals of S1, S3 and S5 are made to get the gate pulses for gate pulses S4, S6 and S2 respectively. This can be achieved by adding a NOT gate after each comparator and then the resultant signal is given to the remaining three switches.

In this thesis, SPWM is implemented with 120^o mode of operation to ease the simulation. With 120^o mode of operation only the amplitude will vary without changing any other vital characteristics, therefore the inverter output waveforms will not alter much. In 120^o mode of operation, each transistor will conduct for 120^o and only two transistors will conduct simultaneously.

Chapter 4

Harmonics Mitigation And Shunt Active Power Filter

4.1 Introduction

AC-DC rectifier is the first stage of SST, which is also non-linear and leads to a higher harmonic content in the source current. Owing to these harmonics, the source current waveform gets distorted. SAPF's are utilized for modification of distorted source current via injection of a compensating current in parallel with the load current. The injected current will reshape the source current into a sinusoidal form. In this chapter, harmonics mitigation techniques are presented along with SAPF, SAPF has been achieved through instantaneous reactive power theory (p-q theory) and hysteresis current controller to generate and inject the reference current respectively, in parallel to the load. Consequently modifying the distorted source current into a sinusoidal waveform.

4.2 Harmonics Mitigation

The extensive use of power electronic converters (PEC) in the power system during the past few decades has been witnessed, due to their high efficiency, fewer losses,

small size, highly reliable, and capacity to handle the large current [123]. When these converters are used with non-linear loads, they cause harmonics in the power system due to non-sinusoidal waveform. These harmonics are the main cause of different power quality problems [124, 125]. Due to these unwanted harmonics, a large current is drawn from a system that is considered to be the major issue for the three-phase system [126]. These non-linear loads are not only causing resonance problems but also result in harmonics into the system; therefore, a mitigation solution is required to overcome these issues. Whereas many techniques are presented in [127] as a solution to these problems.

By using filters, harmonics content from the system can be reduced, different methods are available for this purpose. These filters can be a passive filter or an active filter. When passive elements are used to make the filter, then such a filter is called a passive filter (PF), i.e. the inductor and capacitors. PF does need an external power source. The main benefit of PF is its low cost; for harmonics, this filter provides the low impedance path. They can be used in many applications, such as in power distribution networks, bypassing power supply, and many more. In contrast, analogue electronic filters are mostly active filters, which are primarily being used in high voltage supply applications. While comparing the active filters with passive filters, active filters are expensive and have a complex circuit, but they possess many advantages over passive filters [128].

4.2.1 Passive Harmonic Mitigation Techniques

To reduce the harmonics content from the power systems, different passive techniques are usually implemented such as line reactors, tuned filters, and multi-pulse converter circuits. The common purpose of all these methods is to block the unwanted harmonic currents that flow into the system.

This can be achieved by either adding the high impedance in series with the path so that it can prevent the harmonic current flowing into the system, or by using

a low impedance parallel to the path, so it can divert the harmonic current flow [129].

For power factor correction, harmonics mitigation techniques use two methods to improve the performance of the system. One approach is to set a limit on the power factor value for the load; for example, many appliances have fixed power factor 0.75 lagging and 0.8 leading. In another method, absolute maximum limits are defined for the current harmonic [130].

In single and three-phase rectifiers, typically a current waveform is non-sinusoidal. The line current contains high harmonic content, subsequently, the power factor becomes low. In rectifiers, the input current is highly discontinuous due to small source reactance; therefore, the power drawn from the grid has a low power factor [131, 132].

4.3 Active Harmonic Mitigation Techniques

In active harmonic mitigation techniques, to cancel the distorted waveform, an equal and opposite voltage or current waveform is injected into a system, which results in improved power quality.

To generate such a waveform in the AC line, which cancels the effect of the original distorted waveform, the insulated gate bipolar (IGBTs) are used in active harmonics filters (AHF's). The main part of AHF is the controllers. To improve filter stability and performance, AHF uses control strategies, which have a crucial role, with the help of the controllers.

There are two types of control strategies used in AHF design. In the first method to calculate the amplitude as well as phase angle of harmonic order, the Fourier transform is used. In this method, the current waveform is generated, which has the same amplitude as the original distorted waveform but has the opposite phase angle. While the second method filter uses a controller that generates a full current

waveform that eliminates the fundamental frequency component and allows the filter to generate the waveform, which is inverse of the remaining waveform [130].

Active power filters have two significant configurations, which are series and shunt active power filters [133].

4.3.1 Shunt Active Power Filter

Shunt active power filter (SAPF) installed in parallel with the non-linear load as in figure 4.1. To eliminate the current harmonics and to make the source current waveform pure sinusoidal,i.e. free from harmonics, SAPFs are generally used in most of the power factor correction techniques. When considering the performance and functionality, SAPF is superior to the series AHF. In SAPF, only load harmonic current content is carried out, which makes SAPF more beneficial as compared to series AHF, in which full load current is carried out [133, 134].

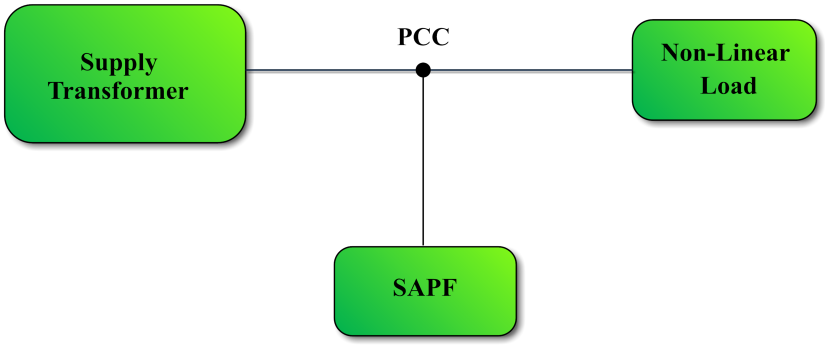

FIGURE 4.1: SAPF Basic Diagram.

4.4 Shunt Active Power Filter Working Principle

To reduce the harmonic content, a reference current is generated and injected into the system at the point of common coupling (PCC) using controlling techniques is referred as the working principle of SAPF [135]. Voltage source inverters (VSI)

that use a controller for generating the pluses are used to inject the reference current. SAPF block diagram is shown in figure 4.2.

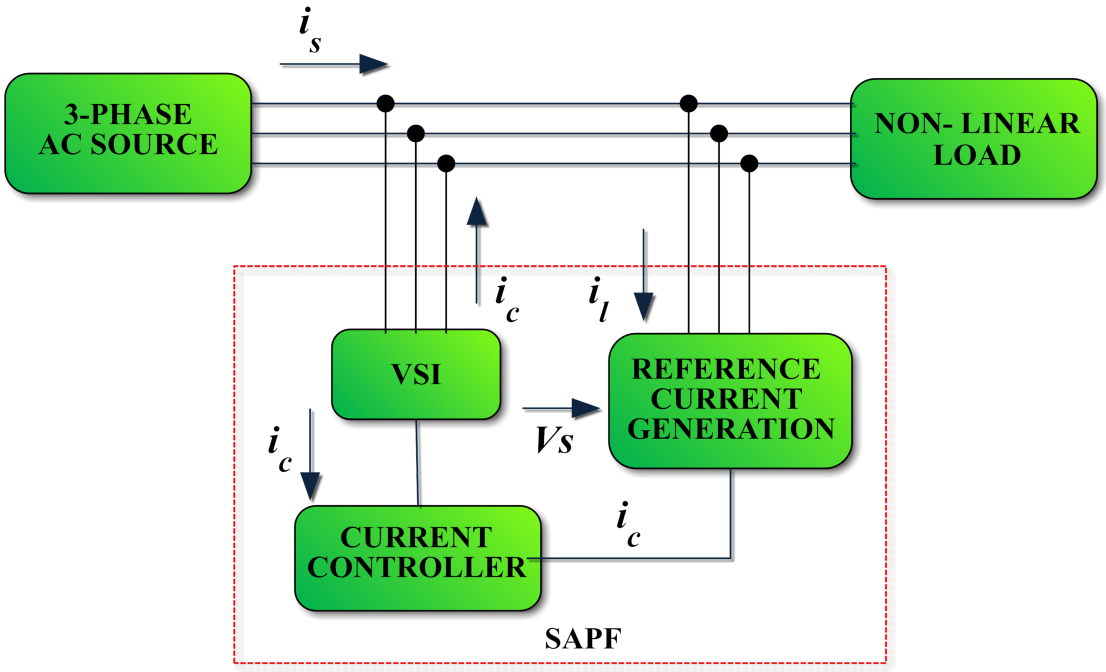

FIGURE 4.2: Shunt Active Power Filter Block Diagram.

Current generation and injection are the two main parts of active power filters (APF). To cancel the harmonic content in the load current an equal and opposite current is injected into the system in parallel. A reference current that should have a magnitude equal to harmonic current but possesses the opposite phase has to be generated first. To do so, many techniques are available in time as well as in the frequency domain. Current and voltage coordinated transformations are considered in time domain-based methods. In contrast, Fourier analysis is considered in frequency domain-based techniques.

These techniques are d-q theory, p-q theory, and discrete Fourier transformation (DFT). In d-q theory, source voltage, frequency, and phase detail are required, i.e. synchronize reference frame. While in DFT and p-q theory, frequency and phase detail are not necessary i.e. in instantaneous reactive power theory.

The first stage of APF is the generation of the reference current. After the generation of reference current, the next stage is injecting a reference current using the controller at PCC. To inject the reference current at the PCC, the controller

needs to track the reference current via generating pulses, these pulses are used to control IGBTs of VSI.

Due to this injected current, harmonics are eliminated, which results in a pure sinusoidal waveform. For precise current injection, DC link voltage regulation is required, which can be achieved with the help of a controller, that not only injects precise reference current but also helps in retaining the required level of current.

Source current i_s of SAPF can be expressed in mathematically form as in equation 4.1

$$i_s = i_c + i_l \tag{4.1}$$

In the above equation,i_l represents load current while i_c represents compensating current. By measuring total harmonic distortion (THD), Harmonics compensation ratio (HCR), and power factor (PF), APF performance can be evaluated.

The mathematical form of THD is expressed in equation 4.2 [136].

$$THD = \sqrt{\frac{I_2^2 + I_3^2 + I_4^2 + ... + I_n^2}{I_1^2}}\ x\ 100\% \tag{4.2}$$

The mathematical form of HCR is expressed in equation 4.3. [137].

$$HCR = \frac{THD\ after\ compensation}{THD\ before\ compensation}\ x\ 100\% \tag{4.3}$$

4.5 Reference Current Generation

The reference current plays an important role in SAPF. Accurate measurement of the load current confirms the precise generation of the reference current. The generation of the reference current must be performed correctly to get a good

filter performance. Reference current generation methods are generally classified as time domain and frequency domain, as shown in figure 4.3

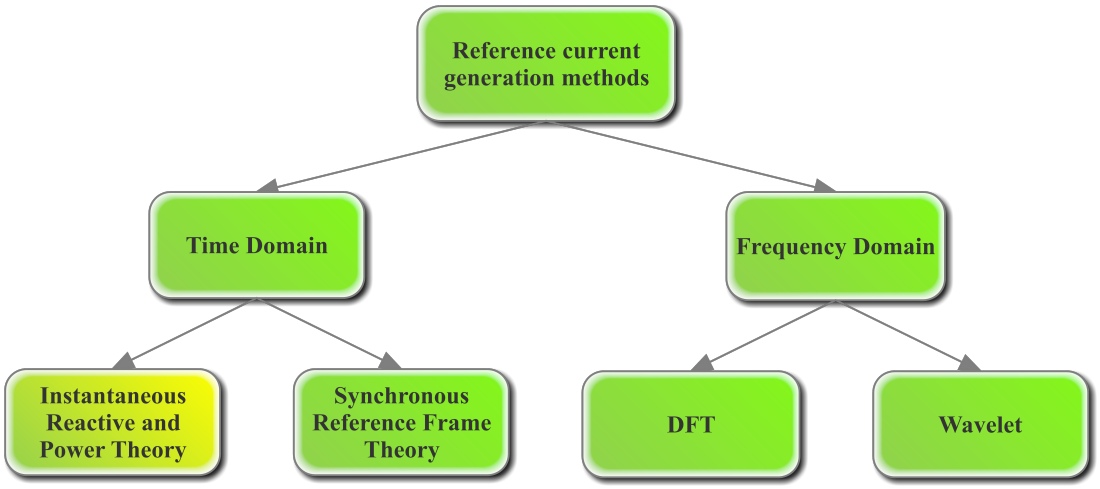

FIGURE 4.3: Generally Used Reference Current Generation Methods.

4.5.1 Instantaneous Reactive And Power Theory

The p-q theory is based on a set of instantaneous powers that are defined in the time domain. There are no restrictions on voltage or current waveform, and it can be applied to a three-phase system without neutral. It is therefore not only valid in a steady-state, but also in a transitional state. This theory is beneficial and flexible in choosing controllers to improve power quality. The block diagram of p-q is shown in the figure 4.4.

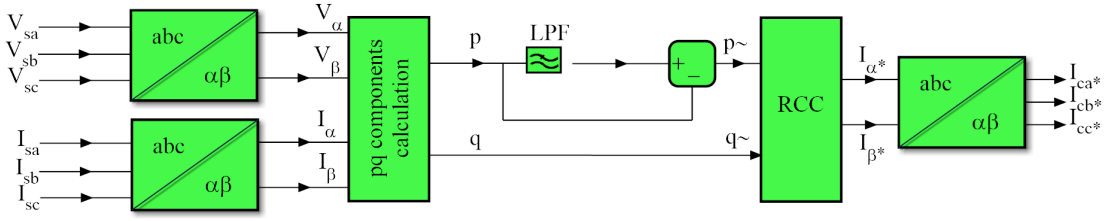

FIGURE 4.4: Block Diagram Of p-q Theory.

This theory uses the $\alpha\beta\theta$ transformation, also known as the Clark transformation, which consists of a real matrix that transforms three-phase voltages and currents into stationary reference frames $\alpha\beta\theta$ [56]. Clark's transformation, transforms the

three-phase instantaneous voltages V_{sa}, V_{sb} and V_{sc} (in the abc phase) into the instantaneous voltages V_α, V_β, and V_θ (on the axes $\alpha\beta\theta$).

The Clark transformation for three-phase instantaneous voltages are given by equation 4.4.

$$\begin{bmatrix} V_0 \\ V_\alpha \\ V_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} \tag{4.4}$$

Similarly, the Clark transformation for three-phase instantaneous currents, I_{sa}, I_{sb}, and I_{sc}, transformed on $\alpha\beta\theta$ axes is given by equation 4.5.

$$\begin{bmatrix} I_0 \\ I_\alpha \\ I_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} I_{sa} \\ I_{sb} \\ I_{sc} \end{bmatrix} \tag{4.5}$$

In a three-phase system, a zero-sequence current component does not exist. In this research, a three-phase system is considered; therefore, I_0 can be excluded from the equation, which leads to simplification and given by

$$\begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} I_{sa} \\ I_{sb} \\ I_{sc} \end{bmatrix} \tag{4.6}$$

The instantaneous power can be defined from instantaneous source voltages and currents, as in a three-phase system, zero-sequence current didn't exist, the zero-sequence power is always zero; therefore, the instantaneous power is expressed by

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} V_\alpha & V_\beta \\ V_\beta & -V_\alpha \end{bmatrix} \begin{bmatrix} I_\alpha \\ I_\beta \end{bmatrix} \tag{4.7}$$

Where p is an instantaneous real or active power, and q is instantaneous imaginary or reactive power.

This can also express in oscillating and average parts, i.e. in AC and DC parts given by

Real power:

$$p = \bar{p} + \tilde{p} \tag{4.8}$$

Where $\bar{p}$ is average part of p and $\tilde{p}$ is an oscillating part of p.

Imaginary power:

$$q = \bar{q} + \tilde{q} \tag{4.9}$$

Where $\bar{q}$ is average part of q and $\tilde{q}$ is an oscillating part of q.

To obtain constant instantaneous power from the source, the SAPF must be installed close to the non-linear load as much as possible that should compensate for the oscillating real power of this load.

Therefore, $\tilde{p}$ and $\bar{p}$ must be separated from p, which can be done by passing the active power through the LPF. The LPF and its cut-off frequency should be carefully selected. In [56], it is suggested that the fifth-order Butterworth LPF with a cut-off frequency between 20 and 100 Hz has been successfully used in practice to separate $\bar{p}$ from p.

Now the reference current can be calculated by using a given equation

$$\begin{bmatrix} I_{\alpha^*} \\ I_{\beta^*} \end{bmatrix} = \frac{1}{V_{\alpha^2} + V_{\beta^2}} \begin{bmatrix} V_\alpha & -V_\beta \\ V_\beta & V_\alpha \end{bmatrix} \begin{bmatrix} p \\ q \end{bmatrix} \tag{4.10}$$

In the final step, the reference current can be calculated in abc coordinates, by using

$$\begin{bmatrix} I_{a^*} \\ I_{b^*} \\ I_{c^*} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & 1 & 0 \\ \frac{1}{\sqrt{2}} & -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} I_0 \\ I_\alpha \\ I_\beta \end{bmatrix} \tag{4.11}$$

4.6 Current Injection Control

To make the source current sinusoidal, generated reference current should be injected precisely in parallel to the non-linear load. Therefore, the current injection controller (CIC) is one of the main parts of SAPF. The main objective of CIC is to make sure that the actual compensating current should track the reference current, which is done by generating the gate pules for voltage source inverter. Therefore, CIC must be selected very carefully, as it significantly affects the SAPF performance. In this research, the hysteresis current controller technique is used for current injection, due to its simplicity and accuracy. Another parameter that must be considered while designing SAPF is DC-link voltage control.

4.6.1 DC-link Voltage Control

A voltage source inverter (VSI) and DC-link capacitor are often used to design the SAPF power stage. The main advantage of VSI-based SAPFs is its capacitive energy storage, which is a more effective, smaller, and less expensive solution. The primary function of the DC-link capacitor is to act as a constant DC storage for the inverter, to generate an injection current to the source current. A suitable DC link capacitor voltage should be more than two-thirds of the mains voltage to ensure that the correct injection current is generated. In this thesis, Proportional-Integral Control (PI) technology is used to regulate the voltage of the DC-link by comparing the actual voltage of the DC link with the reference level, thus creating an error that is processed by the PI controller. This concept is shown in the figure. To regulate and maintain the constant voltage of the DC-link capacitor, it is necessary to control the active power. Injection currents can only be generated accurately if the voltage in the DC-link in the SAPF is maintained at the required reference level, which results in improving the performance of SAPF. This small amount of active current is controlled by the PI controller, and then this current is regulated by the current regulator to maintain a constant voltage across the DC-link capacitor. For this purpose, the actual voltage of the DC-link

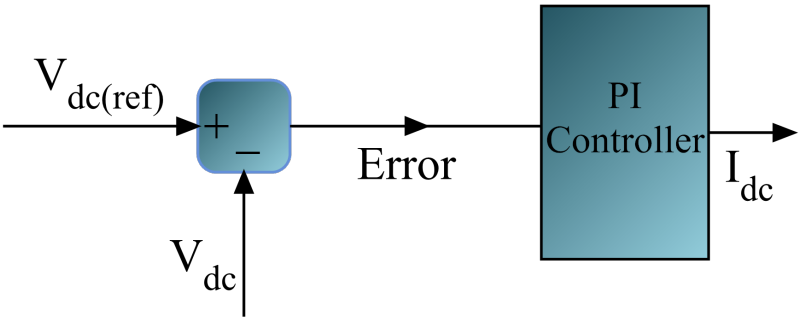

FIGURE 4.5: DC-link Voltage Control.

is sensed and fed to the PI controller together with the reference voltage of the DC link. Therefore, the magnitude of the reference current generated must be set accordingly by controlling the I_{dc}known as the instantaneous DC charging current. The I_{dc}value results from the difference between the actual DC link voltage and the desired reference value so that the SAPF can draw an accurate amount of active power to compensate for its potential losses. Based on this method, the voltage error E, which results from the difference between the V_{dc} and V_{dc}(ref.), is controlled directly by the PI controller to approximate the value of I_{dc}.

To maintain a power balance in which the active power of the power supply should be the sum of the active load power and the inverter losses. The active power consumed by the SAPF throughout the switching process must be controlled to regulate the DC-link voltage. Thus, the active power consumed by the SAPF is made equal to the switching loss to complete the regulation process. In this process, the magnitude of the reference current is adjusted so that the SAPF can draw an accurate amount of active power to compensate for its potential losses.

4.6.2 Hysteresis Current Control

In SAPF Hysteresis current control (HCC), is the most commonly used method for current injection. HHC method offers the advantages of simplicity, good accuracy, reliability, and fast dynamic behaviour. The basic concept of HHC is shown in the figure 4.6. As in this research, a three-phase system is considered; therefore, this method should be applied separately for each phase. This method is used

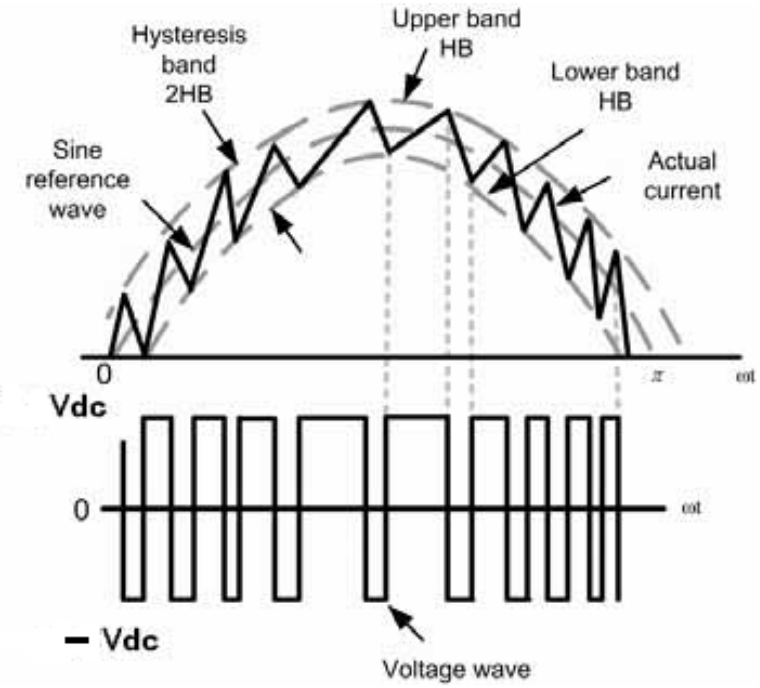

FIGURE 4.6: Basic Concept Of Hysteresis Current Control[49] .

to control VSI, in a way that the generated output current follows a reference current. This is done by limiting the actual current within a fixed hysteresis band. Therefore to restrict the actual current, two limits that are evenly shifted from the reference are set. To generate inverter switching pulses, a fixed hysteresis band is set with upper and lower limits and compared with the current error signal. The hysteresis controller detects an error between the actual current and the reference current and compares it with the assigned band, which generates the gate signals from the VSI.

It also noted that a short circuit might appear across the voltage supply of DC-link. Therefore simultaneously ON and OFF of switches of VSI should not be allowed. If the actual current remains within band limits, then there are no switching pulses required for an inverter. Whenever the actual current increases as compared to the reference current and the upper band limit is reaches than the current should decrease and if the actual current decreases and the lower limit of the band are reaches than the current need to be increased. So that current remains within the fixed hysteresis band.

AC-DC converter is the first stage of SST, which makes the load non-linear. Therefore, the source current gets distorted. To overcome this problem the SAPF technique is used. In which firstly, the reference current is generated, and then injected parallel to the load thus to make the distorted source current sinusoidal. To generate the reference current p-q theory is used, while for injection of reference current hysteresis current controller is used. The simulation results of these techniques are shown in chapter 6.

Chapter 5

Simulation Results

5.1 Introduction

To evaluate the performance of the proposed design, the design was simulated by using MATLAB/SIMULINK. Simulations have been done with and without using the SAPF, and their results have been compared too. A balanced load and a three-phase wire system are used for simulation. The performance of SAPF is also evaluated by calculating the source current THD.

A complete model of the SST has been shown in figure 5.1(a).

In figure 5.1(a), the three-phase 11 kV grid AC voltage is applied with 50 Hz frequency.

Before 1^{st} stage AC-DC rectifier, a SAPF in installed in parallel which helps to remove the unwanted harmonics, present due to non-linear load.

The output of the 1^{st} stage AC-DC rectifier is DC voltage approximately equal to 14200 V. The 2^{nd} stage is DC-DC converter as shown in figure 5.1(b) and 5.1(c), in which three modules of DAB are used.

Equation 4.11 is used to estimate the core loss of the transformer. To verify this estimated result, open circuit transformer test in Simulink has been done, and the

values of magnetization, inductance and resistance have been calculated which are later on implemented in the Simulink model of the transformer. The combined output voltage of DC-DC Converter is approximately 419 V.

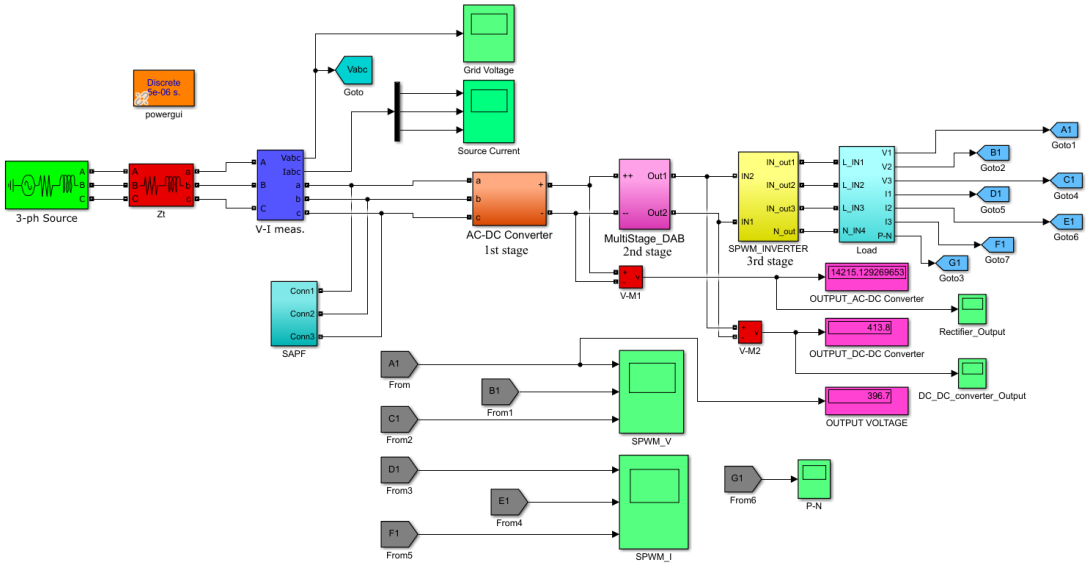

Figure 5.1a: Simulink Model Of SST.

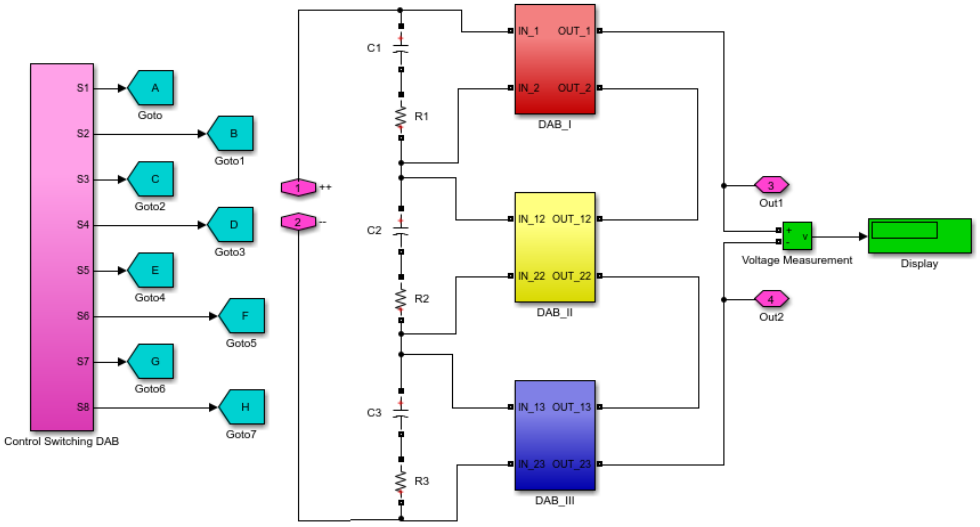

Figure 5.1b: Multi-Stage DAB Converter.

Finally, in the last stage, as shown in figure 5.1(d), the output of three-phase DC-AC inverter is approximately 396 V, which is within the range permissible to the consumer end voltages i.e. 380-415 V.

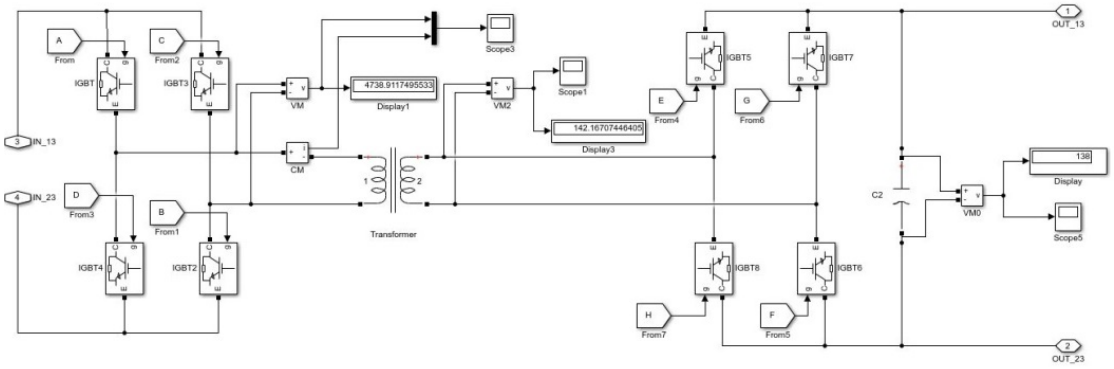

Figure 5.1c: Circuit Diagram Of DAB-I Converter.

A pulse signal in SPWM methodology (control switching) is generated by comparing a sinusoidal reference signal with a triangular carrier signal.

When the reference sinusoidal signal becomes greater than the carrier triangular wave, the switching devices will turn ON.

Sinusoidal reference signal has a phase difference of 120^o relative to each other.

The switching gate pulse is generated when the sinusoidal reference signal (U, V, and W) intersects triangular wave, the control switching circuit diagram is shown in figure 5.1(e).

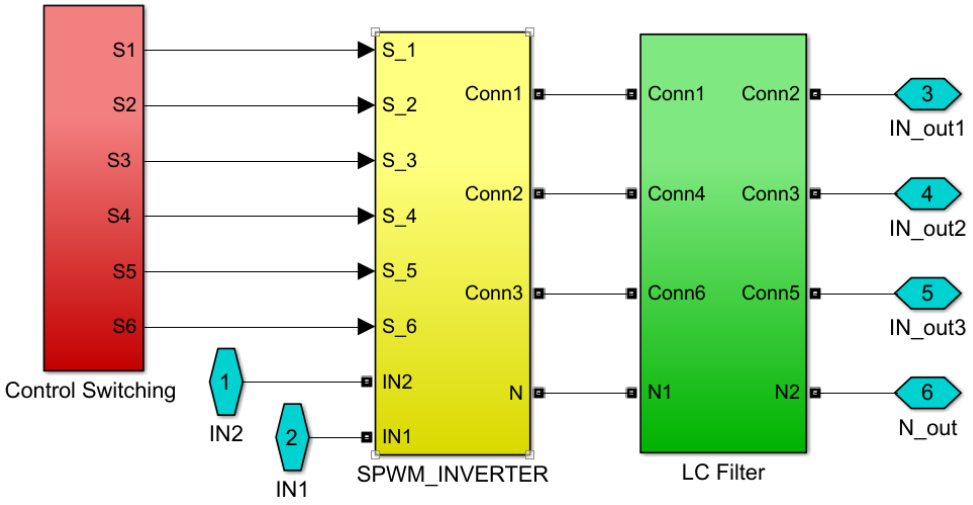

Figure 5.1d: SPWM Inverter With LC Filter.

Overall, the simulation results have verified the proposed design.

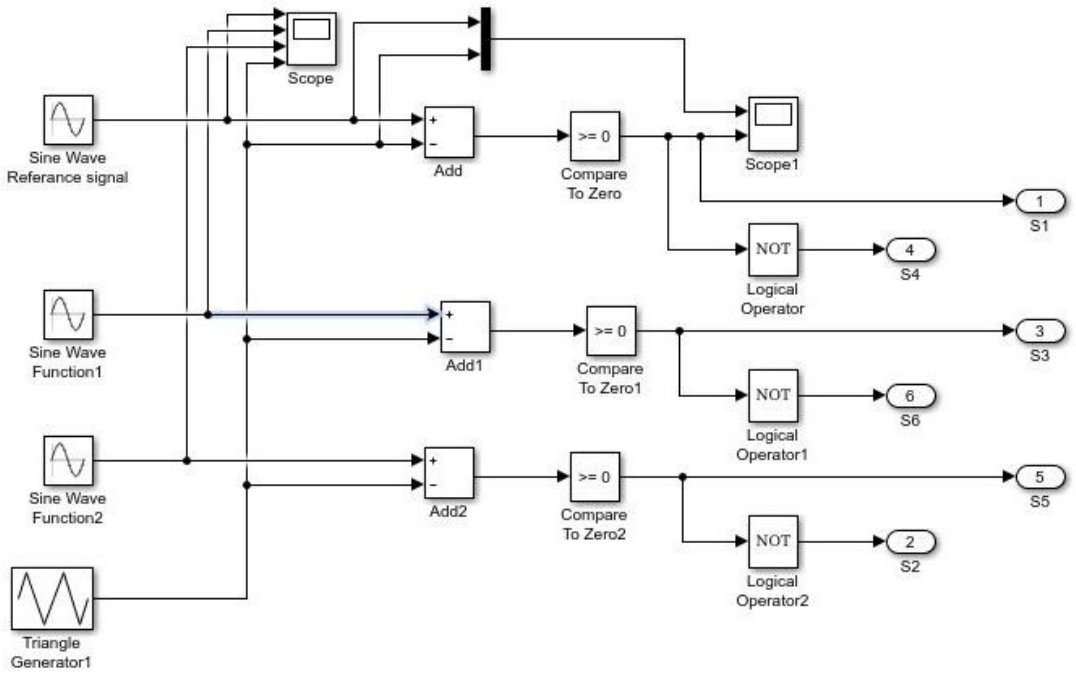

Figure 5.1e: Control Switching Circuit Diagram.

When the system was simulated without using the SAPF technique, THD of source current was found to be 130.09%, as shown in figure 5.2(a), while the load current results are shown in figure 5.2(b).

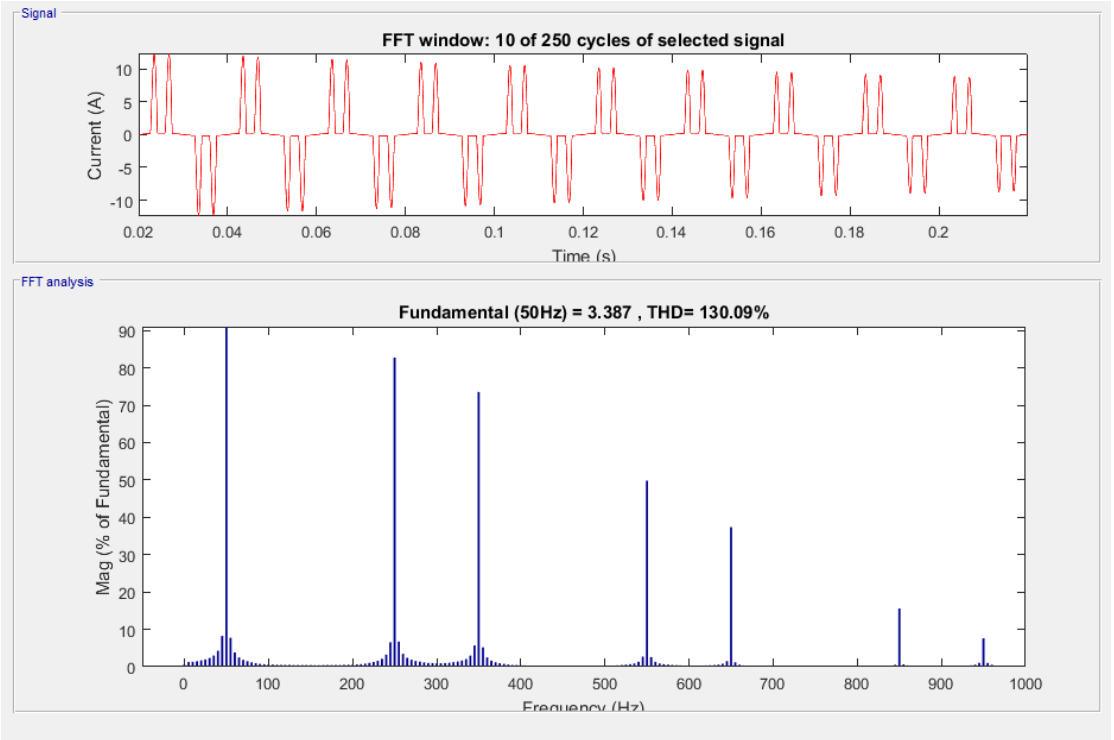

Figure 5.2a: THD of Source Current Without Using SAPF.

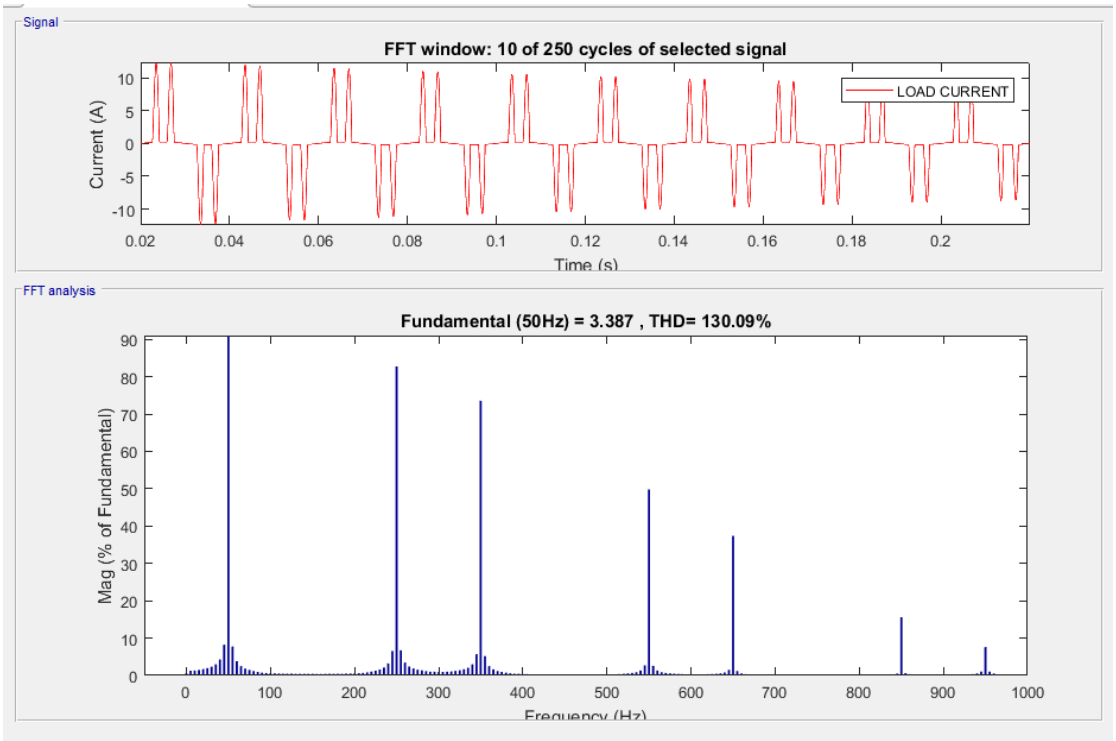

Figure 5.2b: THD Of Load Current Without Using SAPF.

Similarly, the same system, when simulated using the SAPF technique, the THD of source current was reduced to 1.20%, as shown in figure 5.2(c).

The result depicts a significant improvement in THD as well as in the efficiency of the system, consequently, verifies our model of SAPF.

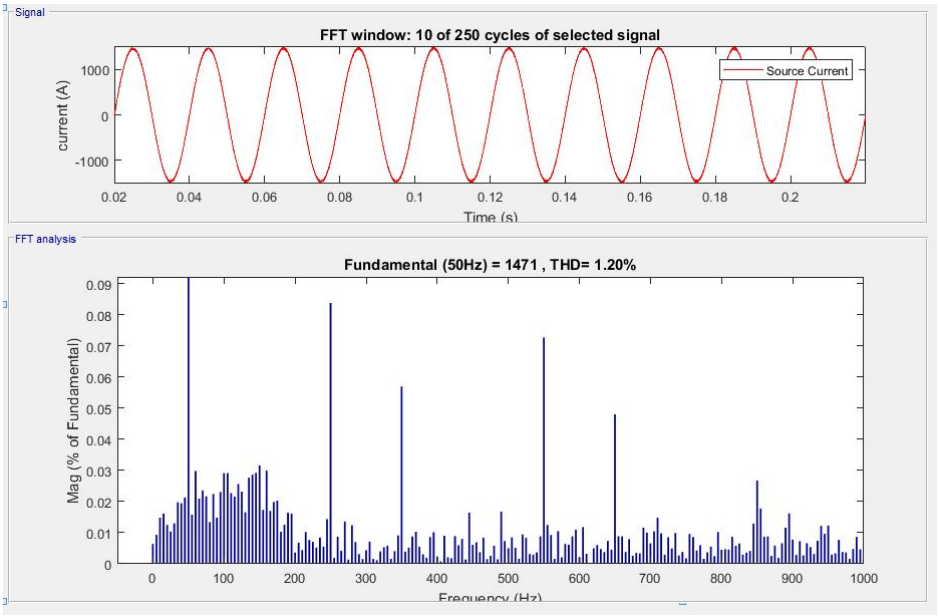

Figure 5.2c: THD Of Source Current With SAPF.

Simulation results of the proposed SST design at various stages using SAPF have also been illustrated. The supply voltage and current of Phase A, at the grid side, are shown in figures 5.3 and 5.4 respectively.

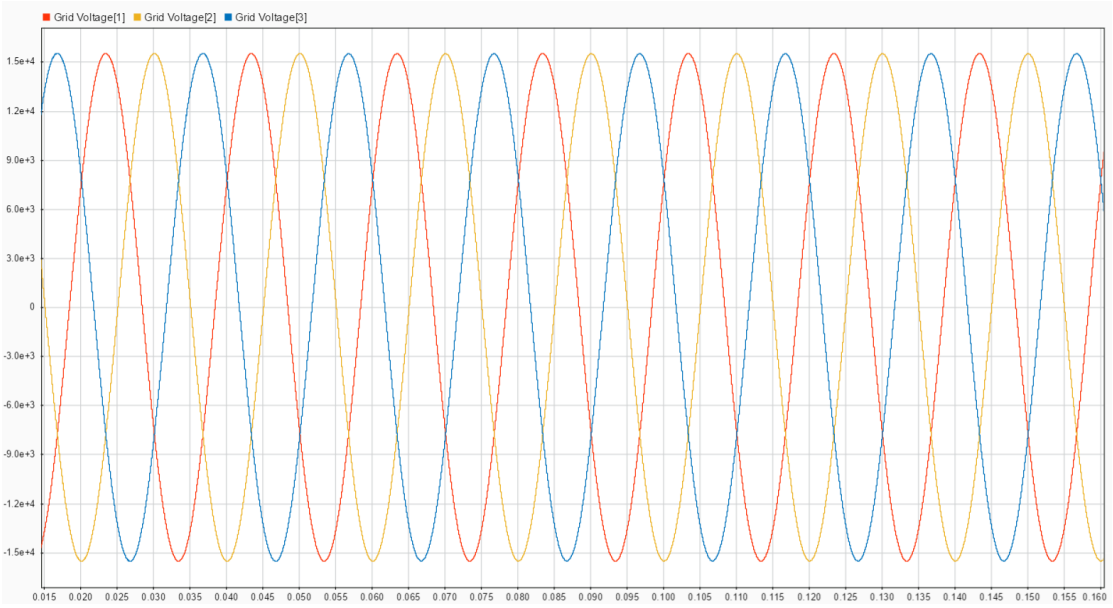

FIGURE 5.3: Supply Voltage On The Grid Side (11 kV, 50 Hz).

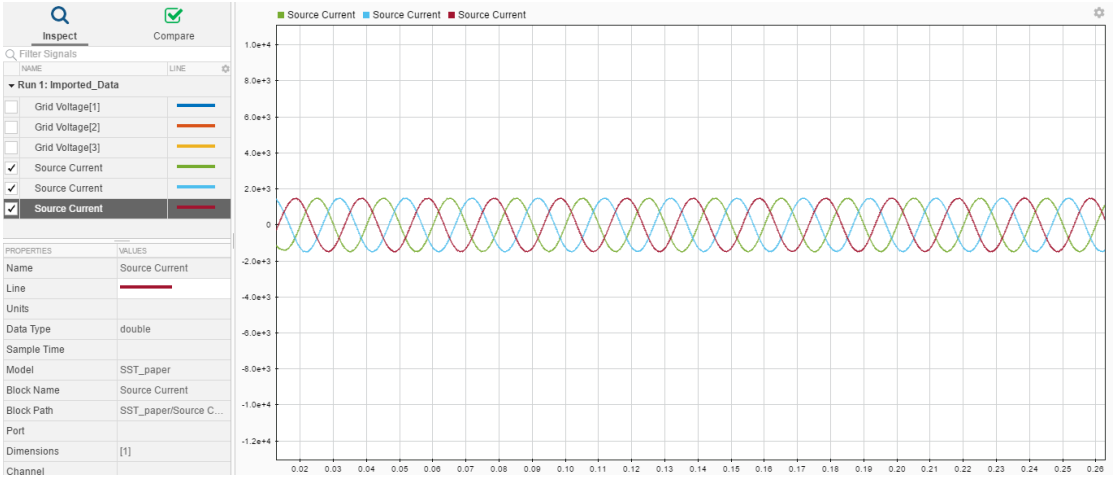

FIGURE 5.4: Source Current On The Grid Side.

From figure 5.5, it is clear that both voltage and current at the grid side are in phase.

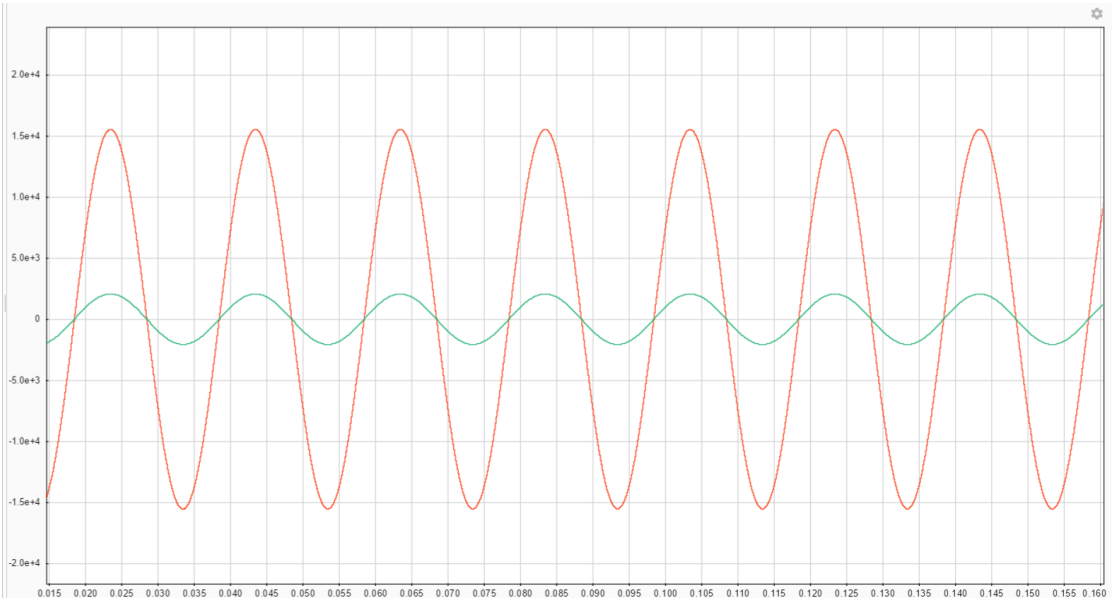

FIGURE 5.5: Source Voltage And Current Of Phase A At The Grid Side.

SAPF implementation in Simulink is shown in figure 5.6.

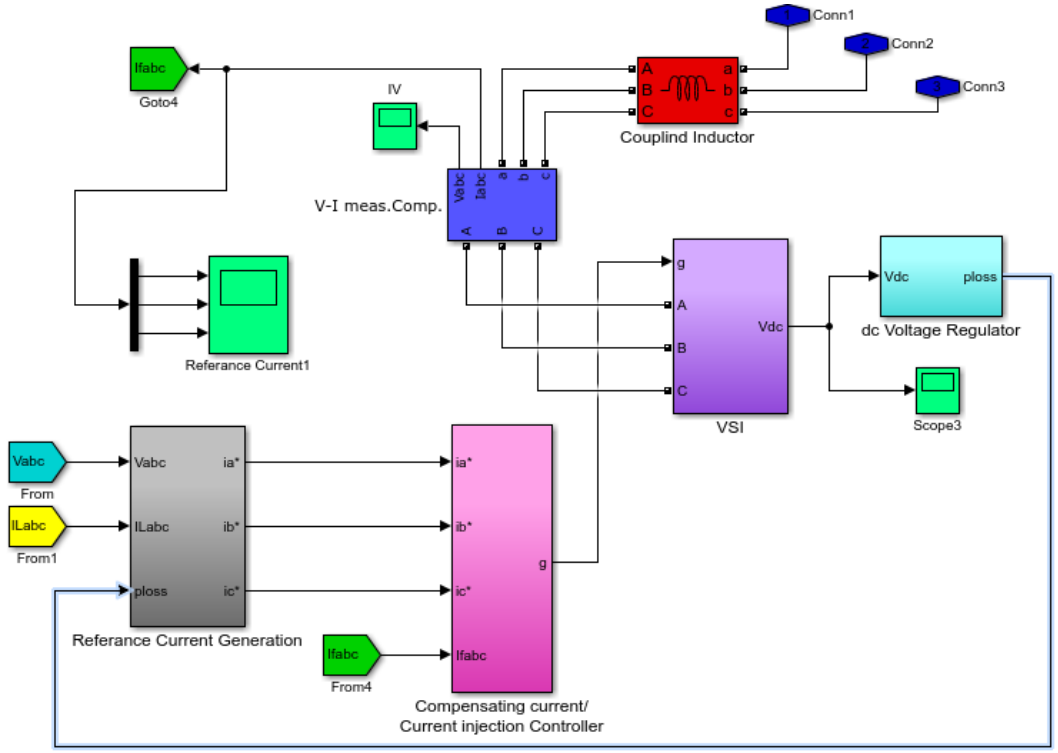

FIGURE 5.6: SAPF Simulink Model.

In the figure shown above, the reference current generation block is used to generate the reference current which is 180^o out of phase to the harmonics current.

The reference current generation is based on instantaneous reactive power theory or p-q theory.

The current injection controller block is used to inject the reference current using a hysteresis current controller to make the distorted source current sinusoidal. The operation of the injection current regulator is to generate the gate pulses of the VSI to force the actual compensation current to follow the reference current.

The DC source regulator is used as constant dc storage for an inverter.

The output of the first stage of SST, AC-DC rectifier is shown in figure 5.7.

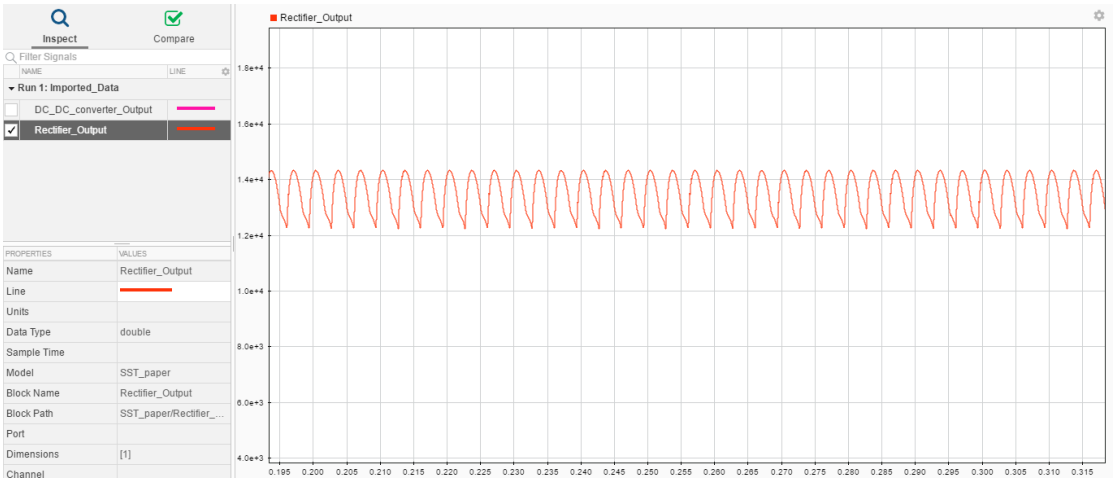

FIGURE 5.7: First Stage AC-DC Rectifier Output Voltage.

In the DAB circuit, a square wave is generated using a full-bridge inverter that is fed into medium-frequency transformer (20 kHz frequency), the transformer then steps-down the voltage level.

At the other end of the DAB, a full-bridge converter is used which rectifies the voltage at MFTs secondary side.

The combine output of the multi-stage DC-DC Converter is shown in figure 5.8. Voltages at the primary side of MFT and at the secondary side of MFT of first module of DAB are shown in figures 5.9 and 5.10 respectively.

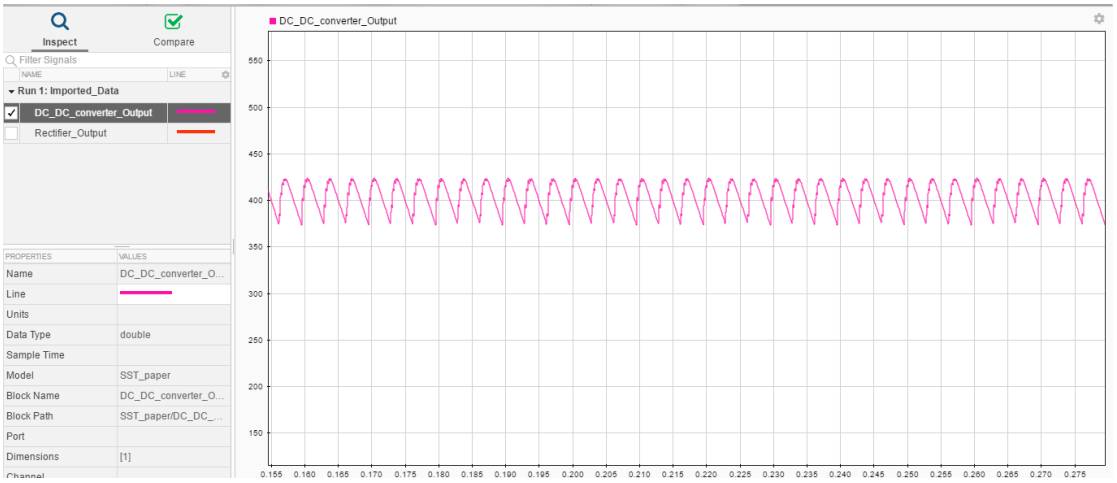

FIGURE 5.8: DAB Output.

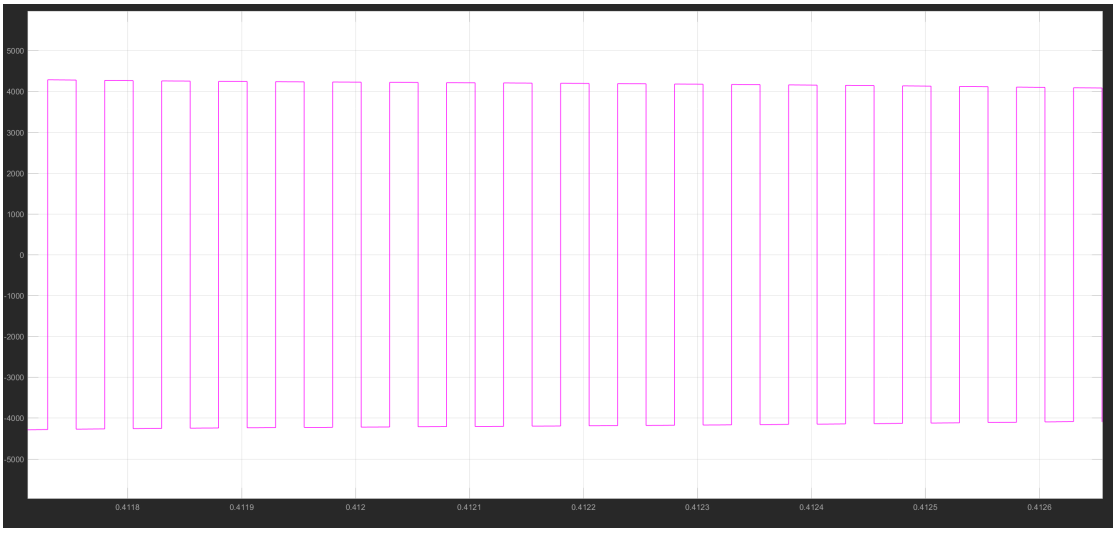

FIGURE 5.9: Transformer Input Voltage At The 1^{st} Module Of DAB.

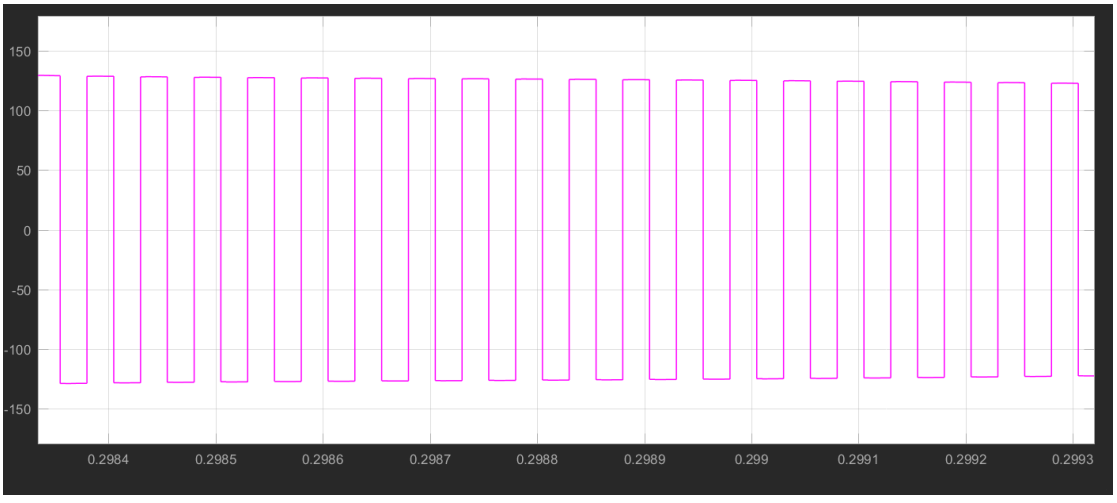

FIGURE 5.10: Transformer Output Voltage At The 1^{st} Module Of DAB.

SPWM pulses are used to generate the three-phase voltage at the consumers end with having a 50 Hz frequency. The results of the output voltage with the LC filter are shown in figure 5.11.

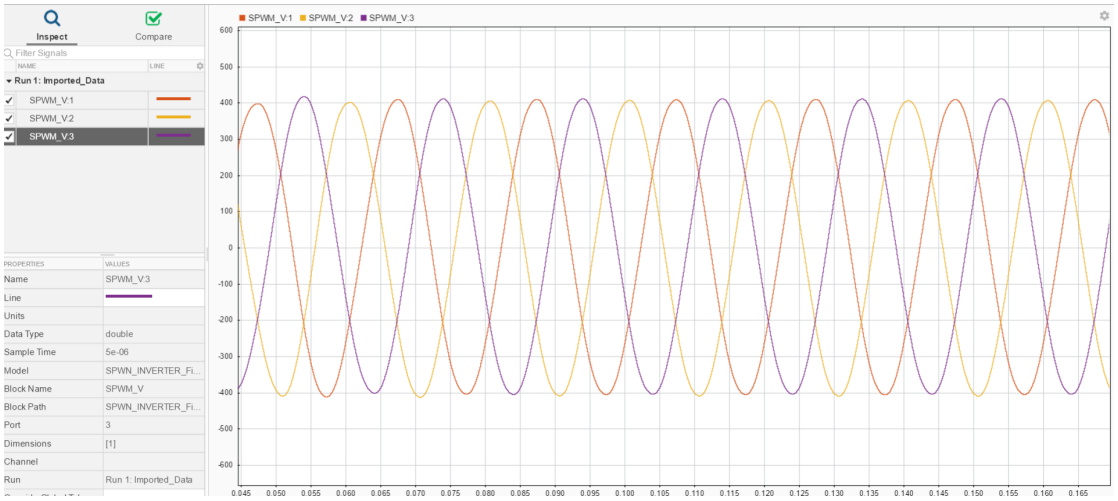

FIGURE 5.11: Load Voltage Output with the LC Filter.

5.2 Characteristics Of Performance Compression

Characteristics of performance compression between SST and CPT [138] are summarized in Table 5.1.

TABLE 5.1: Characteristics Performance Compression

	SST	**CPT**
Transformer power rating	100 kVA	100 kVA
Efficiency[%]	98	98.16
Volume[m^3]	0.0131	1.1025
THD	1.20%	11.50%
Losses	999 W	1715-2779 W

Table 5.1 depicts the comparison between our generated SST values and the conventional values with several parameters. This comparison illustrates that our

implemented mechanism shows better performance regarding all the cited parameters.

Where,

The total volume of SST is the sum of the core Volume and the Window volume which can be found out by using equations (5.1) and (5.2) respectively.

Core Volume:

$$V_c = l_m A_c \tag{5.1}$$

Window Volume :

$$V_m = MLTw_a \tag{5.2}$$

Total Volume :

$$V_T = V_c + V_m$$

Chapter 6

Conclusion and Future work

6.1 Conclusion

The alternative of bulky transformers, reduce sized, three-phase 100 kVA, 20 kHz solid-state transformer for energy distribution system has been proposed in this research, which also eliminates the harmonic content. With the help of analytical calculations, the SST model is developed and then implemented in the MATLAB simulation program.

The proposed design has three stages, the first stage is AC-DC rectifier, at the input of AC- DC rectifier, 11 kV AC voltage is applied which is then converter into approximately 15 kV DC voltage at the output of the rectifier. Nevertheless, the shape of the current at the output of AC-DC rectifier is distorted. Due to which the shape of source current does not remain sinusoidal.

The simulation results show that the total harmonic distortion value of source current is 130.9%. Shunt active power filter technique is utilized for the modification of distorted source current by injecting a compensating current in parallel with the load current. The injected current will reshape the source current into a sinusoidal waveform. The power factor has been significantly improved using SAPF technique based on instantaneous reactive power theory. Simulation results show that when SAPF technique is used, the THD value of source current reduces

from 130.9% to 1.2%, which is far better than the THD value (11.5%) of the source current of conventional power transformer.

The second stage of SST is DC-DC Converter. The input of the DC-DC converter is 15 kV DC, which is an output of the 1^{st} stage of SST. To work at high voltage, multi-level DC-DC converter topology is used, as modern power electronic converters are mostly feasible for voltages ranging from 3.3 to 6.9 kV.

The efficiency of SST is highly depended on the DC-DC converter stage. DC-DC converter has three important parts, DC-AC inverter, medium frequency transformer and AC-DC rectifier. Among them, MFT is the most vital part. One of the main advantages of SST is its reduced size, which highly depends on MFT. The DC-DC converter must be highly efficient as well as capable of providing galvanic isolation, and must have a soft- switching method. All of these can be achieved by using a dual active bridge. In the DAB, two full bridges are connected by an MFT.

The core of a transformer is made of amorphous material. As the amorphous material has a high saturation flux density (1.56 T), reasonable cost, and a much lower core loss. Amorphous material, therefore, offers a right balance between cost, efficiency, and power density. An analytical calculation shows that our new designed transformers size (core and window volume) reduced to $0.0131m^3$, while the size of the conventional transformer reported previously was $1.1025m^3$.

Hence proposed design offers 84% reduction in the size. From the calculations, the efficiency of the design turns out to be approximately 98% with much fewer losses. Our design bears losses approximately equal to 1 kW, while the conventional power transformer losses range from 1.7 to 2.8 kW approximately.

The third and final stage of SST is DC-AC inverter. The output of DC-AC inverter is low voltage AC. Ideally, the output of the inverter should be sinusoidal; however, in practice, the output of the inverter is not only non-sinusoidal but also contains harmonics. Therefore, to overcome both the upper cited problems, the sinusoidal pulse width modulation technique is used.

The overall simulation results confirm the performance reliability and correctness of the proposed design topology with effective improvements, which ensures the theoretical analysis.

6.2 Future Work

For future perspective, our designed transformer can be employed in the existing power grid network system.

The work presented in this thesis could be extended as per the following recommendations:

The development of the hardware setup for the proposed SST topology, thus to check the validity of the proposed SST model on real-time industrial applications.

Economical viability such as lifetime cost analysis of SSTs vs. conventional transformers.

Nanocrystalline and Amorphous magnetic core materials are the most suitable consideration for medium frequency transformer, however, new advanced magnetic cores materials (i.e. silicon steel with thin laminations) can be considered.

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