CAPITAL UNIVERSITY OF SCIENCE AND TECHNOLOGY, ISLAMABAD


# Implementation of SCSM in Modular Multilevel HVDC Converter with Modified Controller using New Logic Gate Converter for DC Fault Blocking Capability

by

Mirza Imran Tariq

A thesis submitted in partial fulfillment for the degree of Master of Science

in the

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*I dedicate this work to my dearest parents and my wife*


# CERTIFICATE OF APPROVAL

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1. **Mirza Imran Tariq**, Umir Amir Khan, "A New Implementation of three level cell SCSM in Modular Multilevel HVDC Converters with DC-Side Fault Blocking," *Under review in IEEE Journal, Transactions on power delivery, Jul 2020*

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# *Abstract*

Modular Multilevel Converters (MMCs) have become very attractive for medium and high power applications because of its high modularity and high power quality. The MMC is a promising converter technology for various high-voltage high-power applications such as power transmission through HVDC. Fault detection and isolation (FDI) is currently considered a crucial way to increase the reliability of MMC. DC side fault blocking capability has given a significant importance in research domain in recent years. The DC fault blocking capability enables employment of the MMC without expensive DC circuit breakers. HVDC systems has number of advantages over HVAC systems whereas protection issues remains a major challenge. This is largely due to the low inductance and absence of zero crossing in DC network compared to AC interconnection which usually results in a sudden collapse in the DC voltage and rapid rise in the fault current thus reaching damaging levels in few milliseconds. Therefore faults in HVDC system must be sensed and cleared rapidly before it reaches a damaging levels in a few milliseconds.

The basic concept of MMCs is composed of cascaded connection of cells or sub-modules (SMs) which has number of semiconductors and capacitive voltage sources. The stepped voltage waveform is synthesized by selecting different voltage levels generated by the proper connections of sub-modules. The choice of sub-modules being used in Modular Multilevel Converter generally depends on the voltage rating, number of semiconductors, voltage sensors required and DC fault blocking capability. There is a tradeoff between cost and DC fault blocking capability as this capability increases the number of semiconductors and voltage sensors which in results increases the cost.

Comprehensive study has been made for the choice of sub-module, based on the number of semiconductors, required voltage sensors and DC fault blocking capability to select the appropriate sub-module for MMC. Switched-Capacitor Sub-Module (SCSM) has been selected because of having medium number of semiconductors, less number of voltage sensors and having DC fault blocking capability

when compared with other sub-modules. However the selected sub module requires a unique and increased number of gate pulses which can make the control philosophy complex.

This work is mainly aimed to develop a logic converter which can directly interface the selected sub-module to a conventional cascaded half bridge based n-level MMC controller without changing any control and logical philosophy. Complete working principle of SCSM along with the truth tables are also included for the understanding of the sub module and its switching requirements. The design structure involves the use of 100 kV Nine-level MMC tied to a 220 kV Grid having 50 Hz frequency. The grid is having two parallel loads having 50 MW each through successive HVAC transmission lines of 10 km. The modeling and design of grid tied nine-level MMC with the proposed architecture is presented. Converter control is implemented in direct quadrature (dq0) frame using conventional vector control technique, where active and reactive powers are efficiently and independently controlled with Proportional (P) and Integral (I) compensator. Furthermore, nine-level MMC with conventional cascaded half bridge based controller is also presented to show the lacking capability of DC fault blocking. The results of final simulation of proposed architecture shows the satisfactory response of converter with the reduced number of voltage sensors and gate pulses output, which reduces the controller computational burden, and enhances the system reliability.

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# Abbreviations

| | |
|---|---|
| **MMC** | Modular Multilevel Converter |
| **HVDC** | High Voltage Direct Current |
| **FDI** | Fault Detection and Isolation |
| **HVAC** | High Voltage Alternating Current |
| **DC** | Direct Current |
| **AC** | Alternating Current |
| **EMI** | Electromagnetic Interference |
| **SM** | Sub Module |
| **SCSM** | Switched Capacitor Sub Module |
| **dq0** | Direct Quadrature |
| **PI** | Proportional Integral |
| **VSC** | Voltage Source Converter |
| **IGBT** | insulated-gate bipolar transistor |
| **PWM** | Pulse Width Modulation |
| **SPWM** | Sinusoidal Pulse Width Modulation |
| **PCC** | Point of Common Coupling |
| **HBSM** | Half-Bridge Sub Module |
| **FBSM** | Full-Bridge Sub Module |
| **ACCB** | AC Circuit Breaker |
| **DCCB** | DC Circuit Breaker |
| **PLL** | Phases Locked Loop |
| **GUI** | Graphical User Interface |
| **MW** | Mega Watt |
| **MVA** | Mega Volt Ampere |

| | |
|---|---|
| **MVAR** | Mega Volt Ampere Reactive |
| **kW** | Kilo Watt |
| **kV** | Kilo Volt |
| **kA** | Kilo Ampere |
| **km** | Kilo Meter |
| **mH** | milli Henry |
| **mF** | milli Farad |
| **ms** | milli Second |
| **rms** | Root Mean Square |

# Symbols

| | |
|---|---|
| $V_{dc}$ | Nominal DC voltage bus |
| $V_{sm}$ | Voltage across sub module |
| $R + jL$ | Phase Reactance |
| $V_{nompri}$ | Transformer nominal primary voltage |
| $V_{nomsec}$ | Transformer nominal secondary voltage |
| $P_{nom}$ | Nominal Base Power |
| $f_{SW}$ | Converter switching frequency |
| $f_c$ | Carrier Frequency |
| $\hat{m}$ | Amplitude Modulation Index |
| $m_f$ | Frequency Modulation Index |
| $\phi$ | Phase displacement per carrier |
| $N_s$ | Total switching signals per phase |
| $N_{smt}$ | Total SCSM signals in 3 phase |
| $T_{spower}$ | Sampling time for power GUI |
| $V_s$ | AC source voltage |
| $I_S$ | AC Source current |
| $N$ | Number of sub-modules or Number of carriers |
| $\pi$ | Transmission line |
| $f$ | Grid frequency |
| $L$ | AC load |
| $V_P$ | Peak Voltage |
| $T_s$ | Sampling Time for converter control |
| $E$ | Voltage across sub module capacitor |

| | |
|---|---|
| $f_{sw}$ | Converter Switching Frequency |
| $T_a$ | Average Converter Switching delay |
| $\omega$ | Angular Frequency |
| $K_p$ | Proportional Gain |
| $T_i$ | Integral Time constant |
| $K_i$ | Integral Gain |
| $K_d$ | Differential Gain |
| $f_s$ | Sampling Frequency |
| $f_0$ | Minimum Frequency |
| $C$ | capacitor |
| $V_d : V_q$ | dq frame voltage |
| $I_d : I_q$ | dq frame current |
| $P\&Q$ | Active and reactive power at PCC |
| $L_{arm}$ | Arm inductance |
| $R_{arm}$ | Arm resistance |
| $Y_g\Delta$ | wye grounded Delta |

# Chapter 1

# Introduction

## 1.1 Background

Several applications in commercial and industrial sector have begun to demand higher power devices in past few years but it's been many years that this need was fulfilled using alternating current (AC) because of its generation, transmission and distribution in the similar pattern [1]. Previously it was considered an effective way to generate, transmit and distribute AC due to the presence of transformers and induction motors to achieve desired power levels easily and economically.

However when transmission of bulk power over long distances is required, AC becomes an uneconomical and an inefficient way of transmitting power. Similarly for a intermediate voltage grid, it is hard to link directly one semiconductor power switch with DC bus. To overcome this problem, power multilevel converter structure has been introduced as an alternate solution for different voltage situations as well as for HVDC systems. This multilevel converter attains high power ratings as well as empowers the utilization of renewable energy sources. These sources such as wind, fuel cells, and photovoltaic can be easily integrated with a multilevel converter based system for application of HVDC. [2–4].

HVDC systems has number of advantages over HVAC systems however protection issues remains a big trial. This is mainly because of the fact that DC networks

have low inductance compared to AC links which usually results in an abrupt breakdown in the voltage as DC fault current rises exponentially and propagates rapidly resulting from the low inductance and absence of zero crossing in DC systems, thus attaining destructive levels in a small number of milliseconds.

This implies that fault current interruption in DC side must therefore be done very quickly than in AC side since a fault in one part of the grid (DC side) can consequently result in a total shut down of the entire network [5, 6]. This is an undesirable condition for the AC grid as well as for the converter as it may permanently damage the sub-module due to the AC grid contribution towards fault via sub-module freewheeling diodes, however this can be avoided in some other sub-modules but at the cost of additional number of semiconductors and converter losses. That is why blocking capability for DC fault with intermediate number of semiconductors is very important for a consistent working of sub-module.

## 1.2 HVDC vs. HVAC

The foreseen global energy shortage and apprehensions about greenhouse emissions have led to extensive progresses in renewable sources, and to connect different apart sources HVDC has many advantages over classical transmission. Some of its advantages are given below:

1. As there is zero frequency of HVDC, the transmission line has no inductive or capacitive losses, enabling the electrical power with unity power factor [7].

2. As frequency is zero, there is no skin affect which offers full utilization of the conductor cross sectional area.[7], also the less corona loss.

3. HVDC is highly environment friendly nullifying the requirement of large areas for installation purpose [7].

4. HVDC allows long distance bulk power transmission whereas reactive power compensation is required while transmitting HVAC over long distance [7, 8].

5. Provision of stable interconnection among asynchronous AC networks [7, 8].

6. HVDC reduces line losses thus lowers transmission price over the long distance. A general cost comparison between HVDC and HVAC cables is shown in Fig 1.1. [9].

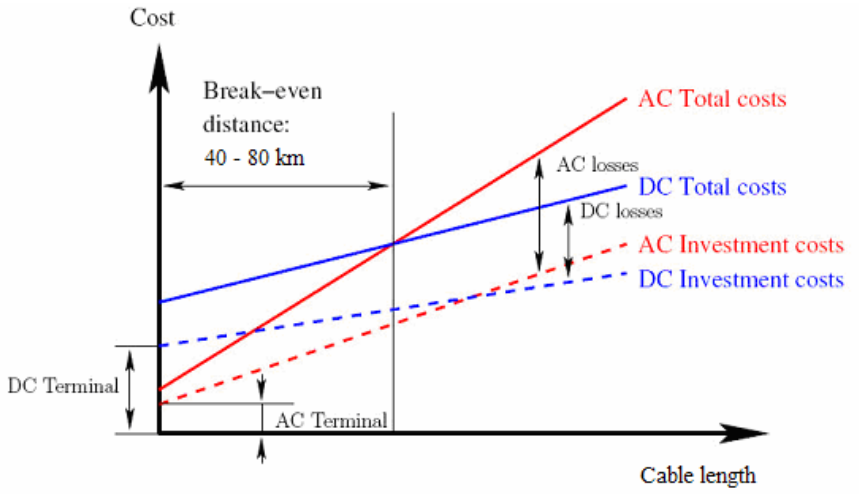



FIGURE 1.1: AC vs. DC Transmission price [9]

Above all advantages makes HVDC transmission to be considered as practical alternative for HVAC transmissions. The basic architecture of a two terminal HVDC transmission link is shown in Fig 1.2. Generally consists of two nodes i.e. a transmitting node which is known as Rectifier station which converts AC into DC and a receiving node known as inverter which again converts DC into AC. This DC - DC link is a long distance overhead or underground transmission line used for transmitting high voltage high power [7].

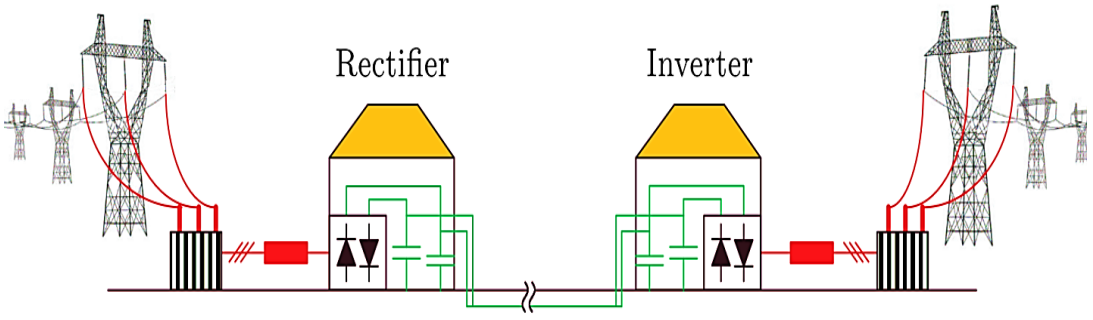



FIGURE 1.2: HVDC basic layout [10]

## 1.3 Multilevel Modular Converter

In the mid of 1970s the basic concept of multilevel converters was introduced [11]. The word multilevel starts with the converter having at least three levels. Later on, numerous multilevel converter topologies have been introduced [12–15]. Now a days modular multilevel are one of the most encouraging and challenging converters topologies for high-voltage, high-power applications such, due to their scalability, modularity and improved power quality [2–4].

### 1.3.1 Structure of Multilevel Modular Converter

Multilevel converters are systems for power conversion built by cascaded arrangement of semiconductors and voltage sources (usually capacitors) that, when properly coupled and controlled, can produce a multi-stage waveform of voltage with variable and governable frequency, phase, and amplitude. This stepped voltage waveform is produced by choosing different voltage levels generated by the appropriate linking of different voltage sources with the load. This dynamic connection is implemented by the appropriate power semiconductor switching.

The converters number of level can be described by the number of fix voltage levels or steps that a converter can generate between the output node and any arbitrary internal reference node of the converter. The internal reference is called neutral and usually a DC-link node denoted by N. At least three different steps or voltage levels are to be generated by a converter (for each phase) to be called multilevel, which differentiates it from classical two-level voltage source converter. Single-phase examples of this idea and their corresponding outputs are shown in Figure 1.3 for different number of levels. In general, different output voltage level are equidistant from each other in multiples of $V_{dc}$ [16].

By adjusting a time average of voltage level of two-level converters, variable frequency and amplitude voltage waveform can be generated. This is commonly performed with pulse-width modulation (PWM) techniques [17], but the converter

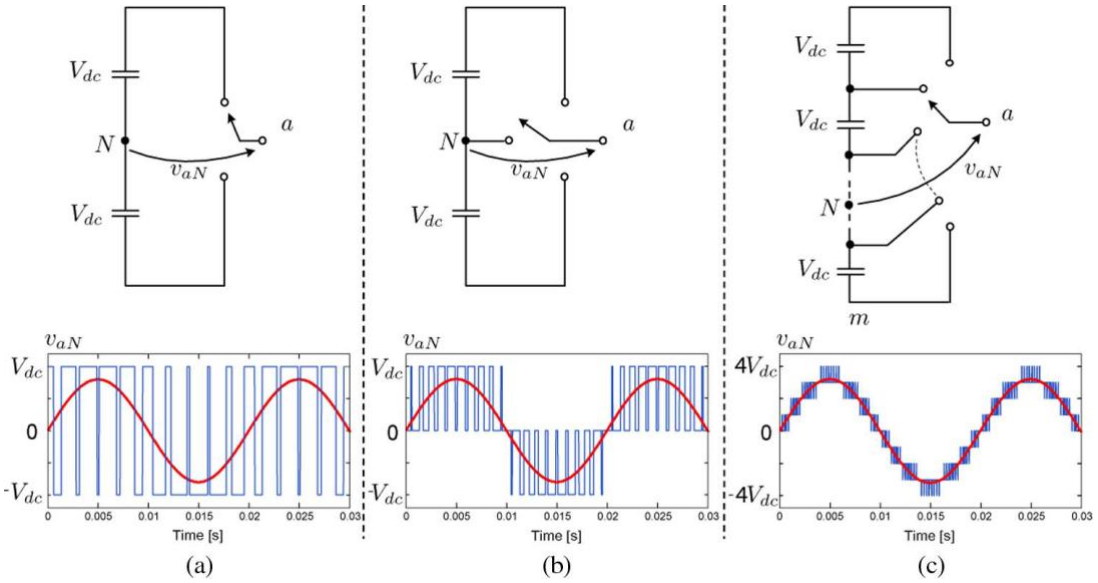



FIGURE 1.3: Converter Output Voltage: (a) two-level, (b) three-level and (c) nine-level

can give only two levels at the output and the switch has to bear the voltage rating of Vdc/2 and in order to achieve the very high operating voltages required for an HVDC scheme, several hundred IGBTs have to be connected in series and switched concurrently in each valve [18]. This scheme requires special type of IGBTs with complex gate drive circuits, and may results electromagnetic interference of very high level. On the other hand, multilevel converters allow the use of the voltage levels as an additional control element and giving more options to generate the output waveform. And the voltage rating of each switch is divided by the number of levels. For this reason, multilevel inverters have inherently improved power quality, more sinusoidal waveforms and lesser dv/dt, which decrease or even eradicate the requirement of output filters[19].

### 1.3.2 Selection of Sub-Module for MMC

Cells of several types are being used in practice such as the half-bridge [12], full bridge [13], modified full-bridge [14], cross-connected SM [14], clamp double SM [13], asymmetrical SM [15], mixed cells [20, 21], and modified mixed cells [22]. Switched- Capacitor Sub-Module has also been proposed in [23] which is used as

a most suitable sub-module for this work. The choice of sub-module is based on the number of semiconductors, voltage sensors and DC fault blocking capability.

## 1.4 Switched-Capacitor Sub-Module (SCSM)

Switched-capacitor sub-module (SCSM) is a three-level cell architecture [23]. The SCSM is able to operate with half number of voltage sensors when matched with other MMC sub-modules and it can also block DC- side faults. The SCSM comprises of two identical capacitors which can have connection in series or parallel. The sum of voltages can be attained by enabling series connection ($V_{SM} = E_1 + E_2$). While output voltage is equal to single capacitor voltage in parallel connection ($V_{SM} = E_1 = E_2$). The parallel connection forces the both capacitors voltages to be equal that is why single sensor is enough for their voltages to be measured. Bypassing the sub-module results the Zero output voltage ($V_{SM} = 0$). The architecture of SCSM is shown in Fig 1.4

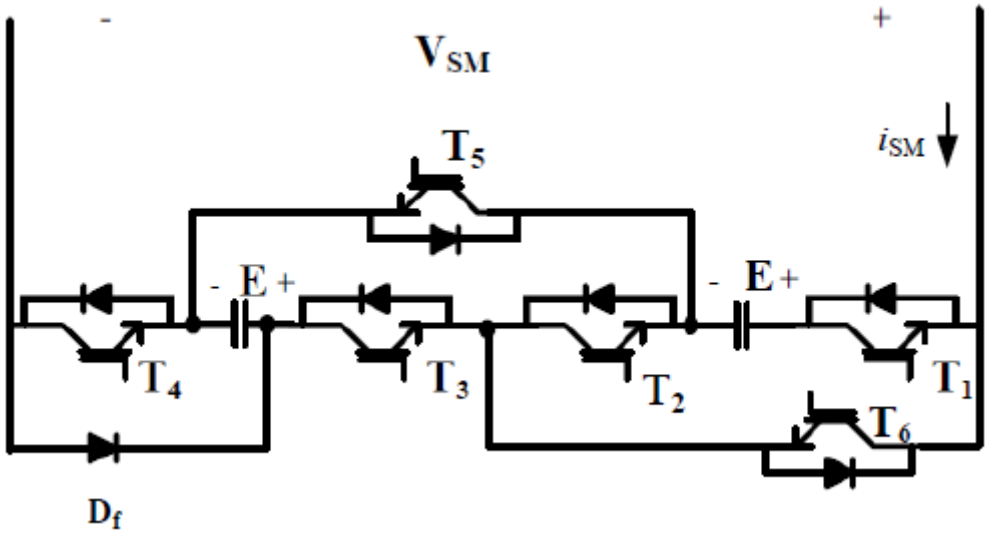



FIGURE 1.4: Architecture of Switched-Capacitor Sub-Module

## 1.5 Thesis Objectives

Following are the thesis objectives to be achieved:

1. Comparative study of sub-modules and its implementation based on the number of semiconductors, voltage sensors and ability to block DC side faults.
2. Selection of SCSM as a suitable sub-module and its implementation for 09-level modular converter is required.
3. Integration of power stage with the conventional cascaded half bridge grid tied controller without changing the control philosophy.
4. Complete operational requirements of SCSM using truth tables for the development of logic converter that can directly interface the SCSM based power stage with N-level MMC controller.
5. Development of conventional control structure for a close loop active and reactive power control at common point of coupling i.e. Grid terminal.
6. Simulation of DC side fault to illustrate the lacking capability of half- bridge sub-module to handle DC side faults.
7. Later the replacement of half bridge power stage with SCSM to interface with the conventional controller using the developed logic converter.
8. The logic convertor is aimed to provide successful operation of the MMC with one third the PWM outputs when used without the proposed converter.

## 1.6 Thesis Overview

**Chapter 1** of this thesis presents the of electrical power requirements in past and the need of transformation of HVAC to HVDC and use of multilevel modular converter.

**Chapter 2** presents the literature review. A review of DC side fault issues and their effect on converter. A comparative study of sub-modules and its implementation in multilevel modular converter. The choice of sub module based on the number of semiconductors, required voltage sensors and DC fault blocking capability. By the end of this chapter gap analysis is identified and problem statement for this thesis is defined.

**Chapter 3** of this thesis presents the implementation of SCSM for MMC. For this purpose complete working and switching requirements of SCSM is discussed. 09-level MMC is modeled and simulations presented are being carried out in Matlab/Simulink 2018a.

**Chapter 4** presents the simulation of work. Initially half bridge based MMC is simulated to show the lacking capability of blocking DC faults. After wards SCSM based power staged interfaced with 9-level MMC conventional controller using the designed logic converter is simulated and results from normal mode of operation and DC side fault conditions are presented.

**Chapter 5** concludes the whole discussion and work made throughout this thesis and expounds the possible future work.

## 1.7 Thesis Outcomes

Thesis major outcomes are described below:

1. Selection of appropriate sub-module based on the comparison among different sub-modules.
2. Development of 09-level MMC model in Matlab/Simulink environment.
3. Development of 220 kV, 50 Hz Grid model along with transmission and load network.
4. Successful coupling of converter model with grid model.
5. Development of logic converter for the integration of SCSM with 09-level MMC controller model.

6. Converter power sharing control on various power references.

7. Verification of the DC side fault blocking capability of SCSM.

8. Illustration of lacking capability of half- bridge sub-module to handle DC side faults.

## 1.8 Chapter Summary

This chapter provides a quick introduction of the trend changing of power requirements from HVAC to HVDC. Advantages of HVDC, emergence of multilevel modular converter and its structure is presented along with the selection of sub-module At the end of the chapter, thesis objectives, overview and its outcomes are listed to give an idea of the whole thesis.

# Chapter 2

# Literature Review

## 2.1 Introduction

The first two level voltage source converter was commercially used by ABB in 1997 [24, 25]. The increased demand of high quality and reliable converters for applications having high voltage and high power led the emergence of multilevel modular converters, which not only addressed the quality issues but also provided efficient power delivery to the electrical grid. The changing trend of power delivery from HVAC towards HVDC also forced the need of efficient and reliable converters for HVDC applications. So in 2003 the first concept of modular multilevel converters for HVDC applications was proposed by Marquardt [26] and in 2010, for the first time it was commercially used in the Trans Bay Cable project in San Francisco. [27]. Among the types of voltage source converter, Modular Multi-level Converter (MMC) is now very popular type for HVDC applications [28]. Many new topologies are developed for MMCs which are discussed briefly. Selection of suitable topology for testing and verification of DC side fault handling, using the minimum possible number of components is also the part. Afterwards the gap analysis is given for this thesis while the problem statement is established at the end of this chapter.

## 2.2 High Voltage Direct Current (HVDC)

For electrical power transmission system high voltage direct current (HVDC) is the power superhighway [29], where direct current is used for massive transmission of electrical power compared with the more common alternating current (AC) systems [30]. Some of its advantages are also mentioned in the previous chapter. HVDC systems have lower losses and are less expensive when used for long-distance power transmission. HVDC nullifies the requirement of large currents need to charge and discharge the cable capacitance each cycle when used in underwater power cables. The greater cost of HVDC transformation architecture compared to an HVAC system may still be justified for shorter distances because of some further advantages of DC of links.

The improvement of renewable energy sources and its integration have become in increasingly vital in past few years due to the development of energy requirement and the continuing enervation of fossil fuels. For renewable energy integration, high-voltage direct current systems based on voltage source converters (VSC-HVDC) are considered to be one of the best practical solutions [25, 31].

### 2.2.1 Voltage Source Converters (VSC)

Voltage source converter (VSC) systems are built with self-commutating switches, usually insulated-gate bipolar transistor (IGBT) technology, which have many benefits as compared to thyristors. The application of pulse-width modulation (PWM) techniques for high-frequency (over 1 kHz) is being offered by self-commutating devices which have been in used in the industrial sector for drives and other needs since the early 1990s. Fully controlled AC voltage may be synthesized by VSC, where active and reactive powers can be controlled precisely by the use of PWM. Fundamental frequency sine-wave is appeared as a voltage output along with harmonics at the switching frequency and its multiples. Fast control allows the voltage source converter to behave as a current source with proper feedback [32]. Harmonics are lower due to higher switching frequencies, therefore requirements for

filtering are reduced. Figure 2.1 shows the basic schematic of a two level VSC HVDC transmission system [33].

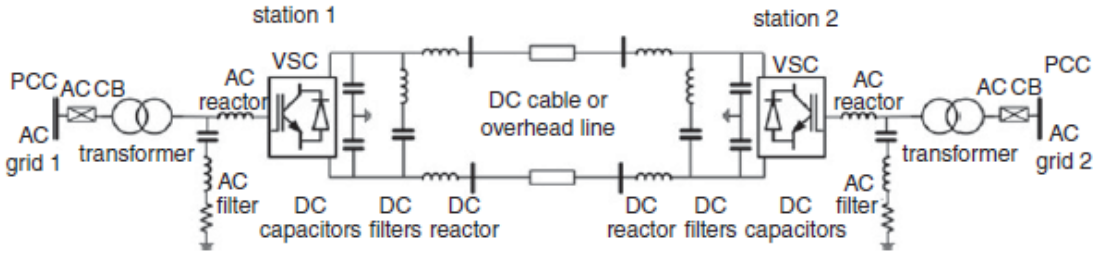



FIGURE 2.1: VSC-HVDC transmission system based on a two-level converter [33]

As given in Figure 2.1 AC power is first transformed to appropriate value and then rectified to DC level. Power is transmitted after filtration through a DC cable or overhead line. At receiving side DC power is inverted to AC using a VSC converter and transformed to AC level to be connected with grid. Before the emergence of multilevel modular converters, two-level converter is being used for a long time with high frequency carrier modulation for the switching of IGBTs to produce the required output.

### 2.2.2 Two level VSC in HVDC

Two level voltage source converter is being used commercially supported by international vendors such as ABB, Alstom and Siemens because of its lower control complexity and simplicity. A list of few commercial projects of two level voltage source converters are given in Table 2.1.

TABLE 2.1: Two level VSC HVDC Commercial Projects [25]

| **Project Name** | **Year** | **Power** |
|---|---|---|
| Hellsjon | 1997 | 3 MW |
| Gotland HVDC Light | 1999 | 50 MW |
| Tajaereborg | 2000 | 8 MW |
| Terrenora Directlink | 2000 | 180 MW |
| TrolA offshore | 2005 | 84 MW |
| Estlink | 2006 | 350 MW |
| Vallhalloffshore | 2009 | 78 MW |
| Caprivilink | 2010 | 300 MW |
| Vastlanken | ongoing | 1200 MW |

The commercial overview of two level voltage source converter shows the capability to handle high voltage high power applications practically for more than twenty years and still in ongoing projects. Despite the fact that two level VSC has proved its capability in commercial sector due its many advantages yet there are still some certain limitations when used in HVDC applications some of them are listed below:

1. Problematic series connection of IGBTs. [30, 34].
2. Static Balancing [30].
3. Dynamic Balancing [30].
4. Requirement of Passive Filters [34].
5. Higher Switching losses [34].
6. High Current Ripple and dv/dt [35].

Based on the above discussion, improvement in converter topologies is still required which can address the limitations of two level voltage source converters.

## 2.3 Multilevel Modular Converter Concept

The basic concept of a multilevel converter for achieving higher power is cascaded semiconductor power switches having many lower voltage dc sources (mostly capacitors) in series connection to implement the power conversion by creating a staircase voltage waveform. Batteries and renewable energy voltage sources can also be used as the multiple dc voltage sources. The commutation of the power switches combine these multiple dc sources to get high voltage at the output whereas, the power semiconductor switch voltage rating depends only upon the dc voltage sources rating to which they are connected and which is the small part of output voltage [36]. The basic working of MMC is givenin Figure 2.2.

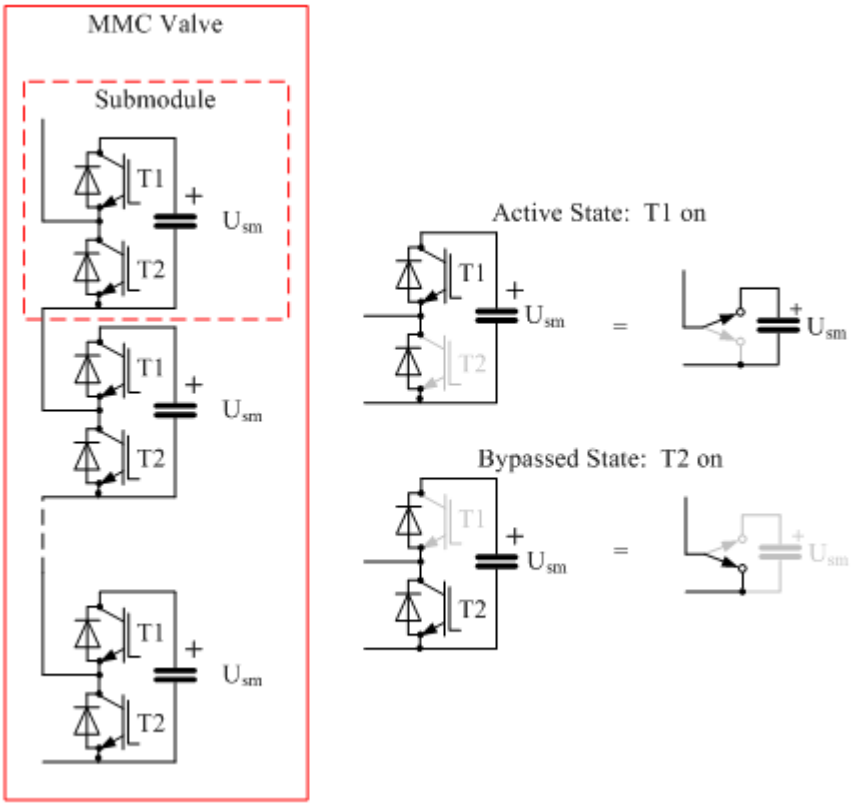



FIGURE 2.2: Basic operation of MMC

As presented in Figure 2.2 each sub-module is compromised of power electronic semiconductor switches and a DC source. Any DC source can be connected (incorporated in current path of any arm) or can be bypassed depending on the direction of arm current. Staircase wave form can be obtained by appropriate switching of power switches. The number of voltage levels or steps that can be produced by the converter between the output node and any arbitrary internal reference node (neutral) holds by the converter are defined as the number of levels of a converter. The MMC has two arms per phase, each consists of n series-connected MMC cells. Overall six arms are required to make a three phase MMC. Figure 2.3 shows the basic three phase MMC connected with AC source along with the voltage waveform of phase arm.

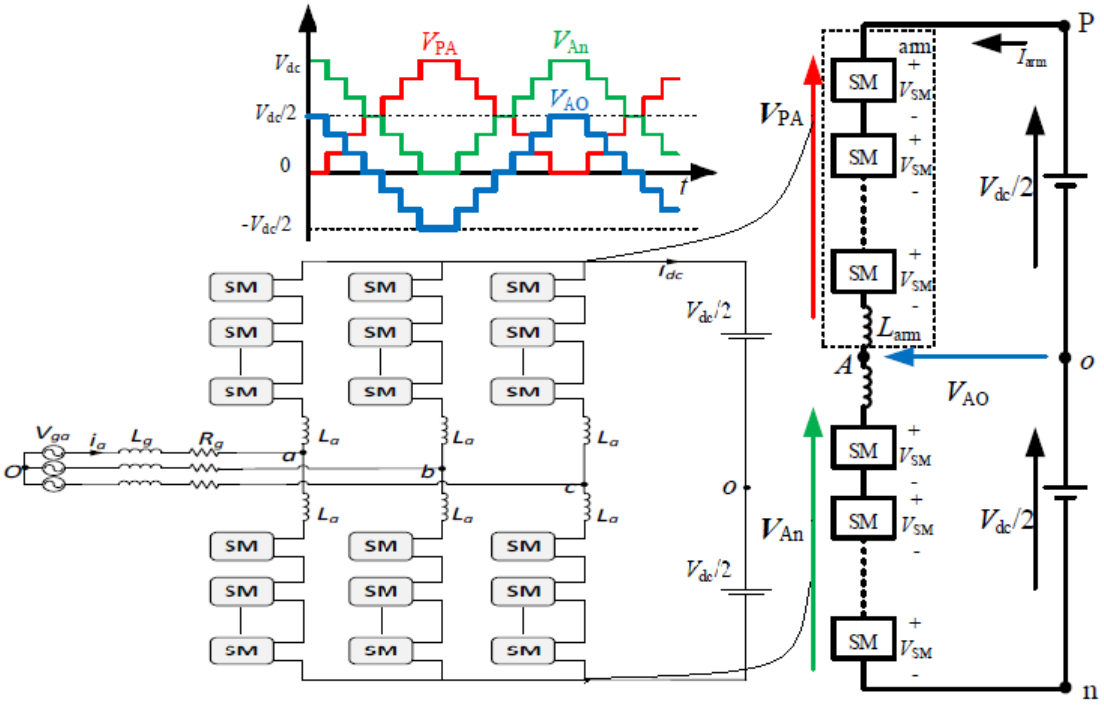



FIGURE 2.3: Three phase MMC with per arm voltage waveform

### 2.3.1 Advantages of Multilevel Modular Converter

There are several advantages of modular multilevel converter as compared to a conventional two-level converter. The attractive features of a multilevel converter are briefly summarized below:

1. Modularity and scalability [2, 4].
2. Low distortion in output voltage [36].
3. Less dv/dt stresses [36].
4. Low switching losses (MMC can be operated at fundamental frequency).
5. Higher efficiency [36].
6. Eliminates the need of output filters [19].
7. Reduced Total Harmonic Distortion (THD) [37].
8. No critical capacitor voltage balancing [37].

### 2.3.2 MMC-VSC in HVDC

High efficiency has made the Modular Multilevel Converters (MMC) the best topology for Voltage Source Converter High Voltage DC (VSC-HVDC) systems because of its attractive and suitable features. The demand for MMC-VSC based HVDC transmission structures has developed considerably in past few years. This development is mainly because of the enhancements in the power and voltage ratings of insulated gate bipolar transistors packages and several new MMC-VSC based HVDC applications. Since the first commercialization, MMC got large interest for HVDC applications. Some of completed and ongoing commercial MMC-HVDC projects are given in Table 2.2.

TABLE 2.2: MMC-VSC HVDC Commercial Projects [19, 38]

| **Project Name** | **Year** | **Power** |
|---|---|---|
| Trans Bay Cable | 2010 | 400 MW |
| Borwin2 | 2011 | 400 MW |
| Skagerrak Pole4 | 2014 | 700 MW |
| INELFE | 2015 | 690 MW |
| SylWin1 | 2015 | 864 MW |
| HelWin1 | 2015 | 576 MW |
| HelWin2 | 2015 | 690 MW |
| BorWin2 | 2015 | 800 MW |
| DolWin1 | 2015 | 800 MW |
| DolWin2 | 2016 | 916 MW |
| DolWin3 | 2018 | 900 MW |
| Caithness Moray | 2019 | 1200 MW |
| BorWin3 | 2019 | 900 MW |
| ULTRANET | 2019 | 2000 MW |
| COBRAcable | 2019 | 700 MW |
| North Sea Link | ongoing | 1400 MW |

## 2.4 Multilevel Modular Converter Cells (Sub-Modules)

The building-block of multilevel modular converter architecture is the basic unit (sub-module) which is used to implement any dc-ac or dc-dc power electronic

converter. In order to fulfil the requirements for any specific application, series or parallel connection of sub-modules can be made in various topologies. The choice of these building block cells is usually based on the number of semiconductors, voltage sensors and DC fault blocking capabilities. The basic function of these sub-modules are discussed below:

### 2.4.1 (a) Half Bridge Sub-Modules [12, 15]

The Half Bridge Sub-Module (HB-SM) offers the lowest expense and lowest power loss module. HB-SM is considered the simplest cell structure to generate a unipolar voltage output. Sub-module switch is required to allow bidirectional current flow with unidirectional blocking of voltage. Operation of cell is offered for two quadrants only and can give output of two voltage levels. Figure 2.4 shows the configuration of half bridge sub module along with output levels.

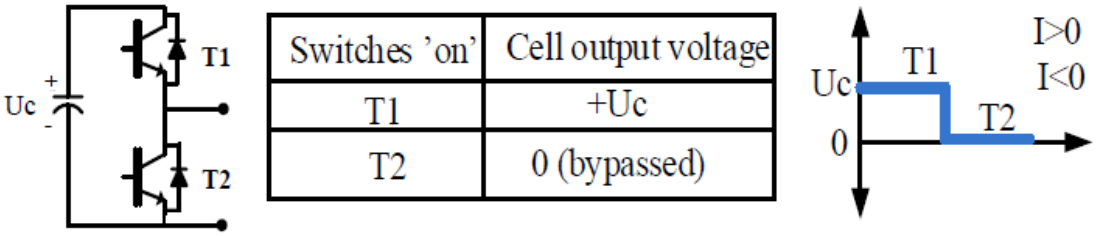
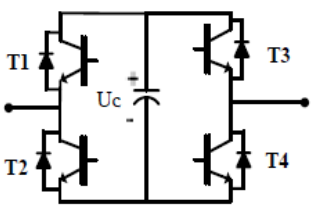



FIGURE 2.4: Half bridge Sub-module operational modes

### 2.4.2 (b) Full Bridge Sub-Module [13, 15]

The Full-Bridge-Sub module (FB-SM) is well recognized and allows the desired function. It can cut off the arms currents of any direction by impressing the appropriate polarity of terminal voltages in the arm. This can be done simply by turning off all the IGBTs. However in normal operation, additional switching states are not very useful when compared with HB-SM, because of the fact that DC-Bus in HVDC applications normally does not requires reverse voltage polarity [13]. Therefore double number of semiconductors will double the losses which

signifies a severe drawback in normal operation. Figure 2.5 presents the structure of full bridge sub module along with output levels.




| Switches 'on' | Cell output voltage |
|---|---|
| T2, T3 | +Uc |
| T1, T4 | -Uc |
| T1, T3 | 0 (bypassed) |
| T2, T4 | 0 (bypassed) |

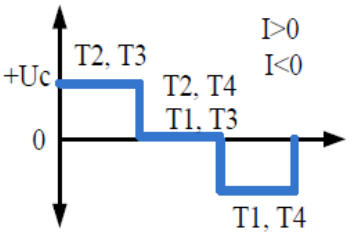


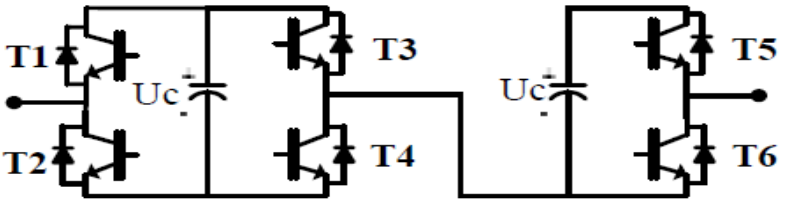

FIGURE 2.5: Full bridge Sub-module operational modes

### 2.4.3 (c) Mixed Cell [15, 20, 21]

Mixed cell can be attained by combining the basic half bridge structure with full bridge cell. Benefits of both unipolar and bipolar cells can be achieved through this combination. Their series connection can generate asymmetrical four voltage levels. In [21] it has become apparent that both network faults either AC or DC can be resisted by mixed cell based MMC, which is core requirement of massive interconnected multi-terminal HVDC grids for next generations. DC fault reverse blocking capability can be attained by mixed cells MMC and three-level cells MMC at lesser losses (on-state) when compared with alternative arm and full-bridge based MMC in the power losses evaluation in [21]. Figure 2.6 shows the structure of mixed cell with four-level voltage output.

### 2.4.4 (d) Asymmetrical Sub-Module [15]

Asymmetrical cell can be created by doubling the basic cell in a different manner. To create an alternative four-level cell configuration two unique voltage levels of basic cells are coupled at the dc side. The overall size of the converter system is reduced by using the asymmetrical sub-modules with different capacitor voltages due to the fact of having less number of semiconductor switches which also lowers the semiconductor losses and the requirement of gate drivers is also reduced. [39]. Furthermore, under conditions of DC line fault, asymmetric mixed MMC based




| Switches 'on' | Cell output voltage |
|---|---|
| T1, T3,T5 | +Uc |
| T2, T4,T5 | +Uc |
| T2, T3,T6 | +Uc |
| T2, T3,T5 | +2Uc |
| T1, T4,T6 | -Uc |
| T1, T4,T5 | 0 (+Uc-Uc) |
| T1, T3,T6 | 0 (bypassed) |
| T2, T4,T6 | 0 (bypassed) |

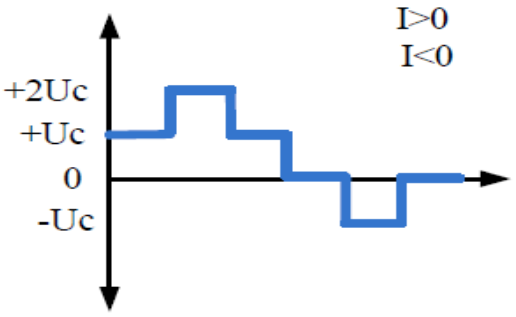
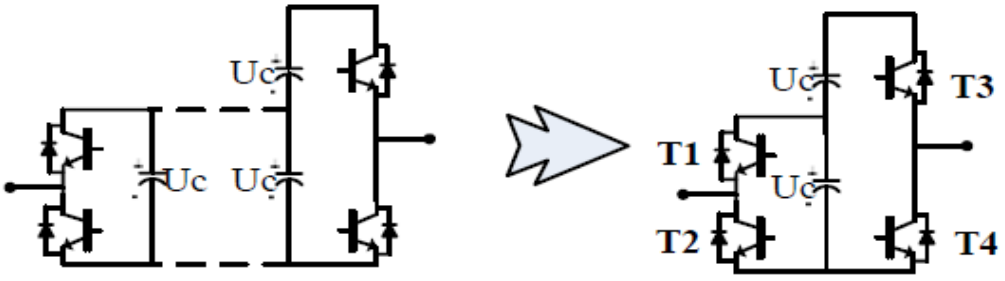



FIGURE 2.6: Mixed cell Sub-module operational modes

HVDC can be operated flexibly at reduced DC voltage even zero level [40]. Figure 2.7 shows the asymmetrical cell along with output levels.




| Switches 'on' | Cell output voltage |
|---|---|
| T1,T3 | +Uc |
| T2, T3 | +2Uc |
| T1,T4 | -Uc |
| T2, T4 | 0 (bypassed) |

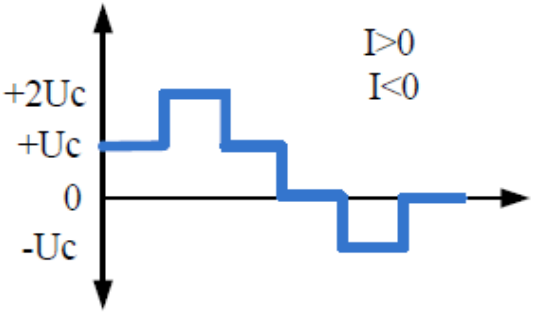
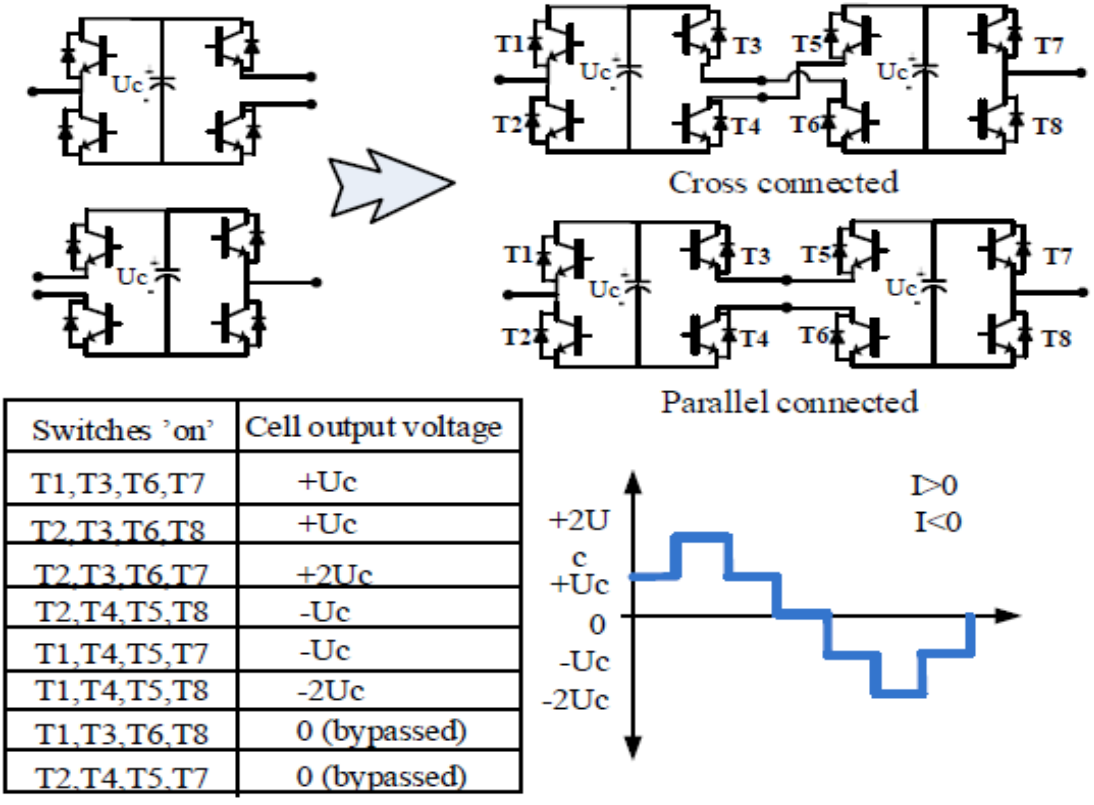



FIGURE 2.7: Asymmetrical cell operational modes

### 2.4.5 (e) Cross-connected Sub-module [14, 15]

As reported in [41], full bridge cell can be connected in cross fashion to get alternative symmetrical bipolar cell configuration as given in Figure 2.8. More importantly, greater voltage levels are acquired by the cross connection of more in-between capacitors in the configuration. Number of switches are considerably reduced by exploiting this topology for multilevel inverter without using high voltage switches [42]. As shown in Figure 2.8, parallel connection can be established by swapping the connection of switch with the in-between capacitors of the cell. This aids in reducing the voltage ripple of capacitor. This alternative scheme at reduced device current rating is proposed in [43].

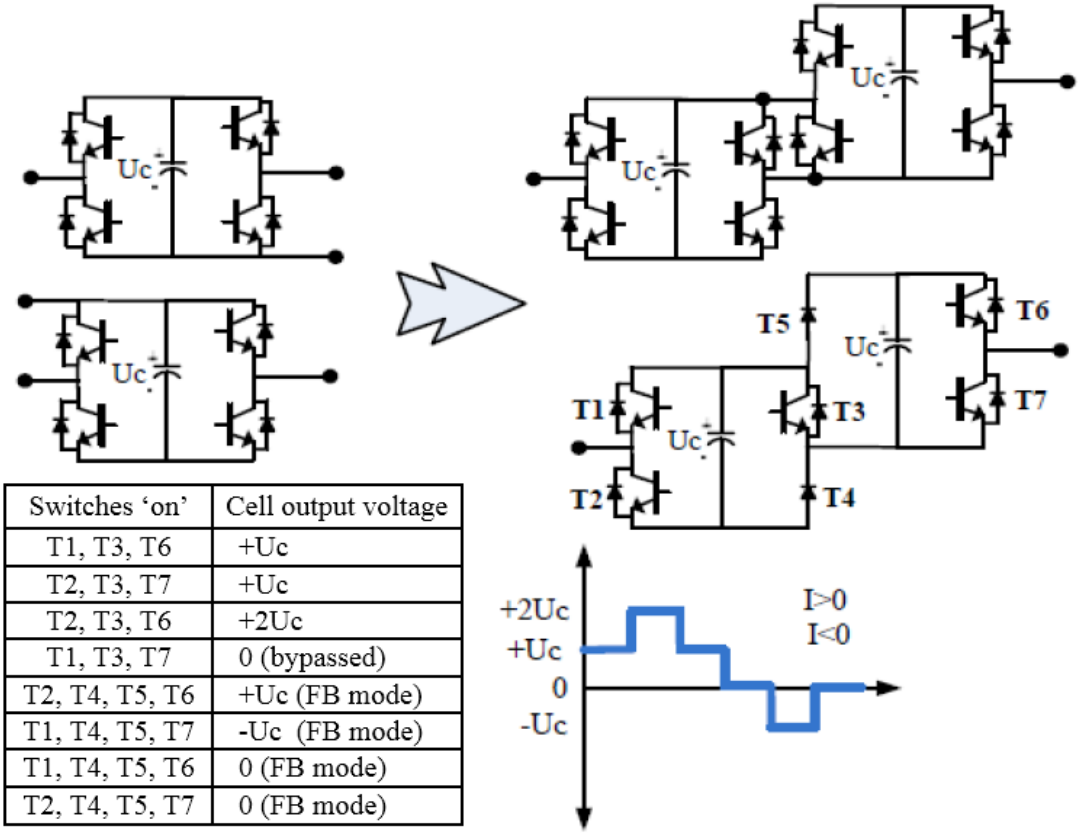



| Switches 'on' | Cell output voltage |
|---|---|
| T1,T3,T6,T7 | +Uc |
| T2,T3,T6,T8 | +Uc |
| T2,T3,T6,T7 | +2Uc |
| T2,T4,T5,T8 | -Uc |
| T1,T4,T5,T7 | -Uc |
| T1,T4,T5,T8 | -2Uc |
| T1,T3,T6,T8 | 0 (bypassed) |
| T2,T4,T5,T7 | 0 (bypassed) |

FIGURE 2.8: Cross-connected Sub-module operational modes

### 2.4.6 (f) Clamp double Sub-module [13, 15]

An alternative connection of the full bridge sub module has been proposed in [43]. Cell capacitors can be reconfigured in series or a parallel by proper switching. Though, additional design attentions should be taken into account for the changeover to the full-bridge mode which two capacitors that may have different voltages will be connected in parallel. As shown in Figure 2.9 one way of avoiding the paralleling issue is to replace active switches by diodes in the parallel path. However, this will limit the full-bridge operation to a three-quadrant sub-module operation. The voltage levels related to the different states of switching and cell structure is presented in Figure 2.9.

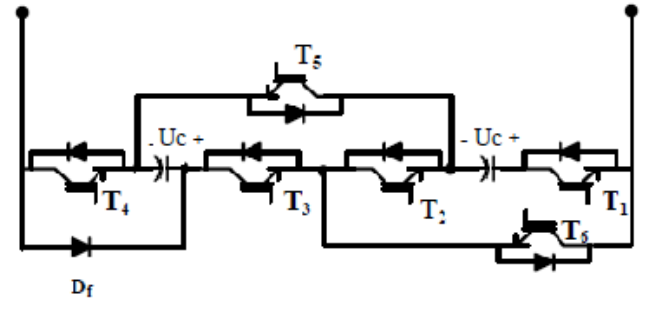



| Switches 'on' | Cell output voltage |
|---|---|
| T1, T3, T6 | +Uc |
| T2, T3, T7 | +Uc |
| T2, T3, T6 | +2Uc |
| T1, T3, T7 | 0 (bypassed) |
| T2, T4, T5, T6 | +Uc (FB mode) |
| T1, T4, T5, T7 | -Uc (FB mode) |
| T1, T4, T5, T6 | 0 (FB mode) |
| T2, T4, T5, T7 | 0 (FB mode) |

FIGURE 2.9: Clamp double Sub-module operational modes

### 2.4.7 (g) Switched-Capacitor Sub-Module [23]

A three-level switched-capacitor sub-module (SCSM) is presented in [23] which allows capacitor to be connected in series or parallel. This SCSM has similar behavior as of the cell given in [43], but with a less number of semiconductor switches with the same voltage rating. With respect to the current of switches in the proposed SM in [44], the engaged semiconductor switches transport the full SM current during bypass and series-connection states, while carrying half of SM current during parallel connection mode. Bypassing the cell gives the zero output voltage, while sum of capacitor voltages can be attained by connecting the capacitors in series. Connection of two capacitors in parallel gives the first voltage level. Voltages are forced to be equal when capacitors are connected in parallel therefore a single sensor is enough to monitor their voltages, i.e. the SCSM is also capable of operation with a reduced number of sensors when compared with other MMC cell architectures [23]. Moreover, the on-state voltage drop, correspondingly conduction losses, of the SCSM is between that of half-bridge based MMC and clamp double SMs based MMC systems [44]. Figure 2.10 presents the configuration of SCSM along with output levels.




| Switches 'on' | Cell output voltage |
|---|---|
| T1,T3,T4,T5,T6 | +Uc |
| T1,T2,T3,T4 | +2Uc |
| T2,T4,T5,T6 | 0 (bypassed) |

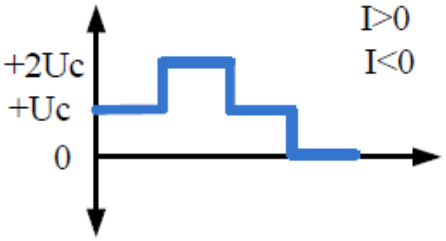



FIGURE 2.10: Switched-Capacitor Sub-Module operational modes

### 2.4.8 Evaluation of Sub-Modules

Based on the above the above discussion, Table 2.3 presents the final evaluation and comparison among different discussed three level sub-modules.

TABLE 2.3: Different type of MMCs Three-level Cells [15, 23]

| **Sub-module type** | **(a)** | **(b)** | **(c)** | **(d)** | **(e)** | **(f)** | **(g)** |
|---|---|---|---|---|---|---|---|
| **No. of IGBTs** | 4 | 8 | 6 | 6 | 6 | 5 | 6 |
| **No. of extra diodes** | 0 | 0 | 0 | 0 | 2 | 2 | 1 |
| **No. of voltage sensors** | 2 | 2 | 2 | 2 | 2 | 2 | 1 |
| **Switches in conduction** | 2 | 4 | 3 | 3 | 4 | 3 | 5 |
| **Bipolar operation** | No | Yes | Yes | Yes | Yes | Yes | No |
| **DC Fault blocking ability** | Unable | Able | Able | Able | Able | Able | Able |
| **Design complexity** | Low | Low | Low | High | High | High | Low |
| **Control complexity** | Low | Low | Low | High | Low | Low | High |

## 2.5 DC Side Faults

HVDC systems has number of advantages over HVAC systems whereas protection issues remains a big challenge, in which DC side fault, protection of converter and contribution of AC grid towards fault via converter freewheeling diodes is the main concern. So far, plenty of work have been concentrated on the modeling [45–47] , control [48–50] and steady-state analysis [51, 52] of the MMC-HVDC. Characteristics of DC faults and corresponding solutions for fault clearance should be investigated in detail especially when the MMC is used in super DC grids and transmission lines having long distance. Mathematical modelling for several DC fault conditions is done in [53] where HVDC system is based on two-terminal VSC. Theoretical analysis is proposed in [54] for VSC cable fault with three stages. But, [53, 54] both are two-level converter based. The operation of MMC under pole-to-ground fault is worked out and expression is derived for DC current in [55].

Whereas, conventional half-wave rectifier bridge is used to achieve the corresponding DC voltage. It must be noted that the equivalent circuit after blocking the MMC is different from the conventional half-wave rectifier bridge, as the former one has an inductor in each arm. A pole-to-pole fault analysis of multi-terminal MMC systems is proposed in [56]. However, the fault current is obtained by electromagnetic transient simulations. Analytical fault current calculation method of pole-to-pole fault for one terminal MMC and MMC-based DC grids are introduced in [14, 57]. Though, the fault current expressions are valid only before blocking the MMC. Reference [58] derives the detailed differential equations of MMC in both pre-blocking and post-blocking conditions, and also proposes the corresponding solving method. However, this method belongs to numerical analysis and the analytical solution cannot be given. Figure 2.11 illustrates the DC short-circuit fault of MMC.

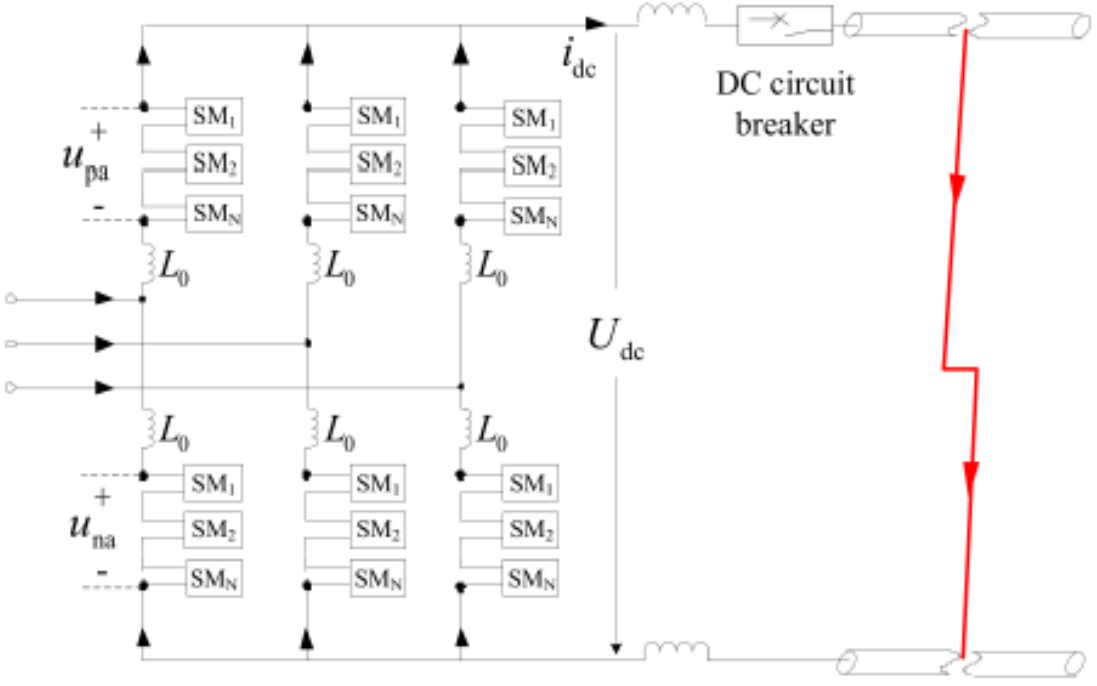



FIGURE 2.11: MMC arrangement under DC short-circuit fault [59]

DC voltage is represented by $U_{dc}$ while DC line current is given by $I_{dc}$. The fault current largely compromises of current discharged by sub-module capacitor and short-circuit current of the three-phase AC system. Current discharged by sub-module capacitor is the leading factor before the MMC is blocked. The fault

current can reach several tens of kA in a few milliseconds as it rises too fast [59]. The main technical barrier that confines the application of MMC in DC grids or long-distance overhead transmission lines is DC fault isolation. Generally, there have been three solutions for solving this problem [60, 61]:

1. The first solution is to trip the AC circuit breaker (ACCB). The benefits of tripping AC circuit breaker includes economic efficiency and highly maturity in the technology. That is why most practical commercial VSC-HVDC projects use this method to clear DC line faults. However, it will take a long time for the system to recover from the DC line faults due to the slow response of the ACCB, [60]. Figure 2.12 shows the DC current of MMC with this solution. Simulation results in [59] shows a DC fault occurs at t = 2 s, and the MMC is blocked at t = 2.00356 s. whereas, it is tripped at t = 2.06 s considering the slow response of the AC circuit breaker. The fault current goes down very slowly.

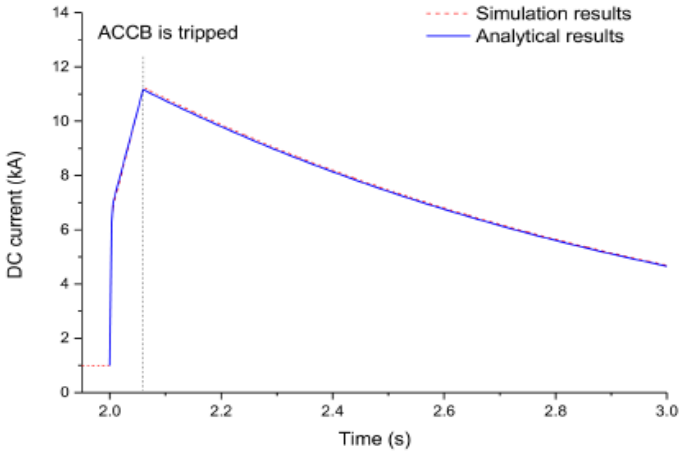



FIGURE 2.12: DC current of MMC with 1st Solution [59]

2. Adopting fault blocking converters is another option [62]. To prevent IGBT damage due to overheating, converters will be blocked when the current flowing through the IGBT reaches double of its rated value. Some converters may produce reversed electromotive force to obstruct the fault current, such as full-bridge MMC. For this solution, power transmission restoration from temporary DC faults is fast. However, the device cost and power losses

increase significantly due to more requirement of semiconductors. Converter based on full-bridge sub-modules needs twice semiconductor switches and therefore power losses increase by double when compared with the half-bridge sub-modules based MMC. Converter based on clamp-double sub-modules requires 1.25 times semiconductor switches and the power losses increase by about 35 percent [63]. Figure 2.13 shows the DC current of MMC with second solution. Simulation results in [59] shows a DC fault occurs in the system at t = 2 s, and the MMC is blocked at t = 2.0035 s. whereas, almost 2.16 ms is taken by the fault current to become zero.

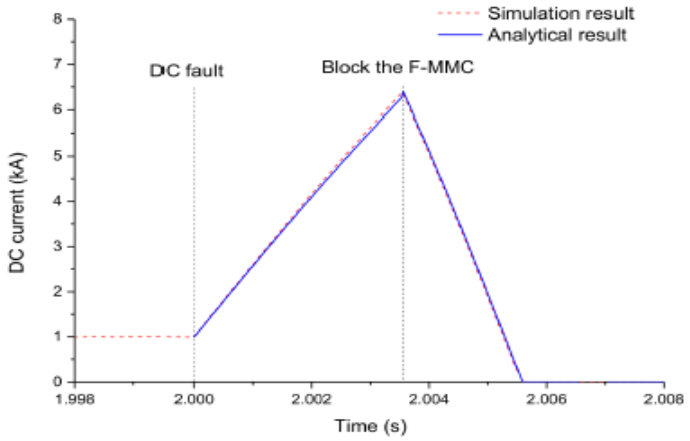



FIGURE 2.13: DC current of MMC with 2nd Solution [59]

3. The engaging of DC circuit breakers (DCCBs) is the third method for DC fault handling. In late 2012, ABB released a hybrid DCCB that can break a maximum DC fault current of 9 kA within 5 ms [64]. There have been some shortcomings for the present DCCBs, such as high cost of manufacturing and that the technology is not so matured. Figure 2.14 shows the DC current of MMC with third solution. Simulation results in [59] shows at t = 2 s, a DC fault occurs at the DC side of the converter. The access of the arrester at t = 2.00806 s will rapidly reduce the fault current. Table 2.4 shows the important factors of the systems having different clearing solutions for DC faults, where the fault clearing time and the maximum fault current are included. It can be realized that solution 1 has largest maximum fault current with slowest fault clearing time. Fault clearing time of Solution 3 is slightly larger than

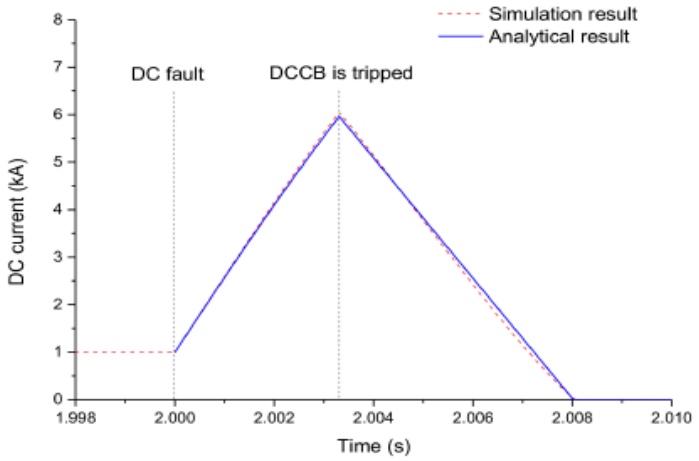



FIGURE 2.14: DC current of MMC with 3rd Solution [59]

TABLE 2.4: Important factors of the systems with three solutions

| | **Fault Clearance Time** | **Maximum Fault Current** | **Converter Blocking** |
|---|---|---|---|
| **Tripping of ACCBs** | 9318 ms | 10.8 kA | Yes |
| **Fault blocking MMCs** | 6.26 ms | 6.4 kA | Yes |
| **Engaging DCCBs** | 8.06 ms | 6.0 kA | No |

solution 2 but the maximum fault current is smaller. Among all solutions, the converter will not be blocked using Solution 3, which means the power can be continuously transmitted when a DC fault occurs in MMC-based DC grids but the high manufacturing cost and low maturity limits the solution.

## 2.6 Control of Grid Tied VSCs

Different types of current control strategies i.e. linear and non-linear current control of VSCs are discussed in [65]. The author classifies linear control into different types i.e. stationary frame PI control, rotating frame PI control, state feedback control, model predictive control and deadbeat control. The main disadvantage of the stationary frame PI control is that it has inherent tracking error i.e. this technique cannot provide zero steady state error. Whereas the model predictive

control and dead beat control cannot afford to provide over current limit. The rotating frame PI control provides zero steady state error but at the expense of dq0 transformations and an extra phase locked loop. The dynamics of current control loop in dq reference frame are fast and well damped. In [66], the author presents two control techniques for the active and reactive power control in a grid tied voltage source converter which mainly include voltage mode and current mode control. The voltage mode control is an open loop control structure in which the real power is controlled by phase angle, and amplitude of converter terminal voltage controls reactive power. This control strategy is being simpler and requires no loops. However as there is no loop closed on current therefore the system is always at the stake of over currents. However current mode control discussed by [66] adopts the strategy in which the converter AC side current is controlled through the converter terminal voltage using an inner control loop and later the active and reactive power are controlled by the angle and magnitude of converter AC side terminal current. The above mentioned technique is also recognized as Vector control. It provides current regulation, protects VSC in overload conditions, provides robustness against system parametric changes (either VSC itself or AC side dynamics) and higher control accuracy. In [19], voltage and current modulators are demonstrated to control the output voltage and current of modular multilevel converter. The current modulators provide fast dynamic response but it does not work with constant frequency therefore filtration is difficult with current modulators. The voltage modulator uses constant frequency, their filter requirements are simpler therefore these modulators are most commonly used.

## 2.7 SPWM

Single and multiphase inverters commonly use the Sinusoidal pulse-width modulation (SPWM). In this technique, the modulating wave which is a reference of the desired sinusoidal waveform is compared to the carrier wave which is a triangular waveform having much higher frequency. The comparator outputs the signals to

drive switches which cause multiple on-off of the converter switches in each half-cycle with variable pulse width to generate a load voltage having modified sine wave. The pulse width starts from a very narrow width initially in every cycle and increasing to a maximum width in the center of each cycle. Then the pulse width starts reducing again after maximum to its minimum width where the period of the half-cycle ends [67]. Figure 2.15 shows the basic SPWM generation.

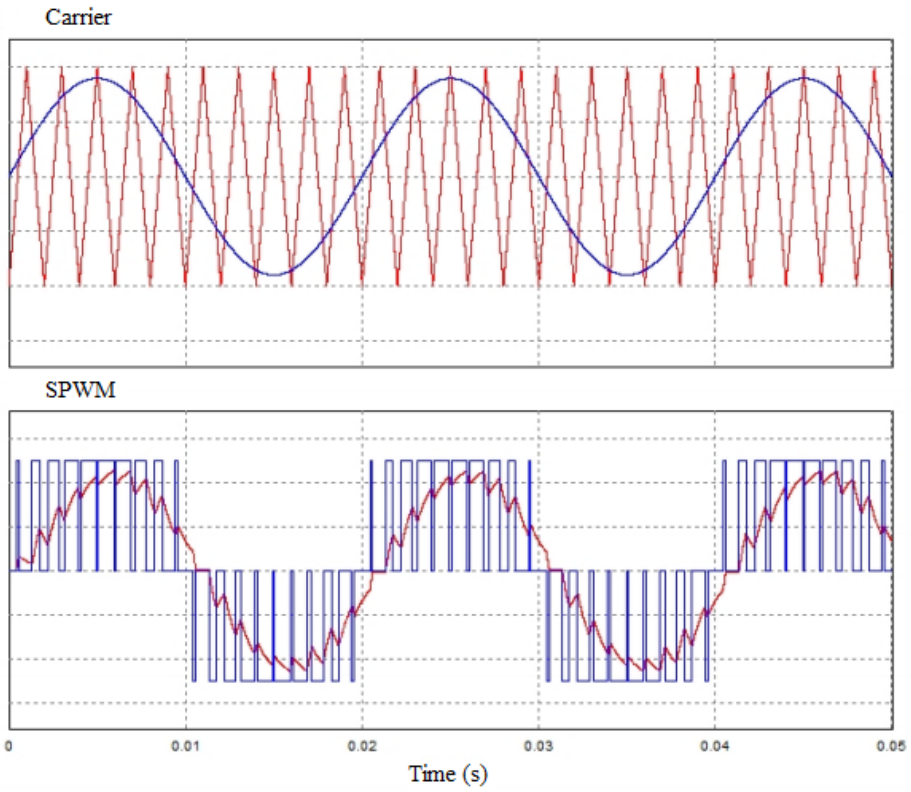



FIGURE 2.15: SPWM Generation technique

By adjusting a time average of voltage level of two-level converters, variable frequency and amplitude voltage waveform can be generated, usually performed with the technique discussed above. On the far side, multilevel converters provide a different phase of waveform generation, allowing more choices to produce the output waveform where utilization of the voltage levels as a further control option [16]. Merging the two concepts of SPWM and Multilevel switching, we can achieve SPWM for multilevel converters. By this we can achieve different levels by switching them in sinusoidal pattern. Figure 2.16 shows the basic switching output of nine level converter.

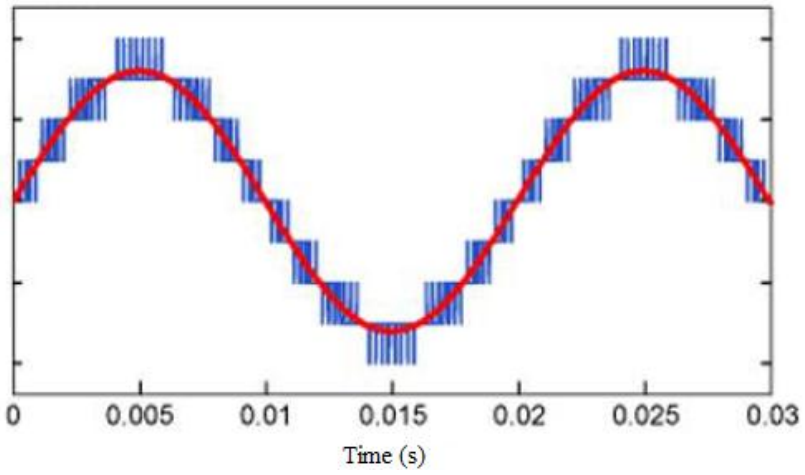



FIGURE 2.16: Nine-level MMC SPWM Converter Output

## 2.8 Gap Analysis

The changing trend of power delivery from HVAC towards HVDC has forced the need of efficient and reliable converters for HVDC applications as HVDC systems has number of advantages over HVAC systems whereas protection issues remains a big challenge. Voltage source converter (VSC) systems are based on self-commutating switches, typically insulated-gate bipolar transistor (IGBT) technology, which have a number of advantages compared with thyristors.

Due to high power quality and modularity of Modular Multilevel Converters (MMCs) they have now become very suitable for medium and high power applications. The building-block cell is the basic unit (Sub-Module) of any multilevel modular converter. Various types of cells are being used in literature such as the half-bridge, full bridge, modified full-bridge, cross-connected SM, clamp double SM, asymmetrical SM, mixed cells, modified mixed cells and Switched-Capacitor Sub-Module. The choice of sub-module is very important based on the number of semiconductors, required voltage sensors and DC fault blocking capability keeping in view the cost, reliability and efficiency of the converter.

Among the three solutions for DC fault isolation, converter fault blocking capability solution is found better for which sub-module must have capability of DC fault

blocking. Switched-Capacitor Sub-Module is found to be suitable for this purpose but the most important technical barrier that limits its application in MMC is its practical implementation for a conventional controller. SCSM has more number of semiconductors which requires unique and unusual switching pattern for the desired output. This in results raise the requirement of PWM signals which increases the requirement of controller outputs. The unique and unusual switching pattern requires sophisticated lookup tables and switching algorithms which in results requires more computational power and makes the control philosophy more complex where reliability maybe compromised. These all stated problems makes the implementation of SCSM practically difficult hence raise the demand of a modified controller which can have a bridge between the MMC conventional controller and SCSM to be operated practically.

## 2.9 Problem Statement

Selection of sub-module for multi-level modular converter keeping in view the DC fault blocking capability, cost, reliability and efficiency. The selected sub-module i.e. SCSM requires extra control signals due to the fact of having more number of semiconductors in unique pattern. This requirement will increase the control complexity and will add more computational burden because of sophisticated lookup tables making the implementation practically difficult. To overcome the stated gap, designing of logic converter that can modify the conventional cascaded half bridge based controller for its direct interface with selected sub-module power stage. It is desired to operate the nine-level HVDC-MMC tied to AC Grid for which it can have active and reactive power control at common grid terminal with DC side fault blocking capability without changing the control philosophy.

## 2.10 Chapter Summary

This chapter investigated the demand of HVDC systems and the contribution of two-level and multi-level voltage source converters in commercial HVDC systems. Concept of multilevel modular converters is also explained along with its advantages and types of sub-modules being used in MMCs. Literature work for DC side faults along with their solutions are also identified. In the end the gap of this work with the previously done work, which is identified through literature, is provided and based on this gap, the problem statement for this thesis is described.

# Chapter 3

# Implementation

## 3.1 Introduction

This chapter gives comprehensive details of working principles of switched-capacitor sub-module (SCSM) and its switching requirements. Based on these principles, a logic converter is developed to interface the SCSM based power stage with half-bridge based nine-level MMC controller. Mathematical model of MMC when tied to grid is also presented along with the simulation model in Matlab/Simulink 2018a environment. In the end section of this chapter the model used for the grid connection and control of converter is also presented and discussed briefly.

## 3.2 Switched-Capacitor Sub-Module (SCSM)

In this work Switched-Capacitor Sub-Module (SCSM) [23] has been selected as an appropriate sub module for grid tied MMC. The selection is based on the comparison being presented in Table 2.3 of previous chapter which involves the number of semiconductors, voltage sensors and DC fault blocking capability.

Switched-Capacitor Sub-Module (SCSM) is a three-level unipolar cell. The SCSM has six IGBTs and two capacitors which is equivalent to the conventional cascaded

two half bridge sub modules, each comprising of two IGBTs. The SCSM can be operated with a lesser number of required voltage sensors (50%) when compared with other MMC sub-modules, and can block DC side faults..

The SCSM comprises of two identical capacitors which can have connection in series or parallel. The sum of voltages can be attained by enabling series connection ($V_{SM} = E_1 + E_2$) while output voltage is equal to single capacitor voltage in parallel connection ($V_{SM} = E_1 = E_2$). Bypassing the sub-module results the Zero output voltage ($V_{SM} = 0$). In other three-level cells, to produce a voltage $E$, either of two capacitors is added in path which causes imbalance in capacitor voltages and to monitor their voltages two separate sensors are needed. The difference in the case of SCSM is the enabling of parallel connection for obtaining the $E$ voltage which forces the voltages of both capacitors to be same and a single sensor is enough to monitor capacitor voltages.

Both capacitors are connected in series for the generation of $2E$ voltage where the two capacitors are matching. Both capacitors will hold same voltage from the preceding parallel connection having the same current path with $E$ voltage and, therefore equal voltages of capacitors can be assured. Small deviations anticipated in the capacitor voltages which will be removed in the next following parallel connections for the $E$ output voltage are due to any discrepancy between the capacitances and their operative series resistances. Following sub sections presents the complete working principles of Switched-Capacitor Sub-Module (SCSM).

### 3.2.1 Architecture of SCSM

Architecture of Switched-Capacitor Sub-Module is shown in Figure 3.1. Switched-Capacitor Sub-Module is a three level unipolar cell where three voltage levels can be achieved with single positive polarity with respect to any arbitrary reference. It comprises of six power electronic switches that are Insulated Gate Bipolar Transistors (IGBTs) with anti-parallel diodes to avoid any negative voltage across the switch. Wide rating range of IGBT and its anti-parallel diode is available in a

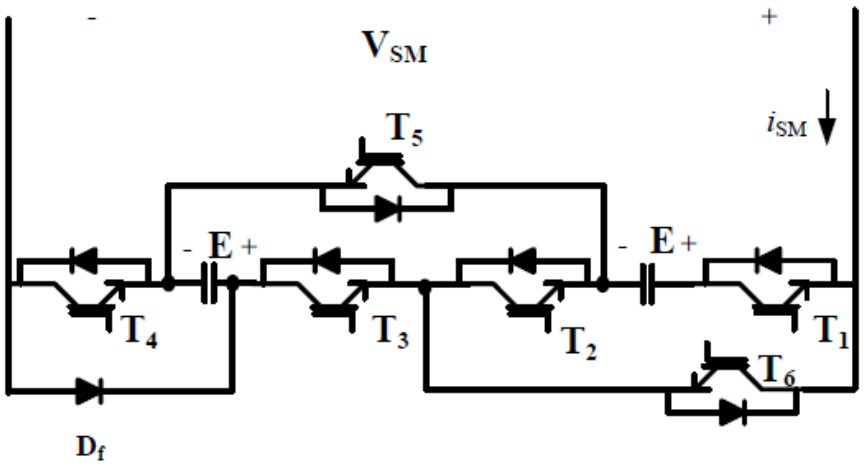



FIGURE 3.1: Architecture of Switched-Capacitor Sub-Module

single package commercially. Two equal rating capacitors are used as two independent passive voltage sources which can be connected either series or parallel. Parallel or series connection of these two capacitors can be achieved through the proper switching of given IGBTs of the module. One extra diode is also the part of the cells architecture for the reverse current in case of all switched off IGBTs. The overall voltage rating of cell becomes $2E$ as all components have the voltage rating of $E$. SCSM working can be allocated into two main parts i.e. normal operation and fault operation, which are explained in the next sub sections.

### 3.2.2 Normal operational modes of SCSM

The three normal modes of operations can be achieved using SCSM architecture which guarantees the voltages of the cell capacitors to be equal. The three voltage levels which can be obtained from the SCSM are 0, $E$ and $2E$.

For obtaining Zero output voltage, the cell is bypassed by switching on the four IGBTs where the remaining two are turned off. Figure 3.2 shows the switching pattern for the cell's transistors to achieve Zero voltage along with its equivalent circuit.

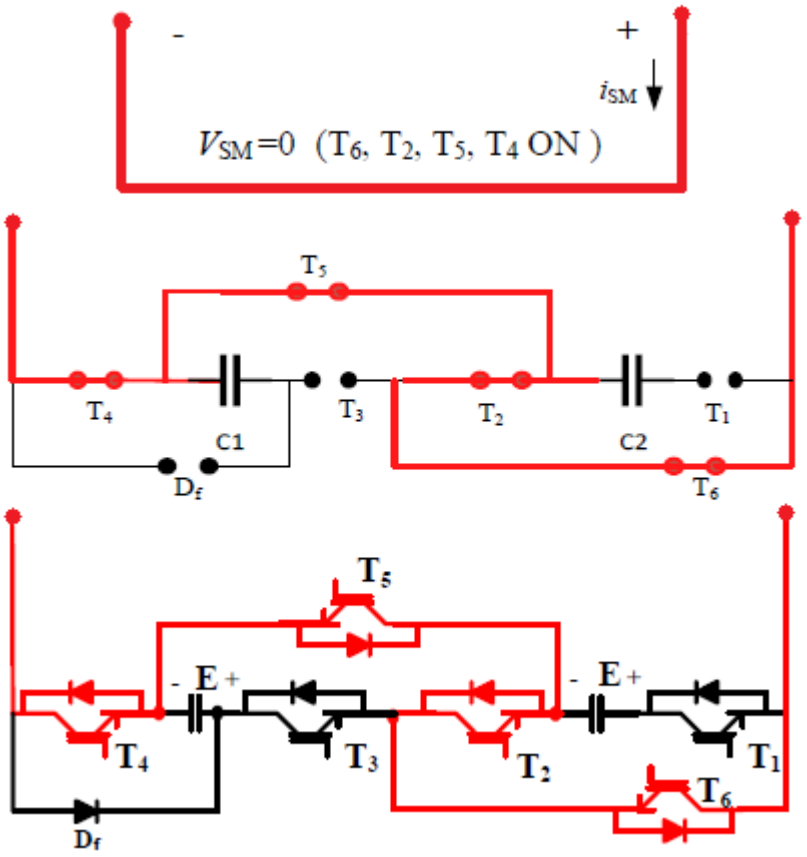



FIGURE 3.2: Switching pattern and equivalent circuit during *Zero* voltage state

The $E$ state is obtained by enabling the parallel connection of the two capacitors inside the cell. For this case, five IGBTs are turned on and only single IGBT remains off. SM current is divided into two identical branches, and as a result of parallel connection the voltages of both capacitors are forced to be equal, and due to this parallel connection only one voltage sensor is enough to see capacitor voltages. Figure 3.3 shows the switching pattern for the cell's transistors to achieve $E$ voltage along with its equivalent circuit.

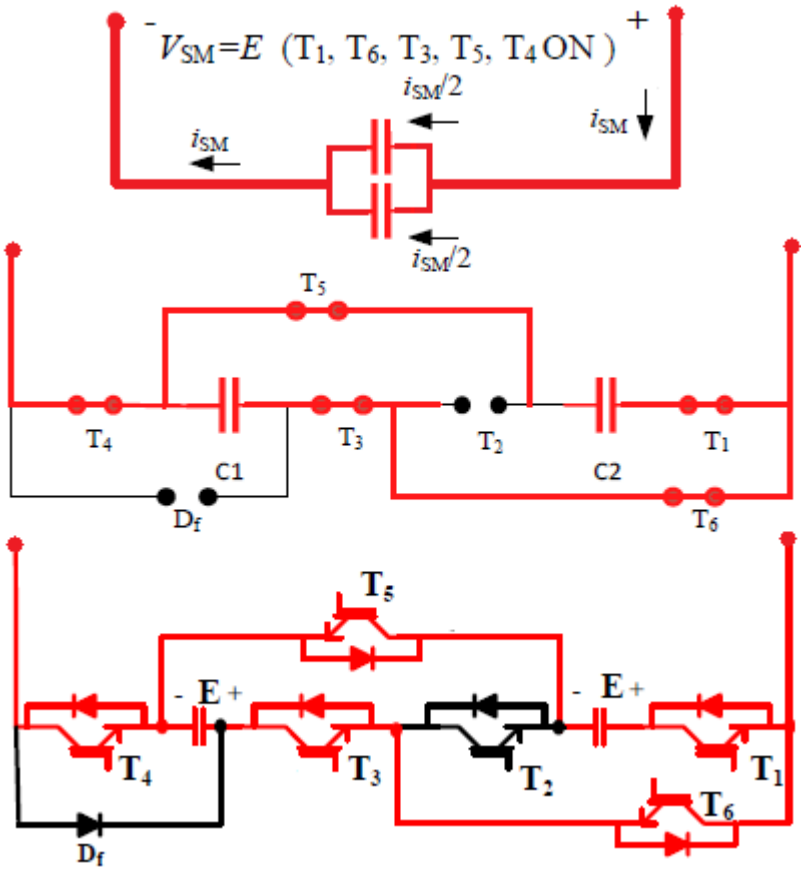



FIGURE 3.3: Switching pattern and equivalent circuit during $E$ voltage state

The last and final $2E$ voltage state is obtained by making the series connection of the two capacitors inside the cell. For this voltage state, four capacitors are turned on, two capacitors are turned off and the sub-module current passes through the two series connected capacitors. Due to the former parallel connection both capacitors had the same initial $E$ voltage, so the effect of the SM current on the capacitors voltages will be similar and this series connection will guarantee the equal voltages of both capacitors

Minor variations between the voltages of series connected capacitors is likely to be expected because of the possible manufacturing gaps and tolerances. The succeeding $E$ state will, however confirms that the equal voltages are reestablished, hence building-up of voltage differences will not happen. Figure 3.4 shows the switching pattern for the cell's transistors to achieve $2E$ voltage along with its equivalent circuit.

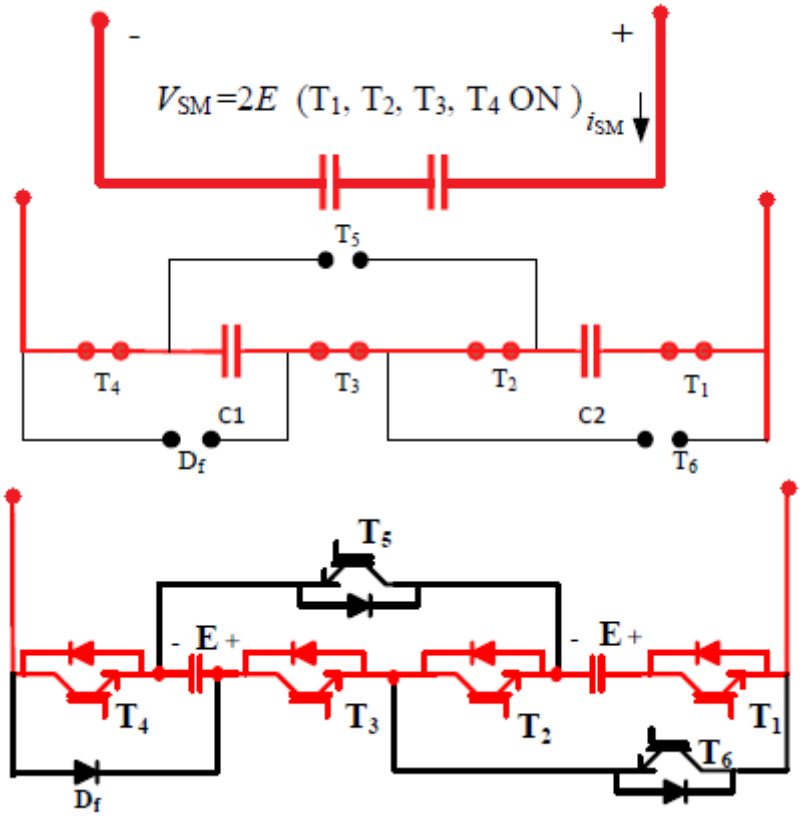



FIGURE 3.4: Switching pattern and equivalent circuit during $2E$ voltage state

### 3.2.3 DC side fault blocking

Blocking of DC side faults is offered by SCSM for Grid-tied MMC based systems. To avoid and protect the MMC from any AC side contribution into the DC side fault, all IGBTs of the MMC should be turned off as soon as the DC fault is discovered. The performance of the proposed SCSM when all IGBTs are turned off is shown in Figure 3.5. Based on the direction of arm current at the initial instant at which the IGBTs are turned off, the current can pass through the SMs diodes as shown in Figure 3.5a for positive arm (SM) current, and in Figure 3.5b for negative arm (SM) current. Current will not be interrupted suddenly by the turning off the IGBTs but capacitors will ultimately block the DC current as shown in Figure 3.5c. It is rather clear that the SCSM can block any AC current contribution into the DC side fault due to opposing voltage to the grid when the

arm current is negative. This property allows engagement of the MMC in power systems without expensive HVDC circuit breakers.

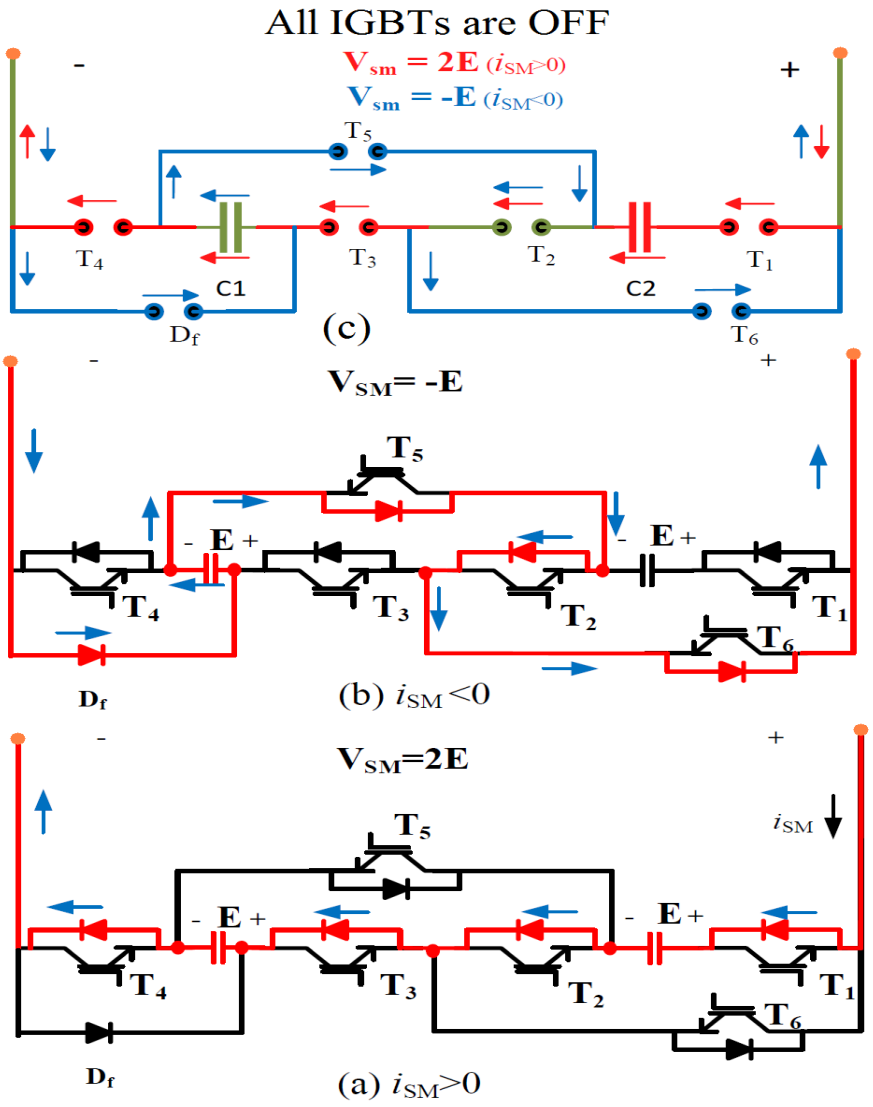



FIGURE 3.5: Switching pattern and equivalent circuit during DC Fault

## 3.3 Working principle of cascaded Half-Bridge based MMC

The basic purpose of this work is to interface the Switched-Capacitor Sub-Module based power stage to a cascaded conventional half-bridge based MMC grid tied controller so that it behaves exactly the same, along with DC side fault tolerant

operation. For this purpose basic working principle of half-bridge based MMC is given in following sub sections.

### 3.3.1 Pulse Width Modulation (PWM)

Power electronic switches of the half bridge converters usually use Pulse width modulation (PWM) for their switching requirments. There are number of different techniques used for the switching of VSCs but the basic techniques follow space vector modulation, selective harmonic elimination and sinusoidal pulse width modulation (SPWM) [68]. Sinusoidal pulse width modulation (SPWM) is usually used for its ease and simplicity [69]. It uses a high frequency carrier and compares it to the low frequency modulation signal, the moments where modulating signal crosses the carrier signal describes the switching instants for the switching devices. While conidering a converter with upper and lower switches, at those instances where the amplitude of carrier is greater than the modulating signal, a turn off command is given to upper switch say $Q_1$ whereas when the modulating signal gets greater amplitude than the carrier wave, turn on command is given to $Q_1$ [66]. The lower switch $Q_4$ behaves in a complementary manner to that of upper switch cell $Q_1$. The amplitude of carrier fluctuates between 1 and -1 over the time period of $T_S$. The switching function is defined as follows [10, 66];

$$S(t) = \begin{cases} 1; \text{ if conduction mode of switch} \\ 0; \text{ if blocking mode of switch} \end{cases}$$

This implies that

$$S_1(t) + S_4(t) = 1 \tag{3.1}$$

Where $S_1(t)$ denotes the switching function for $Q_1$ and $S_4(t)$ denotes the switching function for $Q_4$. Figure 3.6 shows the basic operation of pulse width modulation.

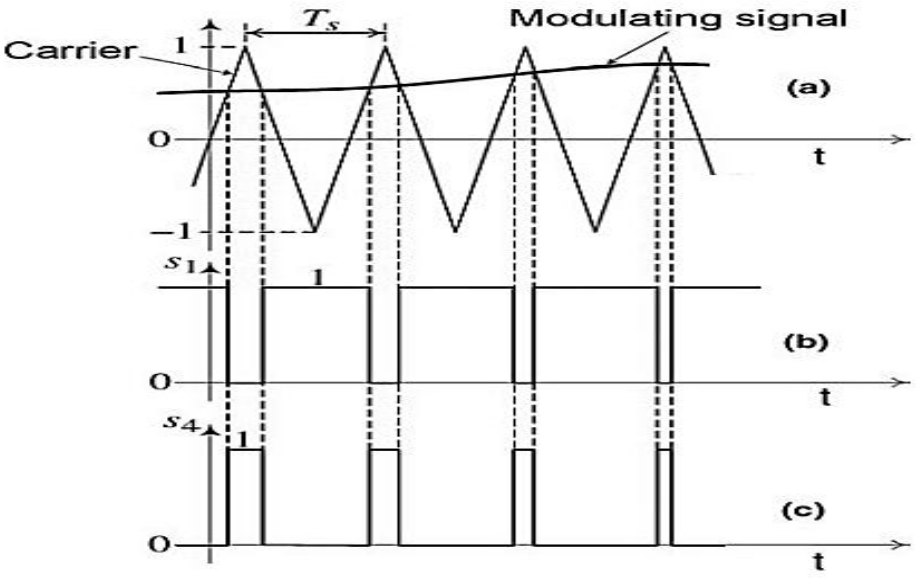



FIGURE 3.6: Basic operation of PWM used for converter switching [66]

### 3.3.2 HB-SM Modular Multilevel Converter

By adjusting a time average of voltage level of two-level converters, variable frequency and amplitude voltage waveform can be generated, usually performed with the technique discussed above. On the far side, multilevel converters provide a new phase of waveform generation, giving more choices to generate the output waveform where allowing the use of the voltage levels as a further control portion. Merging the two concepts of SPWM and Multilevel switching, we can achieve SPWM for multilevel converters. By this we can achieve different levels by switching them in sinusoidal pattern. The basic configuration of N + 1 level single phase half bridge based MMC is shown in Figure 3.7.

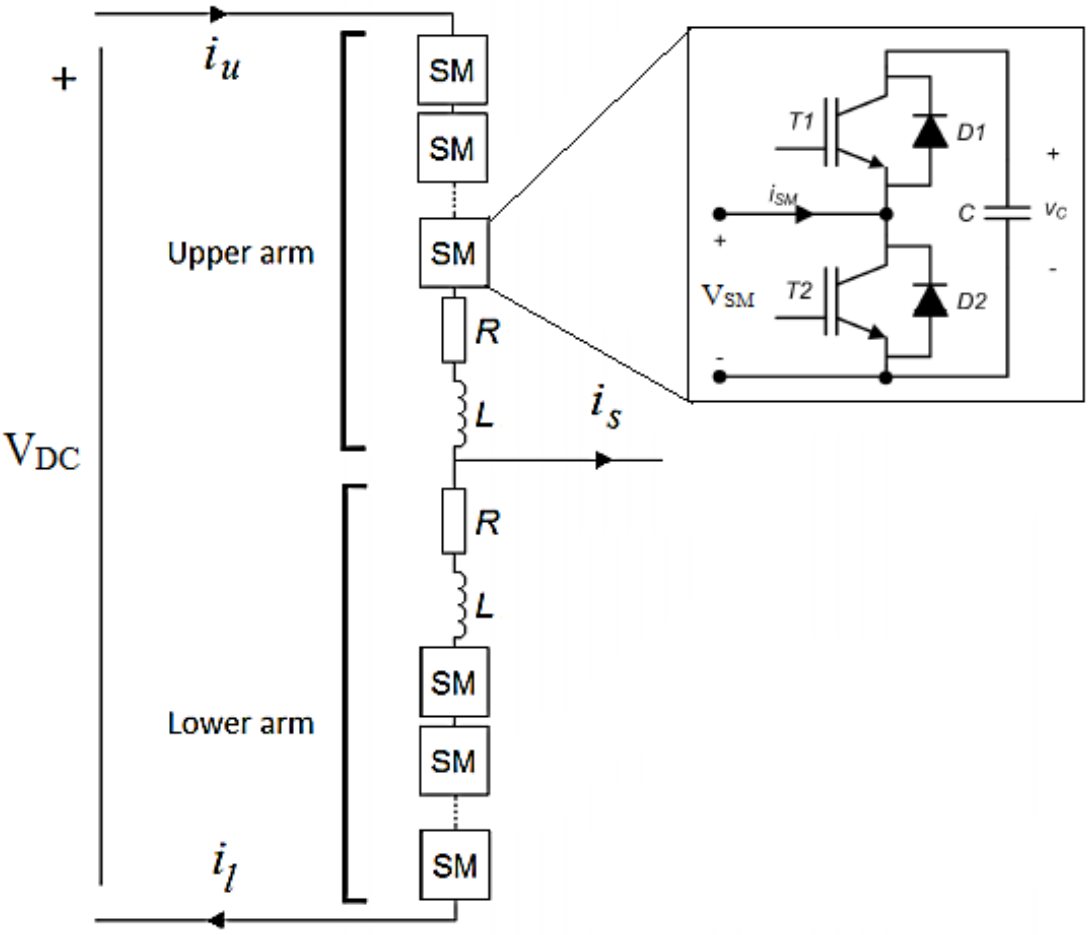



FIGURE 3.7: Basic Structure of HB-SM based MMC

MMC as its name indicates that it is a multilevel converter topology which comprises two arms i.e. an upper arm and a lower arm per leg/phase. Each arm consists of N-1 series connected sub-modules (SM) which corresponds to N voltage levels or steps in the output line to neutral voltage waveform [70] . To limit the circulating current, losses and current rating requirements energy balance between arms is necessary. Many methods have been used in literature. An arm reactor (L) in each arm is used to suppress the circulating currents which arise due to the difference between the phase leg and DC voltages and also minimizes the fault currents during DC side faults.[37]. Half-bridge sub-module consists of two IGBTs, two diodes, and one capacitor. The SM is ON when $T_1$ is ON and $T_2$ is OFF, while SM is OFF when $T_1$ is OFF and $T_2$ is ON. When the SM is ON, the SM voltage is the same as the SM capacitor voltage, while when it is OFF the voltage is zero. According to the SM state and the direction of the SM current,

TABLE 3.1: HB-SM conduction state, voltages and currents

| **HB-SM State** | $T_1$ **State** | $T_2$ **State** | $i_{sm}$ | $\Delta V_c$ | **Conduction** | $V_{sm}$ |
|---|---|---|---|---|---|---|
| ON | 1 | 0 | $>0$ | + | $D_1$ | $V_c$ |
| ON | 1 | 0 | $<0$ | - | $T_1$ | $V_c$ |
| OFF | 0 | 1 | $>0$ | 0 | $T_2$ | 0 |
| OFF | 0 | 1 | $<0$ | 0 | $D_2$ | 0 |
| BLOCK | 0 | 0 | $>0$ | + | $D_1$ | $V_c$ |
| BLOCK | 0 | 0 | $<0$ | x | $D_2$ | 0 |

the current circulates through the capacitor producing its charge or discharge, or maintains its voltage while not circulating through the capacitor. In DC side fault scenerio, the HB-SM turns OFF all IGBTs but the fault current will be conducted through the freewheeling diodes which is the quotient between the AC voltage and the impedance of the arm inductances[19]. Table 3.1 shows the conduction states, voltage and currents of HB-SM.

## 3.4 Generation of Gate-Pulses for SCSM

In N-level MMC to build one arm, the number of SCSM cells are (N-1)/2 cells. The number of voltage sensors per arm required to measure the capacitor voltages will also be (N-1)/2 sensors which is the fifty percent of sensors needed when compared with the other cells. The measured references and voltages for the N-level MMC are fed to controller for the generation of gate pulses as shown in Figure 3.8. When less number of voltages are given to the controller and less number of PWM pins from controller is used, the computational burden will be minimized.

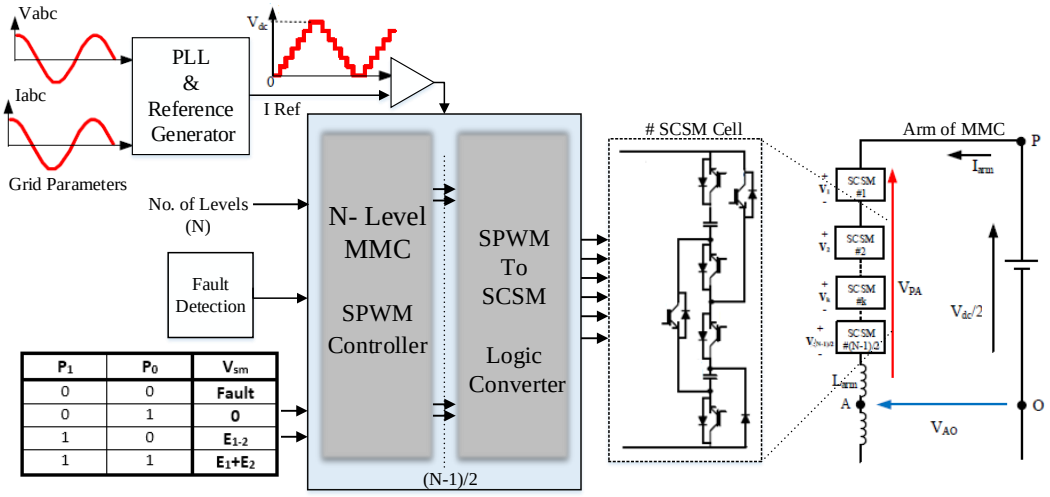



FIGURE 3.8: Gate pulse generation for SCSM (Single Arm)

The SCSM is a three level cell and has six IGBTs and two capacitors which is equivalent to the two conventional cascaded half bridge sub modules, each comprising of two IGBTs. Half bridge requires only single PWM gate signal (inverted PWM to the second switch) but as two half bridge modules are equivalent to a single SCSM so the two PWM gate signals are merged together as input of single SCSM. The SCSM has six switches for this it cannot directly be connected to the two merged output pulses of the controller, so there is a need to convert the two (1+1) cascaded signals into six PWM signals for SCSM. As SCSM has more number of IGBTs, so it requires more number of PWM pulses which will add more computational burden and will require more PWM outputs from controller side.

According to the structure of SCSM it has four possible states and for each state, set of required logic for IGBTs is given. For *fault* state all IGBTs are turned off and to achieve *Zero* state and $2E$ state only two IGBTs are turned off and remaining four are turned on. For state $E$ only one IGBT is turned off and remaining all are turned on. The required switch status for four possible states is given in Table 3.2

TABLE 3.2: Switch status for four possible states

| **SCSM State** | **Fault** | **Zero** | $E_{1-2}$ | $E_1 + E_2$ |
|---|---|---|---|---|
| **IGBT**$_1$ | 0 | 0 | 1 | 1 |
| **IGBT**$_2$ | 0 | 1 | 0 | 1 |
| **IGBT**$_3$ | 0 | 0 | 1 | 1 |
| **IGBT**$_4$ | 0 | 1 | 1 | 1 |
| **IGBT**$_5$ | 0 | 1 | 1 | 0 |
| **IGBT**$_6$ | 0 | 1 | 1 | 0 |

The four possible states are mapped with $2^2$ logic of PWM and for this truth table is made against the two merged PWM outputs from controller that are to be converted earlier to these two sets of PWM. The $2^2$ truth table for the four possible states is given in Table 3.3.

TABLE 3.3: $2^2$ logic for four possible states

| $P_1$ | $P_0$ | **SCSM State** |
|---|---|---|
| 0 | 0 | **Fault** |
| 0 | 1 | **Zero** |
| 1 | 0 | $E_{1-2}$ |
| 1 | 1 | $E_1 + E_2$ |

The main aim is to convert the PWM of a conventional half bridge MMC grid tied Controller to SCSM pulses for which it behaves exactly the same as the output of half bridge MMC without adding any computational burden. The two merged PWM pulses generated from the conventional half-bridge based MMC controller are first converted into $2^2$ logic for four possible states i.e. *fault*, *zero*, $E$ and $2E$. as in Table 3.3. Required conversion logic of PWM pulses to SCSM $2^2$ logic is given in Table 3.4.

TABLE 3.4: PWM Pulses to SCSM $2^2$ logic

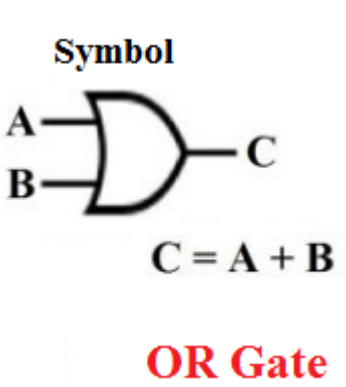
| | **PWM** | $2^2$ **Logic** | **SCSM** | **Voltage Level** |
|---|---|---|---|---|
| $P_0$ | 1 | 1 | $T_1$:1 ; $T_4$:1 | |
| $P_1$ | 1 | 1 | $T_2$:1 ; $T_5$:0 | $E_1 + E_2 = 2E$ |
| **Enable** | 1 | 1 | $T_3$:1 ; $T_6$:0 | |
| $P_0$ | 0 | 0 | $T_1$:1 ; $T_4$:1 | |
| $P_1$ | 1 | 1 | $T_2$:0 ; $T_5$:1 | $E_{1-2} = E$ |
| **Enable** | 1 | 1 | $T_3$:1 ; $T_6$:1 | |
| $P_0$ | 1 | 0 | $T_1$:1 ; $T_4$:1 | |
| $P_1$ | 0 | 1 | $T_2$:0 ; $T_5$:1 | $E_{2-1} = E$ |
| **Enable** | 1 | 1 | $T_3$:1 ; $T_6$:1 | |
| $P_0$ | 0 | 1 | $T_1$:0 ; $T_4$:1 | |
| $P_1$ | 0 | 0 | $T_2$:1 ; $T_5$:1 | **Zero** |
| **Enable** | 1 | 1 | $T_3$:0 ; $T_6$:1 | |
| $P_0$ | x | 0 | $T_1$:0 ; $T_4$:0 | |
| $P_1$ | x | 0 | $T_2$:0 ; $T_5$:0 | **Fault** |
| **Enable** | 0 | 0 | $T_3$:0 ; $T_6$:0 | |

## 3.5 Logic Gate PWM Converter for SCSM

The main aim is to convert the PWM of a conventional half bridge nine-level MMC grid tied Controller to SCSM pulses for which it behaves exactly the same as the output of half bridge MMC without adding any computational burden. Simple logic gates are used for this purpose which makes the conversion simple for which the SCSM can replace any conventional half bridge power stage of MMC and directly be interfaced with controller without changing the control philosophy. Total three type of logic gates are used for this conversion. For the sake of understanding these three gates are discussed briefly in the following sub-sections.

### 3.5.1 OR Gate

To implements logical incoherence OR gate is used which is a digital logical gate. It performs conferring to its truth table. When either or both the inputs to the gate are HIGH (1) output is also HIGH (1). Whereas output is LOW (0) when neither of the input is HIGH (1). Figure 3.9 shows the symbol and truth table of OR gate.




**Truth Table**

| INPUT | | OUTPUT |
|---|---|---|
| A | B | A OR B |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

FIGURE 3.9: OR gate symbol and its truth table

### 3.5.2 XOR Gate

XOR gate (Exclusive OR) is a digital logic gate that gives a true (1 or HIGH) output when the number of true inputs is odd. An XOR gate implements an exclusive or that is, a true output results if one, and only one, of the inputs to the gate is HIGH (1). When both inputs are alike i.e. both are HIGH (1) or both are LOW (0), output results LOW (0). Inequality function is represented by XOR, i.e. the output is HIGH (1) when the inputs are not equal else the output is LOW (0). Figure 3.10 shows the symbol and truth table of XOR gate.

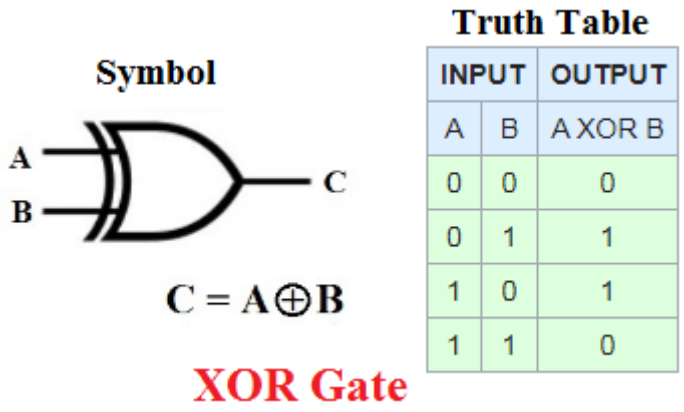



FIGURE 3.10: XOR gate symbol and its truth table

### 3.5.3 XNOR Gate

Digital logic gate that does the logical complement of the exclusive OR (XOR) gate is known as XNOR gate (Exclusive NOR). The gate implements logical equivalence, behaves according to its truth table, and hence the gate is often called an "equivalence gate". When both of the inputs to the gate are the alike a HIGH (1) output results whereas a LOW (0) output results when one but not both inputs are HIGH (1). Figure 3.11 shows the symbol and truth table of XNOR gate.

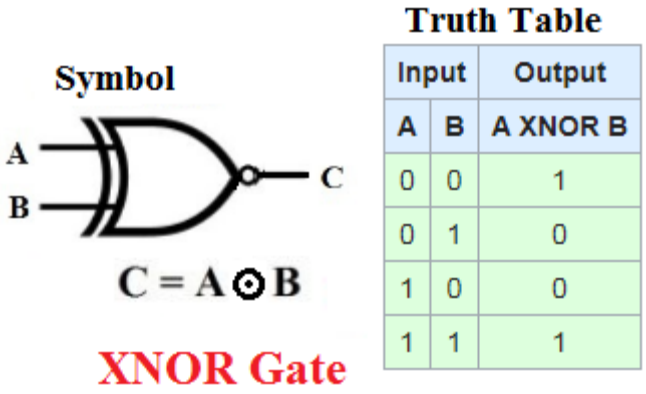



FIGURE 3.11: XNOR gate symbol and its truth table

### 3.5.4 Conversion Principle

The two PWM pulses are first converted into $2^2$ logic for four possible states i.e. *fault*, *zero*, $E_{1-2}(E)$ and $E_1 + E_2(2E)$. The truth table is developed in Table 3.4

for the four possible states against two PWM outputs that will convert the two sets of PWM to $2^2$ logic. Two logic gates OR and XNOR are used for this purpose. Set of two PWM out is given to the two logic gates to convert them to the required logic.

Once the PWM is converted to required $2^2$ logic, it is further translated for the final switching of SCSM. As SCSM has six IGBTs so six pulses are required for the desired operation. $2^2$ logic pulses are further passed from the two logic gates OR and XOR to get six required pulses as per the required switch status given for the four possible states in Table 3.2.

The overall logic converter compromises of four logic gates which has two PWM inputs merged together from the half-bridge MMC controller, and one enable signal. The developed converter gives output pulses for six switches for the desired four possible levels of SCSM. The enable input is a single common signal that will turn off all IGBTs immediately. Complete logical diagram of developed converter is given in Figure 3.12.

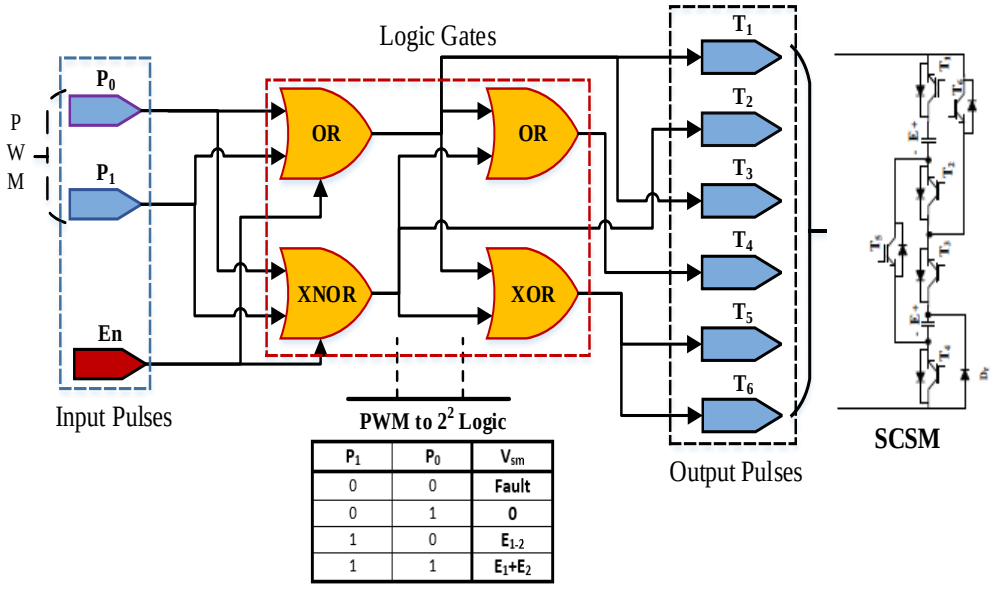



FIGURE 3.12: Logic gate PWM converter for SCSM

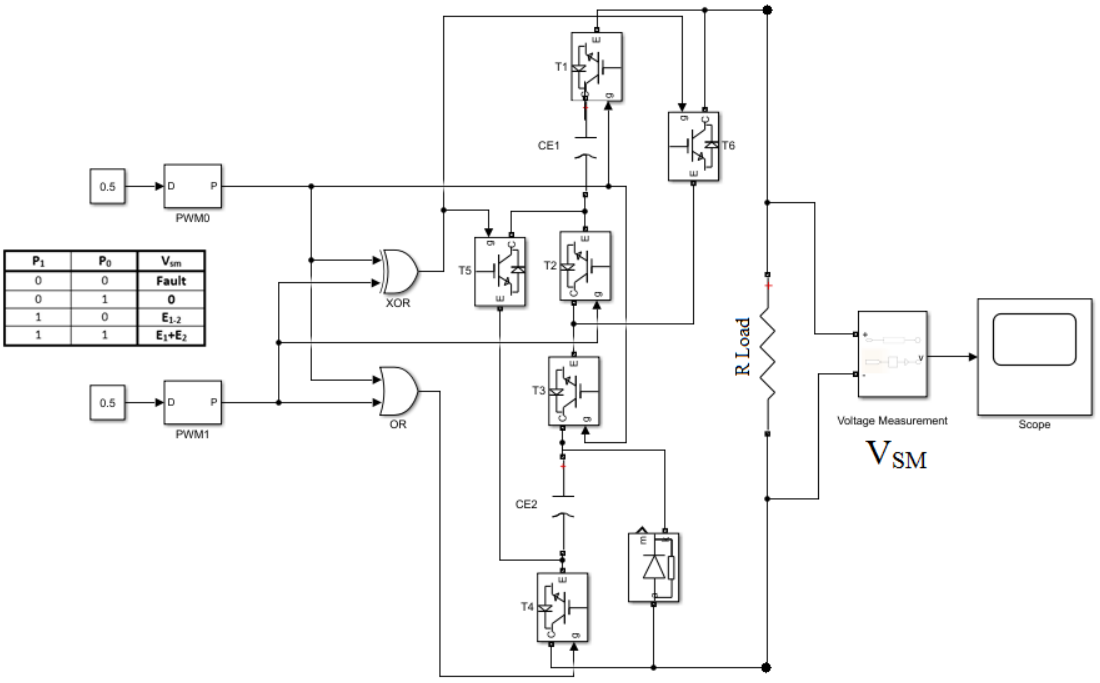
### 3.5.5 Matlab/Simulink Simulation

A simulation model has been developed for the verification of logic converter for SCSM. Switched- Capacitor Sub-Module has been built in Simulink using six IGBTs switch models and two capacitors along with a diode model. PWM are generated using PWM generator and the output voltage of SCSM is measure across a resistive load. Simulation parameters are given in Table 3.5.

TABLE 3.5: logic converter simulation model parameters

| **Description** | **Unit** | **Value** |
|---|---|---|
| Frequency $P_0$ | Hz | 20 |
| Frequency $P1$ | Hz | 10 |
| Duty cycle | % | 50 |
| Load | ohms | 500 |
| Capacitance | mF | 6 |
| Capacitor initial voltage | volts | 100 |

In order to test the logical truth tables as given in Table 3.2 and Table 3.3, two gates are used for the testing of four possible states along with PWM generators. Simulink model and Simulation results are given in Figure 3.13 and Figure 3.14 respectively. Results show the satisfactory response and working of conversion from $2^2$ logic to sub-module IGBT gate switching as per the given logical truth tables.




| $P_1$ | $P_0$ | $V_{sm}$ |
|---|---|---|
| 0 | 0 | Fault |
| 0 | 1 | 0 |
| 1 | 0 | $E_{1-2}$ |
| 1 | 1 | $E_1+E_2$ |

FIGURE 3.13: Simulink model of SCSM

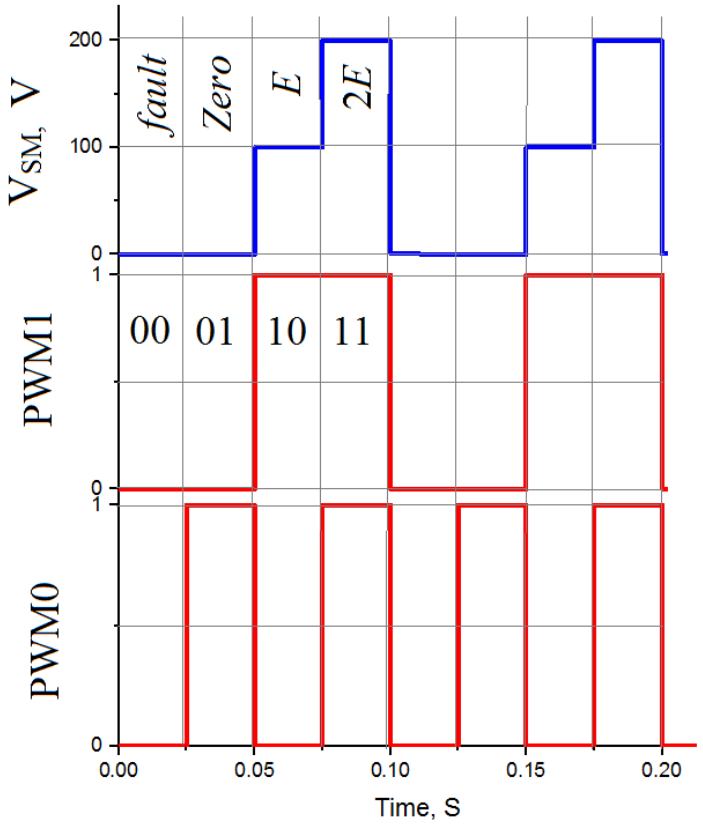



FIGURE 3.14: Waveforms of PWM and Voltage output SCSM

After the successful testing of Switched-Capacitor Sub-Module, Verification of complete logic converter is required as per Table 3.4 which can take PWM out from conventional cascaded half-bridge based MMC controller as input and converts to the required switching pattern of SCSM to achieve all the possible levels. Simulink model and Simulation results are given in Figure 3.15 and Figure 3.16 respectively. Results show the satisfactory response and working of conversion from PWM logic to sub-module IGBT gate switching as per the given logical truth tables.

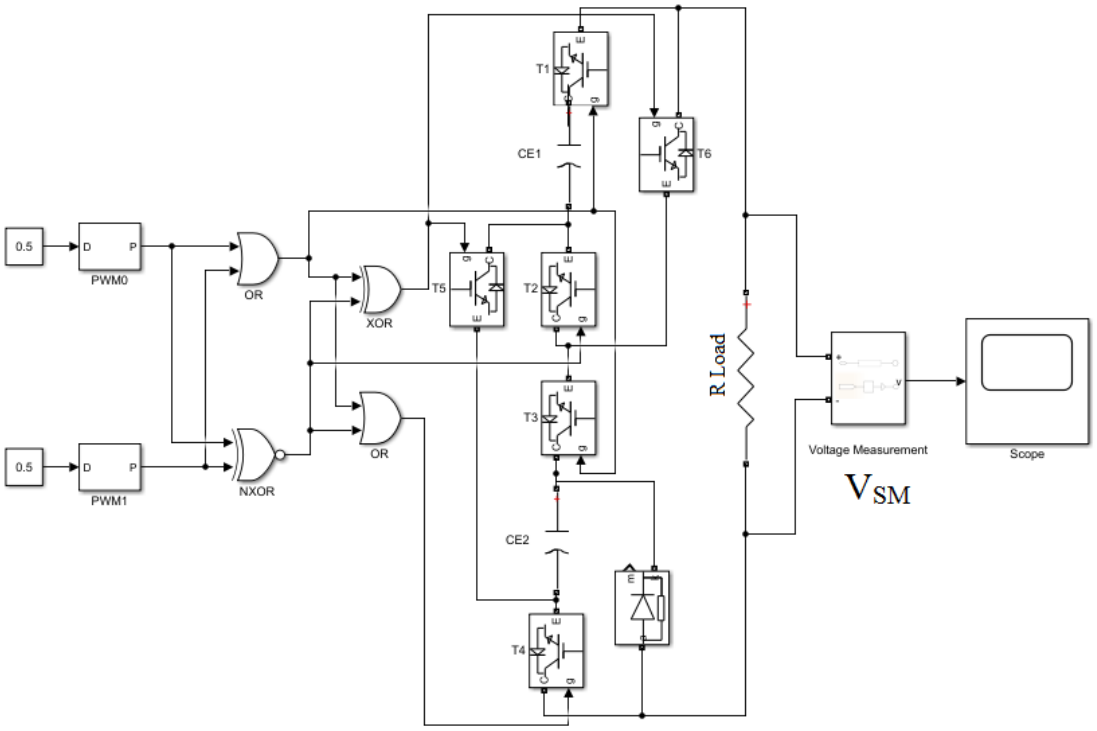



FIGURE 3.15: Simulink model of Logic gate converter for SCSM

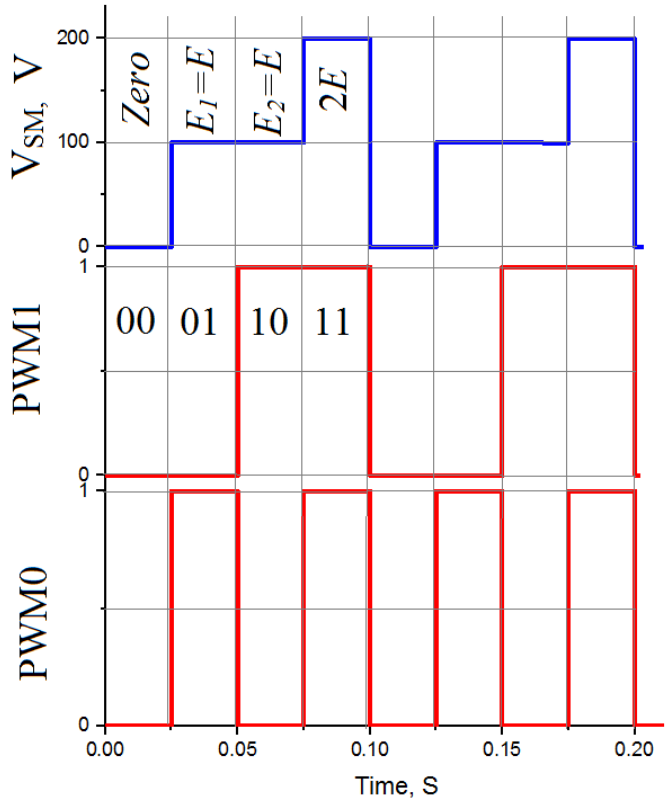



FIGURE 3.16: Waveforms of PWM and Voltage output SCSM

## 3.6 Nine-Level SCSM based Three phase Grid Tied MMC

The selection and verification of SCSM with the designed converter has been tested in the above sections. The power stage based on the SCSM has to be connected now with a Nine-level MMC which is tied to the grid. This section explains the mathematical model of MMC and then presents its simulation model based in Matlab/Simulink environment.

### 3.6.1 Mathematical Modeling

For the mathematical modeling, we consider a basic single phase grid tied MMC configuration as shown in Figure 3.17. The sum of voltages across each capacitor in

upper and lower series connected sub modules are replaced by equivalent variable DC voltage sources separately in both arms [71].

Arm inductance is represented by $L_{arm}$ and the equivalent resistance offered by the arm reactor is represented by $R_{arm}$. . The DC link voltage $V_{dc}$ is split in to two equal halves $V_{dc}/2$ with a separating zero voltage point. The upper and lower arm currents are represented by $i_U$ and $i_L$ respectively.

For improving the quality of output current waveforms and to lessen the AC side high frequency harmonics, the phase reactor used is represented by $R_g + jL_g$. The grid side voltage is represented by $V_s$ whereas $V_t$ and $i_t$ are converter output terminal voltage and current respectively.

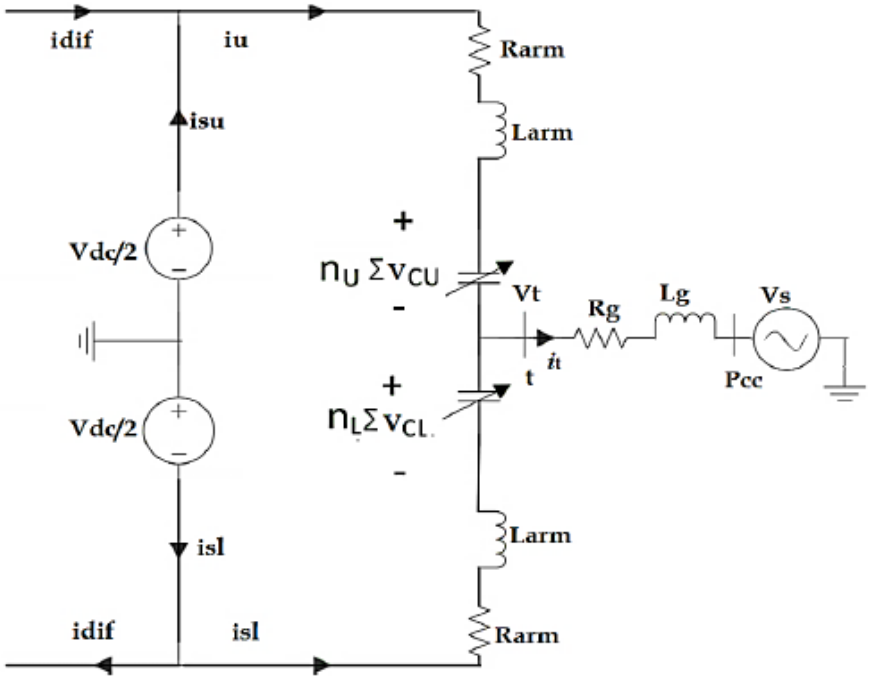



FIGURE 3.17: Single phase MMC equivalent model [71]

The circuit modeling is done on the basis of the assumption that the number of series connected cells and the switching frequency used for the switching of the semiconductor devices is considered infinitive. These assumptions help to develop a continuous model of MMC [71]. Applying Kirchhoff's current law (KCL) in Figure 3.17.

$$i_U + i_L = i_t \tag{3.2}$$

$$i_U = i_s u + i_{dif} \tag{3.3}$$

$$i_L = i_{sl} - i_{dif} \tag{3.4}$$

Substituting 3.4 and 3.3 in 3.2 we get,

$$i_t = i_{su} + i_{sl} \tag{3.5}$$

The difference between the upper and lower arms currents is,

$$i_U - i_L = i_{su} - i_{sl} + 2i_{dif} \tag{3.6}$$

Let $N$ is the total number of series connected cells per arm of MMC and $n_k$ is the insertion index for the sub-modules inserted in the arm where $k = U$ and $L$. Then the voltage of capacitor across each cell $V_c k$ and the total voltage per arm $V_{ck}$ which is the sum of the individual capacitors per sub-modules is represented as [19, 71]

$$v_{ck} = n_k \sum v_{ck} \tag{3.7}$$

If $n_k = 0$, it employs that all cells in the converter leg are bypassed and when $n_k = 1$, it employs that all the cells in the converter leg are included. As $n_k$ ranges from 0 to 1 therefore the number of included cells in the one arm means the bypassing of sub-modules in the other arm. Hence, it is stated as

$$n_U + n_L = 1 \tag{3.8}$$

Applying Kirchhoff's Voltage Law (KVL) in the lower and upper leg in Figure 3.17

$$\frac{V_{dc}}{2} - n_U \sum v_{sk} - V_s(R_{arm} i_{dif} + L_{arm} \frac{d}{dt} i_{dif}) - (L_g \frac{d}{dt} + R_g i_t) = R_{arm} i_{su} + L_{arm} \frac{d}{dt} i_{su} \tag{3.9}$$

$$\frac{V_{dc}}{2} + n_L \sum v_{sk} + V_s(R_{arm} i_{dif} + L_{arm} \frac{d}{dt} i_{dif}) - (L_g \frac{d}{dt} + R_g i_t) = R_{arm} i_{sl} + L_{arm} \frac{d}{dt} i_{sl} \tag{3.10}$$

Suppose the source current in upper and lower arm are equal i.e.

$$i_{su} = i_{sl} \tag{3.11}$$

Therefore combining the fact that $V_s = V_s$ with the assumption made in 3.11 and using in 3.9 and 3.10 which gives,

$$V_s - n_U \sum v_{sk} + n_L \sum v_{sk} = 2(R_{arm} i_{dif} + L_{arm} \frac{d}{dt} i_{dif}) \tag{3.12}$$

From 3.12 $\sum v_{cu} = \sum v_{cl} = V_{dc}$ is a case where the upper and lower arm capacitor voltages are perfectly balanced. This condition implies that the circulating current produces only when there is imbalance between the converter arm voltages. The circulating current becomes zero in steady state if the deviancy of sum of capacitor voltages from the DC link voltage $V_{dc}$ is zero [71]. Substituting the supposition made in 3.11 in 3.5 and later in 3.6 then we get,

$$i_{su} = i_{lu} = \frac{i_t}{2} \tag{3.13}$$

And

$$i_{dif} = \frac{i_U - i_L}{2} \tag{3.14}$$

Substituting 3.13 and 3.14 in 3.9 and 3.10 and then adding the both equations gives,

$$n_L \sum V_{cu} - n_u \sum V_{cl} = 2V_s + 2R_g i_t + 2L_g \frac{d}{dt} i_t + R_{arm} i_t + L_{arm} \frac{d}{dt} i_t \tag{3.15}$$

The output terminal voltage of the converter $V_t$, the resistance $R_{eq}$ and the equivalent inductance $L_{eq}$ is given in 3.16, 3.17 and 3.18 respectively.

$$V_t = \frac{(n_L \sum V_{cu} - n_u \sum V_{cl})}{2} \tag{3.16}$$

$$R_{eq} = \frac{R_{arm}}{2} + R_g \tag{3.17}$$

$$L_{eq} = \frac{L_{arm}}{2} + L_g \tag{3.18}$$

Rewriting the equation 3.15 as,

$$V_t = L_{eq}\frac{d}{dt}i_t + R_{eq}i_t + V_s \tag{3.19}$$

The above equation gives the mathematical model for the AC side dynamics of grid tied single phase MMC. This model is further extended for grid tied three phase system in the following equation 3.20.

$$V_{tabc}(t) - V_{sabc}(t) = L_{eq}d/dti_{abc} + R_{eq}i_{abc}(t) \tag{3.20}$$

$$V_{tabc}(t) = \frac{V_{dc}}{2}m_{abc}(t) \tag{3.21}$$

Three phase output terminal voltages $V_{tabc}$ is represented by equation 3.21 in terms of three phase reference modulating signals$m_{abc}$ for three phase modular multilevel converter [19, 45, 71, 72]. The modulating signals are the control signals that are responsible for synthesizing a controlled N level output voltage waveform [73]. As in this work we are using the control of conventional cascaded half-bridge based MMC we have $\frac{(N-1)}{2}$ sub-modules, as SCSM is a three level cell. As the modulating signal $m(t)$ changes from -1 to 1, in response, the output terminal voltage changes from $\frac{-V_{dc}}{2}$ to $\frac{V_{dc}}{2}$. Equation 3.22 [10, 73] represents the relation for three phase modulating signals as:

$$m_{abc}(t) = \hat{m}cos((\omega t + \theta) + \phi) \tag{3.22}$$

Where $\hat{m}$ represents the modulation index and it ranges from 0 to 1, $\theta$ is the initial phase angle, $\omega$ represents the fundamental frequency in radians and $\phi$ is the angle for three phase AC signals and can take values $\{0, 2\pi/3, (-2\pi)/3\}$ for the respective phases [10, 73].

### 3.6.2 Matlab/Simulink Simulation Modeling

Under this section, the simulation model for 09-level grid tied MMC is presented on the basis of mathematical model developed in the foregoing section. This model is developed in Matlab/Simulink 2018a environment. For N-level MMC the number of series connected SCSM cells to construct one arm is $\frac{(N-1)}{2}$ Cells, so to get nine level output, four sub-modules are connected in series per arm. As SCSM is a three level cell so total twenty-four modules are used as compared to the forty-eight sub modules when half bridge sub module configuration is used. The block diagram of the simulated system is given in Figure 3.18.

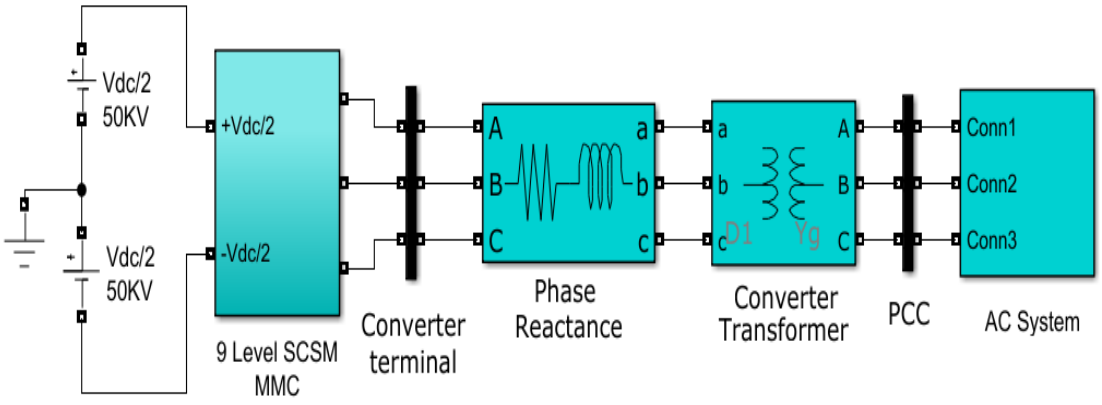



FIGURE 3.18: Simulation model for 09-level Grid tied SCSM based MMC

The DC voltage source $V_{dc}$ = 100 kV is divided into two equal units of the DC voltage $\frac{V_{dc}}{2}$ = 50 kV, having zero volts reference for the whole simulation. All simulation parameters are given in Table 3.6.

The three phase 09-level MMC Simulink model is shown in Figure 3.19. It comprises three phase legs each comprising two arms, an upper one and a lower one. To limit the circulating current, losses and current rating requirements energy

TABLE 3.6: Simulation parameters for 09-level MMC [10, 23]

| **Description** | **Symbol** | **Value** |
|---|---|---|
| DC Voltage Bus | $V_{dc}$ | 100 kV |
| Line Reactance | $R_{eq} + jL_{eq}$ | $0.04\ \Omega + 0.129H$ |
| Transformer Reactance | $R_x + jL_x$ | $0.003\ \Omega + 0.0048H$ |
| Transformer nominal voltages | $V_s : V_P$ | 52 kV : 220 kV |
| Arm Inductance | $L_{arm}$ | 3 mH |
| Arm Resistance | $R_{arm}$ | 1 Ω |
| SCSM Capacitor | C | 6 mF |
| Number of SCSM per arm | $(N-1)/2$ | 4 |
| Output peak voltage | $V_p$ | 50 kV |
| Voltage across each capacitor | $E$ | 6.25 kV |

balance between arms is necessary. Many different ways have been adopted in literature. To get the desired circulating current peak, proper arm inductor along with a resistor is used to limit the circulating current [74]. The arm inductance L_ku for upper arm is equal to the arm inductance L_ku has the value of 3 mH. Therefore the equivalent resistance offered by the arm reactor is also same in upper and lower arm i.e. R_ku = R_kl and it is chosen 1 ohm [10].

The voltage across each capacitor $E$ in a sub-module is 6.25 kV. The upper and lower arm in each phase leg consists of four series connected Switched-Capacitor Sub-Modules (SCSM). These series connected SCSMs are collectively represented by a block named as SMuk for upper arm and SMlk for lower arm where $k$ represent the three phases {a, b, c} respectively.

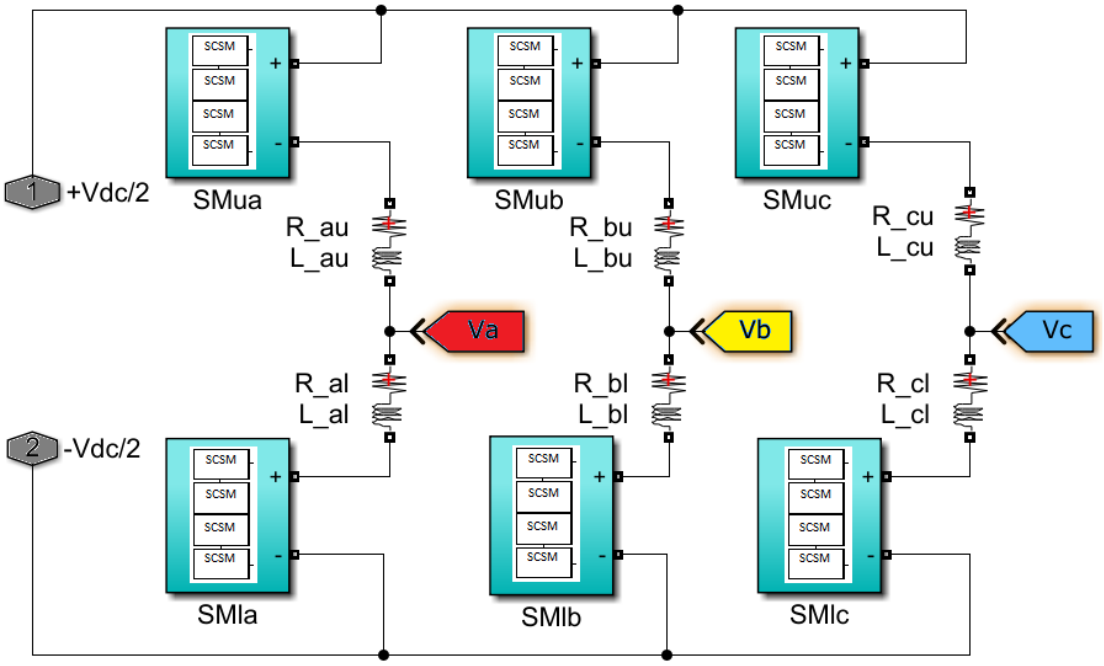



FIGURE 3.19: Simulation model for three phase 09-level SCSM based MMC

The simulation model for SCSM based single phase arm is also developed in Matlab/Simulink. The two gate pulses are merged together and provided to logic converter for the required switching of SCSM. These SCSM are connected in series in the each arm of the converter where each sub-module corresponds to a discrete voltage step in the converter output voltage. The 09-level MMC uses four sub-modules per arm to output nine level voltage waveform. The upper arm of 09-level MMC for phase A, uses four series connected Switched-Capacitor Sub-Modules as given in Figure 3.20.

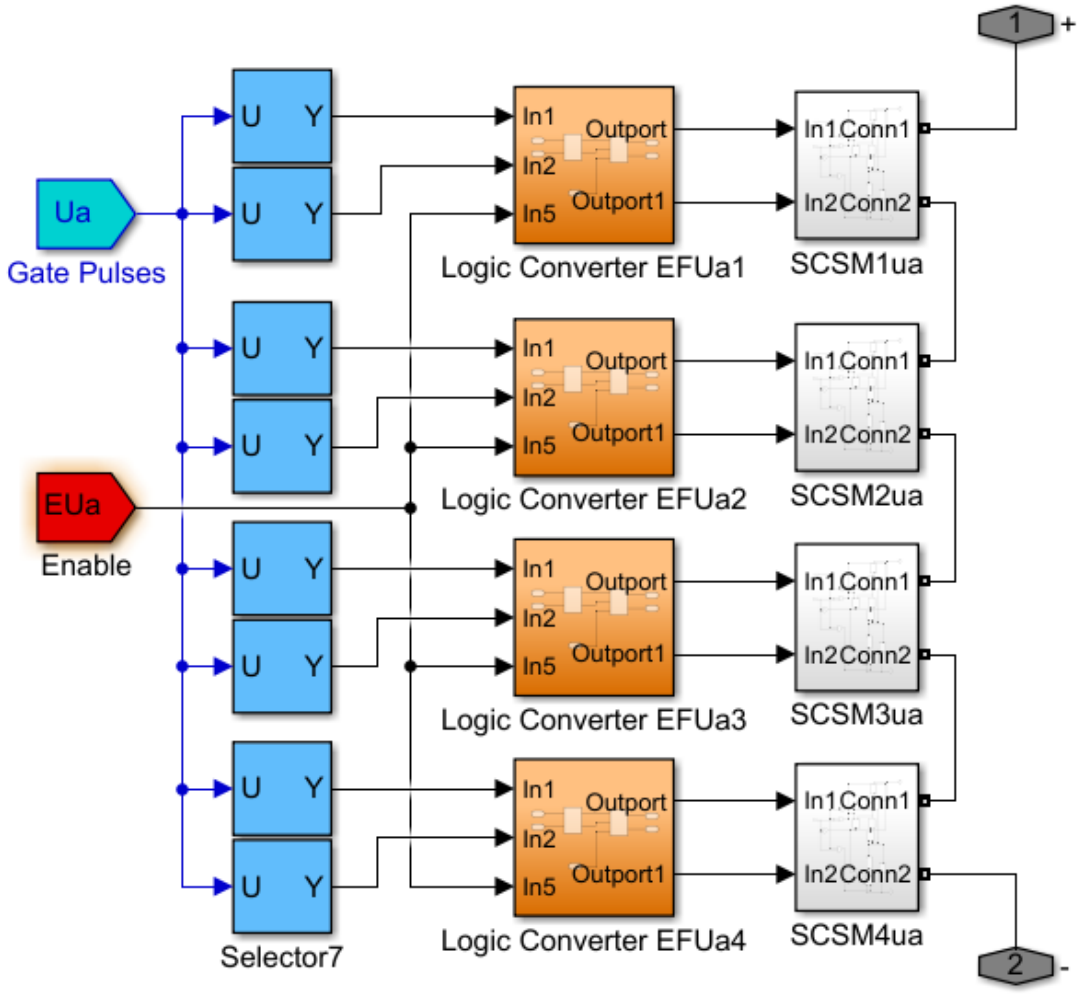



FIGURE 3.20: Simulation model for three phase 09-level MMC single phase arm

## 3.7 220 kV AC Grid Model

To connect the 09-level SCSM based MMC to a AC grid, practical realization is made simply using a balanced three phase symmetrical voltage source. a three phase transmission line joins the AC grid through the grid side bus and connects three phase load. This load is linked to another three phase load through a second three phase transmission line which later on joins with point of common coupling PCC.

### 3.7.1 Matlab/Simulink Simulation Modeling

The simulation model of a 220 kV Grid having nominal frequency of 50 Hz is developed in Matlab/Simulink environment. The grid side bus is used to provide connection between the three-phase transmission lines and the grid whereas it also provides the measurement ports for measuring the three phase grid voltages and currents. All simulation parameters are given in Table 3.7.

TABLE 3.7: AC Grid simulation parameters [10]

| **Description** | **Symbol** | **Value** |
|---|---|---|
| AC Grid Voltage | $V_s$ | 220 kV (r.m.s) |
| AC Grid Current | $I_s$ | 347 A (r.m.s) |
| Grid Frequency | f | 50 Hz |
| Total AC Load | 2 × L | 2×50 MW |
| Transmission Lines | 2 ×$\pi$ | 2× 10 km |

An active three-phase 50 MW load with wye-grounded configuration is connected to the AC grid via transmission line of 10 km. This AC load is linked to another load with similar specifications by means of another 10 km transmission line, which in turn connects the load with the point of common coupling PCC. The block diagram of the simulated system is presented in Figure 3.21.

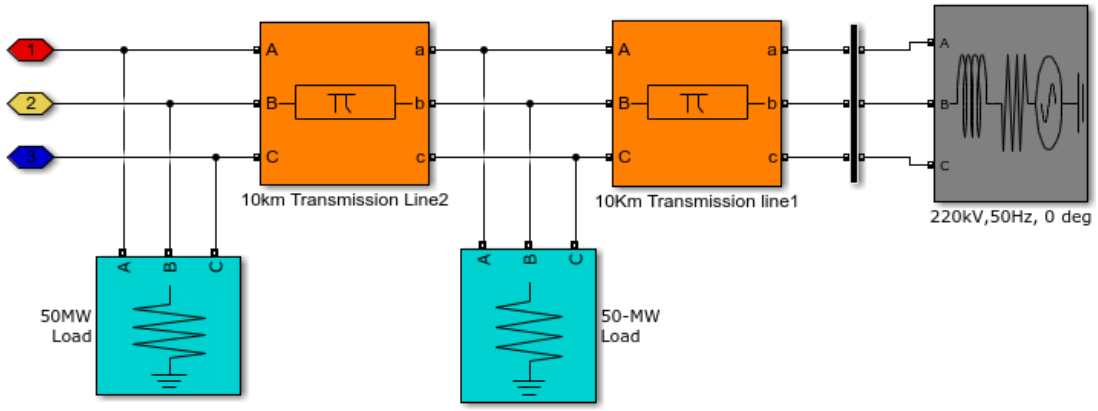



FIGURE 3.21: Simulation model for three phase AC Grid

The instantaneous active power (P) of 100 MW is being delivered by the AC source to the grid connected AC loads of 50 MW each when the converter is in stand-alone mode of operation. The grid power and nominal Grid frequency is shown in Figure 3.22 and Figure 3.23 respectively.

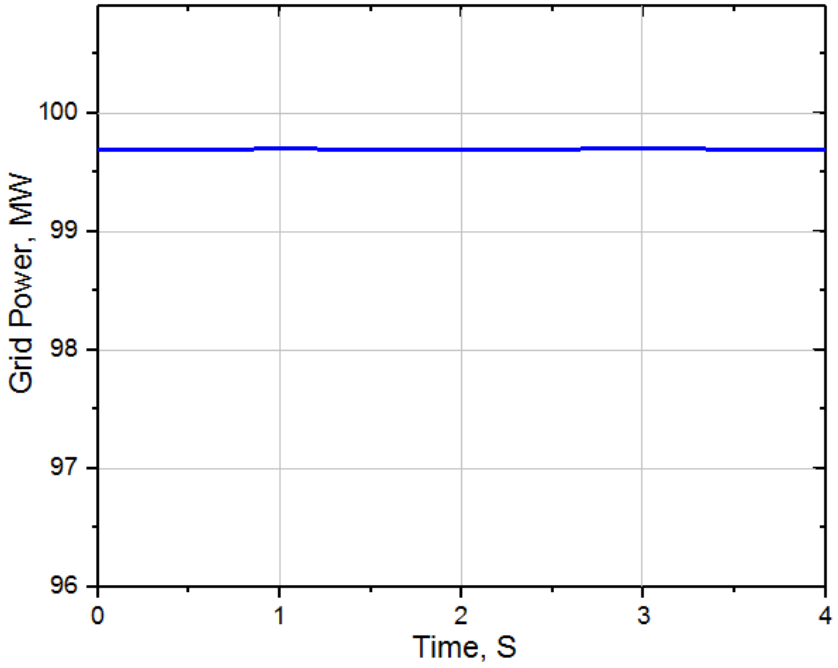



FIGURE 3.22: AC Grid Power in standalone mode of operation

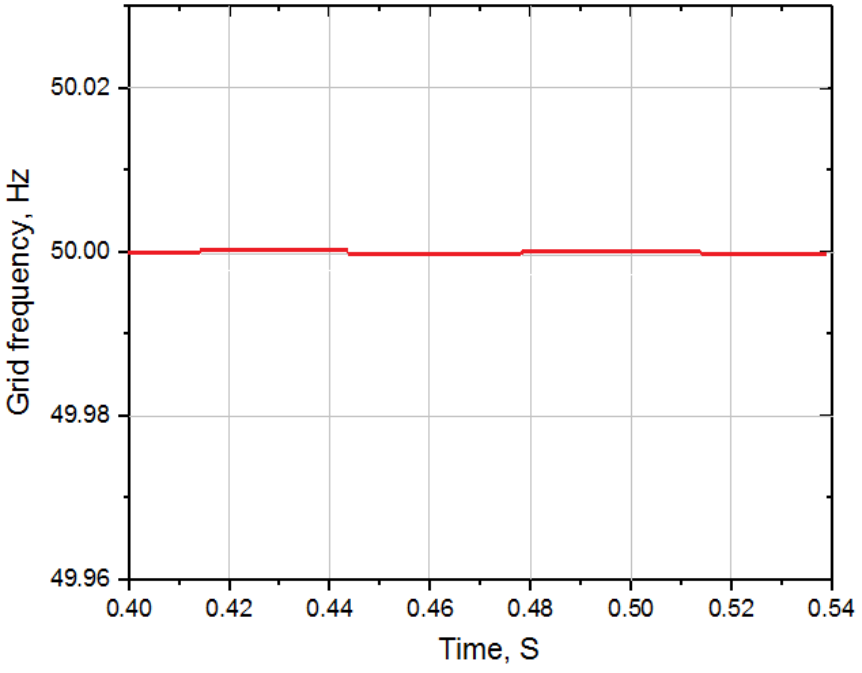



FIGURE 3.23: AC Grid Frequency in standalone mode of operation

The three phase grid voltages and current waveforms obtained from the grid side bus are shown in Figure 3.24 and Figure 3.25 respectively. Simulation results shows the normal operation of AC grid as per the simulation parameters given in Table 3.7.

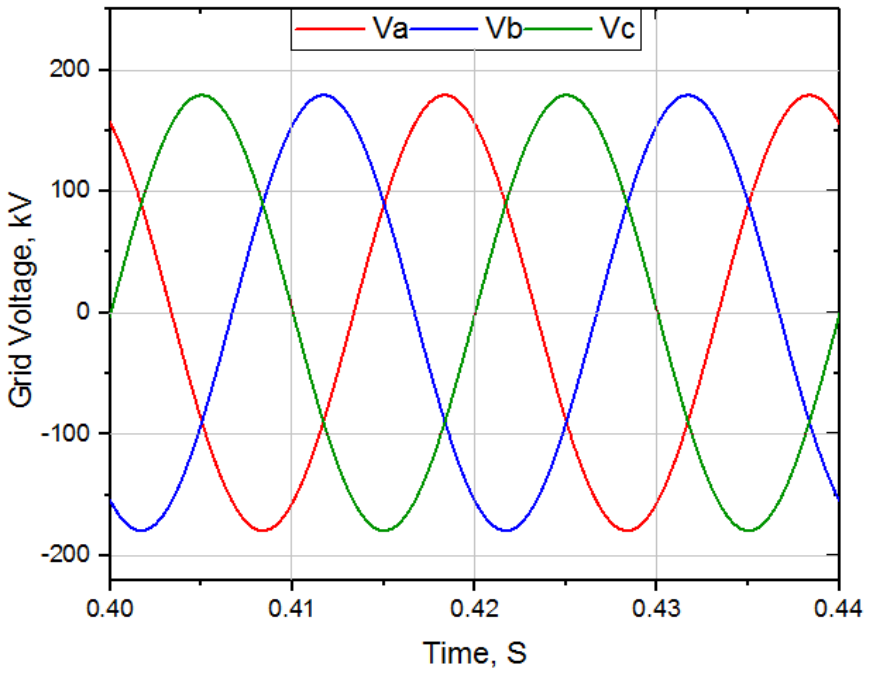



FIGURE 3.24: Three phase Grid voltages measure at Grid side Terminal

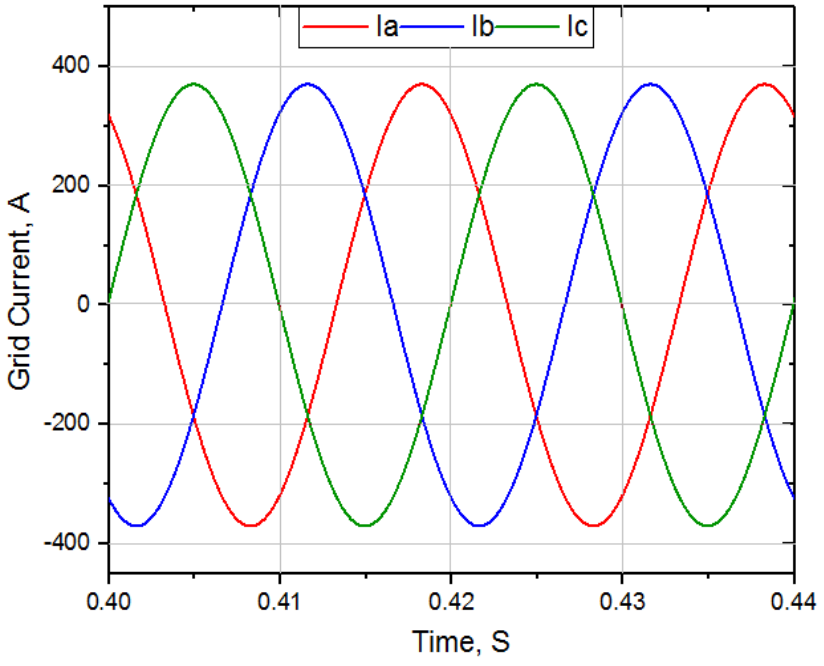



FIGURE 3.25: Three phase Grid Currents measure at Grid side Terminal

## 3.8 Control of Voltage Source Converters

In this section the strategy developed for the design of control structure is discussed for VSC based HVDC systems. As this work is focused to implement the control of half-bridge based MMC, therefore the same control strategy is developed for SCSM based grid tied converter. This control strategy involves the dq0 transformations, Modeling of three grid connected converters in dq0 reference frame, Design of PLL, PI compensator design by using Modulus optimum tuning criteria, Transfer function extraction and control of switching devices [10]. The simulation models of entire control system is also presented by the end of this chapter.

### 3.8.1 Grid Tied MMC System

The control system used for this work transforms the three phase alternating (AC) signals from stationary frame of reference to a rotating reference frame where the vector quantities (signals) are reduced to two constant (DC) vectors [75]. Such transformation is known as direct quadrature or dq0 transformation. The dq0 transformation is a mathematical transformation which is used for the dynamic analysis of three-phase electrical systems because it reduces the complexity and simplifies the system parameters by making them purely dc values. To simplify the control structure design, the three phase mathematical models are transformed to dq0 mathematical model [10] which is beyond the scope of this work. The reference frame model for a grid tied MMC system is shown in Figure 3.26.

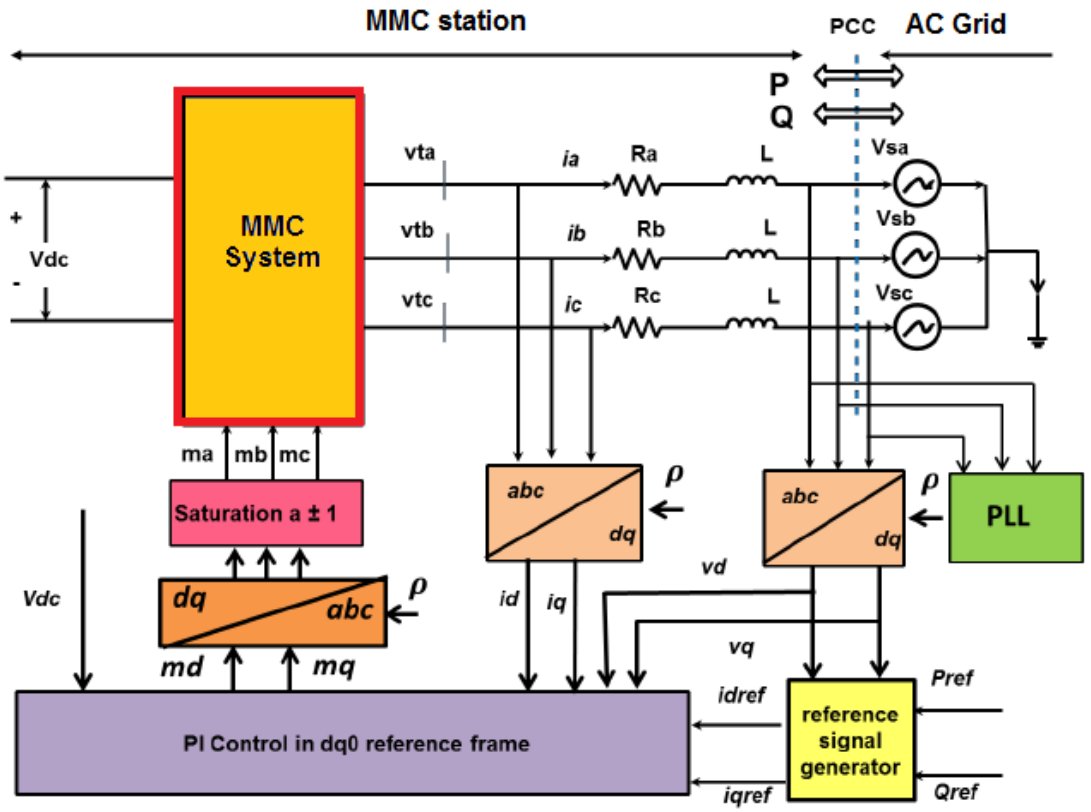



FIGURE 3.26: Model for active/reactive control of MMC in abc/dq0 frame [10, 66, 73]

In reference model L represents the line reactor and R represents the equivalent resistance offered by the line reactor [66]. And $i_d$ and $i_q$ denote the d and q components of converter output current , $V_{td}$ and $V_{tq}$ denote the d and q components of converter voltage of output terminal and $V_{sd}$ and $V_{sq}$ are d and q components of AC grid side voltages respectively. Here $\rho$ is the angle between the ABC stationary frame and dq0 rotating frame of reference and $\omega$ is the angular speed with which the dq0 frame is rotating [73].

Once the grid is synchronized, the active and reactive power can be controlled separately at point of common coupling (PCC) where all the grid voltages and currents are measured. Required synchronization with grid has been achieved by feeding all grid voltages to phased locked loop (PLL). phase locked loop (PLL) has the ability to lock grid phase angle and to regulate the system on the grid frequency [75]. The overall control parameters taken for this work are summarized in Table 3.8.

TABLE 3.8: Control parameters [10, 76]

| Description | Symbol | Value |
|---|---|---|
| Converter Switching Frequency | $f_s w$ | 1650 Hz |
| Average Converter Switching delay | $T_a$ | 0.3 ms |
| Sampling time for converter control | $T_s$ | $6.06e^{-6}$ s |
| Angular Frequency | $\omega$ | 314 rad |
| Frequency | $f$ | 50 Hz |
| Proportional Gain | $K_p$ | 0.683 |
| Integral Time constant | $T_i$ | 10.1 ms |
| Integral Gain | $K_i$ | 67.623 |

### 3.8.2 Matlab/Simulink Simulation Modeling

As per the discussion in the forgoing section and the parameters summarized, a control strategy is developed in Matlab/Simulink environment 2018a. Gate pulse generation and active/reactive power controller is presented in Figure 3.27.

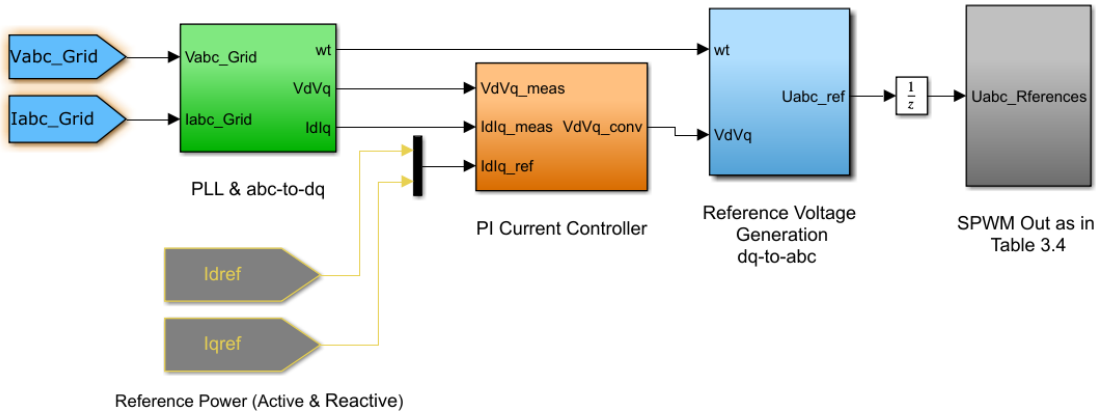



FIGURE 3.27: Simulation model for active/reactive control and PWM generation

The above figure shows that the grid voltages and converter currents are given to the PLL and measurements block which provides the synchronizing angle $\omega t$ and $dq$ transformed grid voltages and currents. The current regulator block is given with the measured dq frame grid voltages and currents along with their references . The current regulator block outputs the dq frame converter output terminal voltages in dq frame which are fed along the grid angle $\omega t$, to the $U_{abc_{ref}}$ generation block. This block generates the reference modulation signals in $abc$ frame. The unit delay is used to compensate the delay during the control system

sampling and processing [10]. After that the PWM generator takes the three phase modulating signals as input and produces gating signals for the switching of the semiconductor devices in each arm of the MMC. Each block in Figure 3.26 is further explained briefly along with is simulation model consequently.

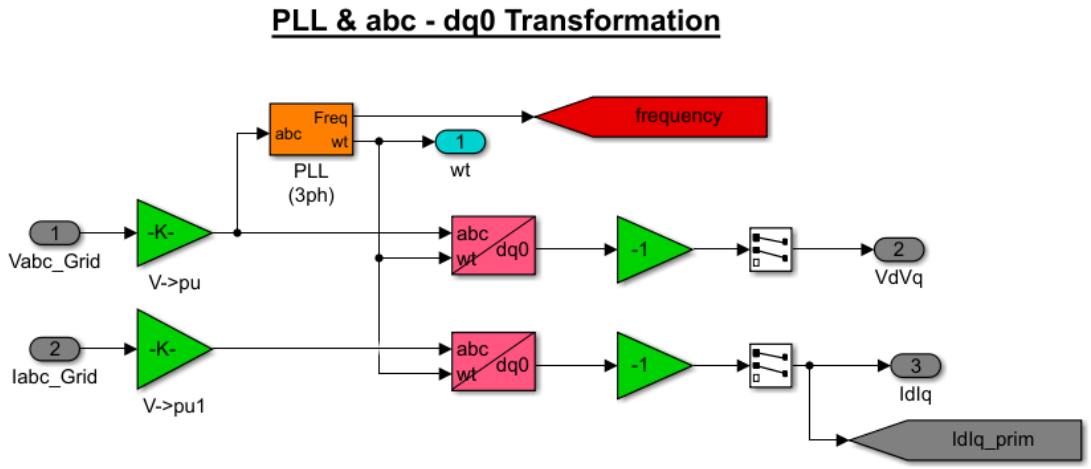



FIGURE 3.28: Simulation model for PLL and dq0 transformation

Figure 3.28 shows PLL and Measurements block which represents the model designed for the dq transformation of converter three phase output currents and grid three phase output voltages. Tracking of grid angle is done with using three-phase PLL block which is given to dq0 transformation blocks to synchronize the dq frame. This synchronization helps the transformation of three phase currents and voltages to dq frame constant vectors. The output of this PLL and Measurement block are grid angle $\omega t$, dq frame grid voltage and currents $v_d$ and $v_q$ and $I_d$ and $I_q$ respectively. The three phase AC signals are normalized before these signals are fed into the transformation block [10]. These normalized values are fed to dq0 transformation blocks along with the grid tracking angle tracked by phase locked loop which ensures the alignment of dq reference frame with grid voltage phasor. The parameters of PLL block and dq0 transform used in Simulink environment are given in Table 3.9.

After the transformation of pure DC signals in dq0 reference frame, these signals are provided to the current control inner loop where the active and reactive power

TABLE 3.9: Control parameters for PLL and dq0 transformation [10, 47]

| Description | Symbol | Value |
|---|---|---|
| Sampling time | $T_s$ | $6.06e^{-5}$ s |
| Sampling Frequency | $f_s$ | 3300 Hz |
| Minimum Frequency | $f_0$ | 50 Hz |
| Proportional Gain | $K_p$ | 180 |
| Differential Gain | $K_d$ | 1 |
| Integral Gain | $K_i$ | 3200 |
| Nominal Base Power | $P_{nom}$ | 1 MVA |
| Nominal Primary voltage | $V_{nomprim}$ | 220 kV |
| Nominal Secondary voltage | $V_{nomsec}$ | 52.05 kV |

are independently controlled by their respective active and reactive current components. The structure of inner control loop developed for the separate control of active and reactive current on the basis of dq0 model of three phase VSC system [61, 62] is shown in Figure 3.29. It constitutes two PI controllers for d-axis current and q-axis current.

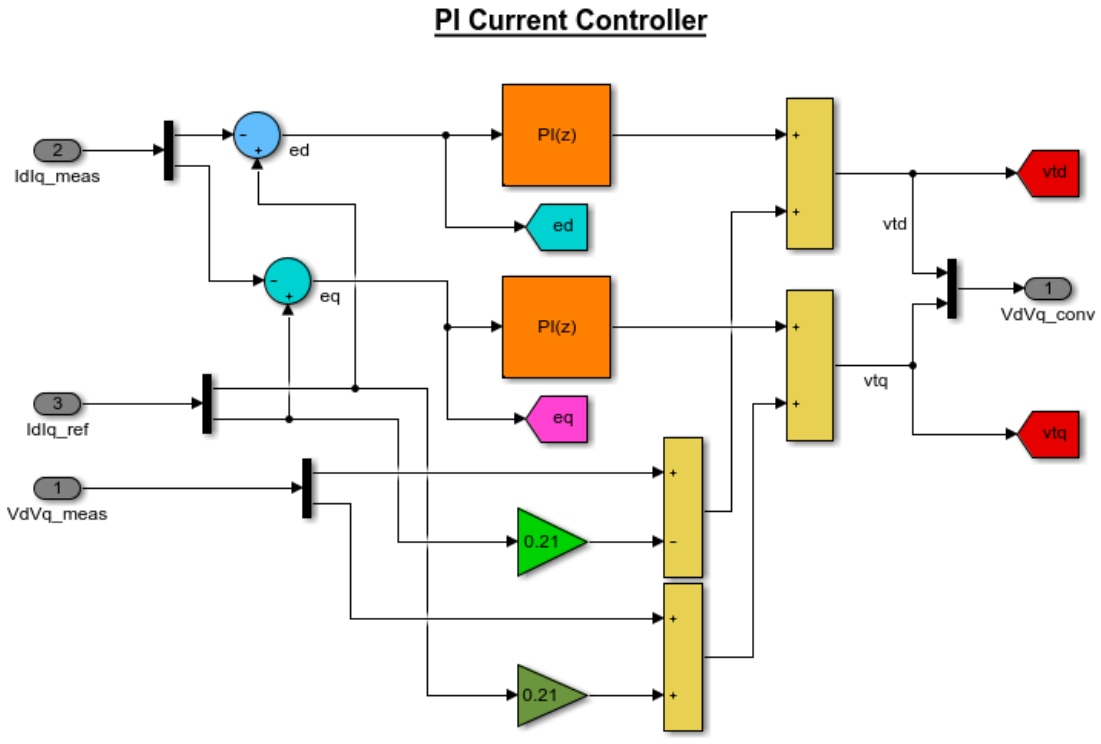



FIGURE 3.29: Current controller inner loop of MMC in dq Frame of reference

The three phase reference modulation signals are later used by PWM block to generate gating pulses for the control SCSM based 09-level grid tied MMC. Figure

3.29 represents the simulation model of the transformation of dq frame modulation signals to three phase modulation signals whereas Figure 3.30 shows the generated signal.

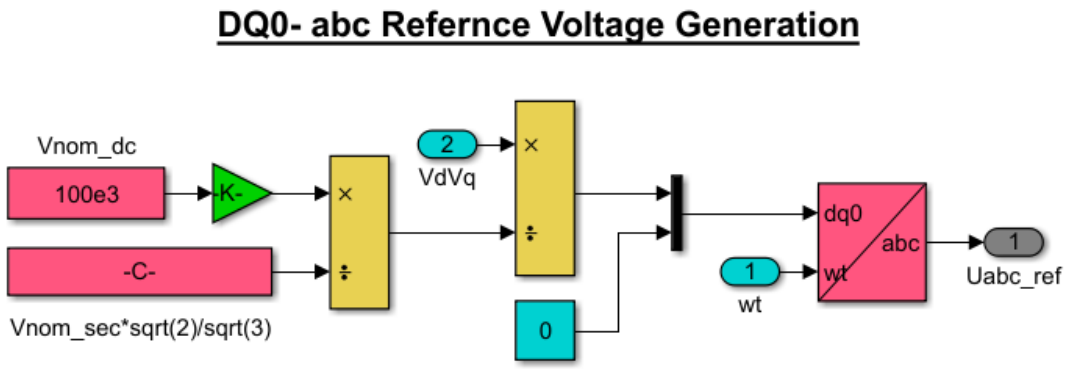



FIGURE 3.30: dq0 - abc reference Transform for modulation signals generation

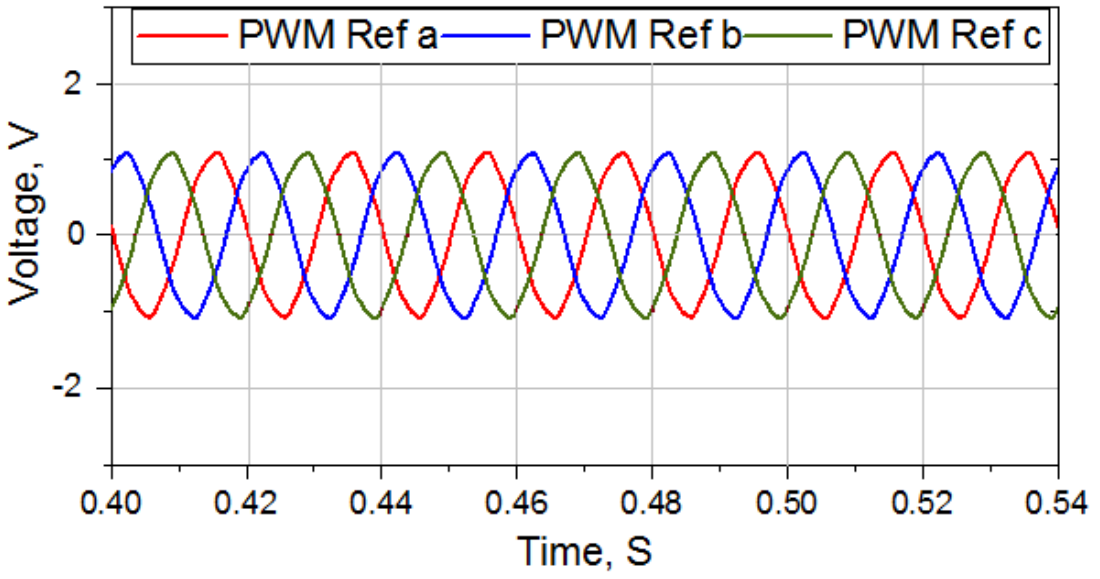



FIGURE 3.31: dq0 - abc for Modulating signals for 09-level MMC

The three phase reference modulation signals $m_{abc}(t)$, having fundamental frequency 50 Hz and amplitude varying between 1 and -1, are compared to the carrier waves, with frequency 1650 Hz and amplitude swinging between 1 and -1, by the PWM generator which is shown in Figure 3.31. As a result switching pulses are generated for the control of each IGBT in each half-bridge sub-module, two of these pulses are merged together for switching of single SCSM afterwards. The

TABLE 3.10: Parameters for PWM generation for 09-level [10]

| **Description** | **Symbol** | **Value** |
|---|---|---|
| Sampling time | $T_s$ | $6.06e^{-5}$ s |
| Number of carriers | $N$ | 8 |
| Carrier Frequency | $f_c$ | 1650 Hz |
| Modulation Frequency | $f$ | 50 Hz |
| Amplitude Modulation Index | $\hat{m}$ | 0.85 |
| Frequency Modulation Index | $m_f$ | 33 |
| Phase displacement per carrier | $\phi$ | $45^o$ |
| Total switching signals per phase | $N_s$ | 16 |
| Total SCSM signals in 3 phase | $N_{smt}$ | 144 |

switching signals for 09-level MMC are generated by using PWM generator (multilevel) block from Simscape Simpower library. Parameters of PWM generation for 09-level MMC is given in Table 3.10.

The modular multilevel converter uses series connected Switched-Capacitor Sub-Modules where each sub-module requires two PWM signals. As the single arm of the 09-level MMC comprises four series connected SCSMs therefore the model generates eight switching pulses for each arm in a three phase MMC. The eight switching signals for one arm are inverted to be used for the switching of other arm in the same converter phase leg. These signals are fed to the designed logic converter which convert them to the required six signals need for the switching of SCSM. Matlab/Simulink block uses three PWM generator blocks for three phase 09-level modular multilevel converter. The PWM block and $2^2$ logic switching signal of first SCSM are shown in Figure 3.32 and Figure 3.33 respectively.

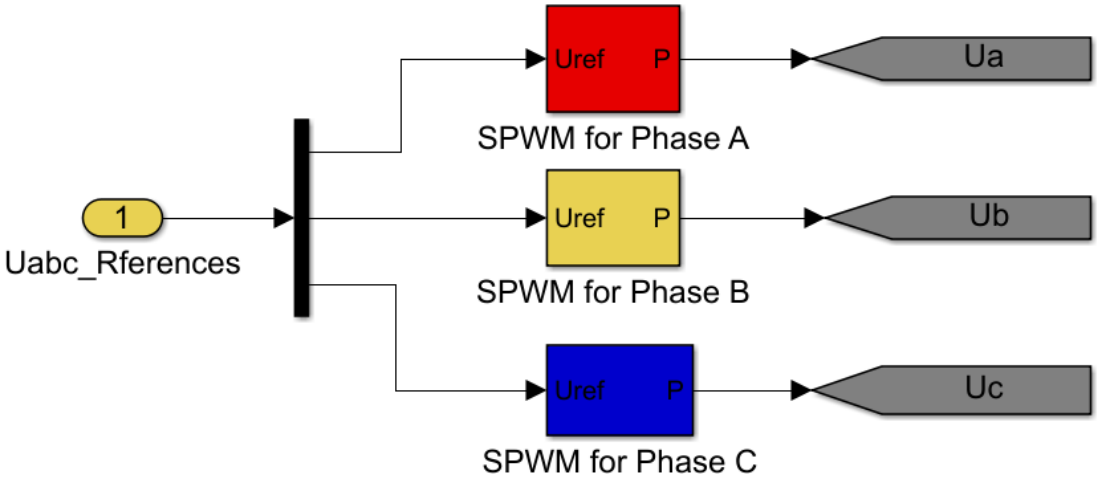



FIGURE 3.32: PWM generation for three phase MMC

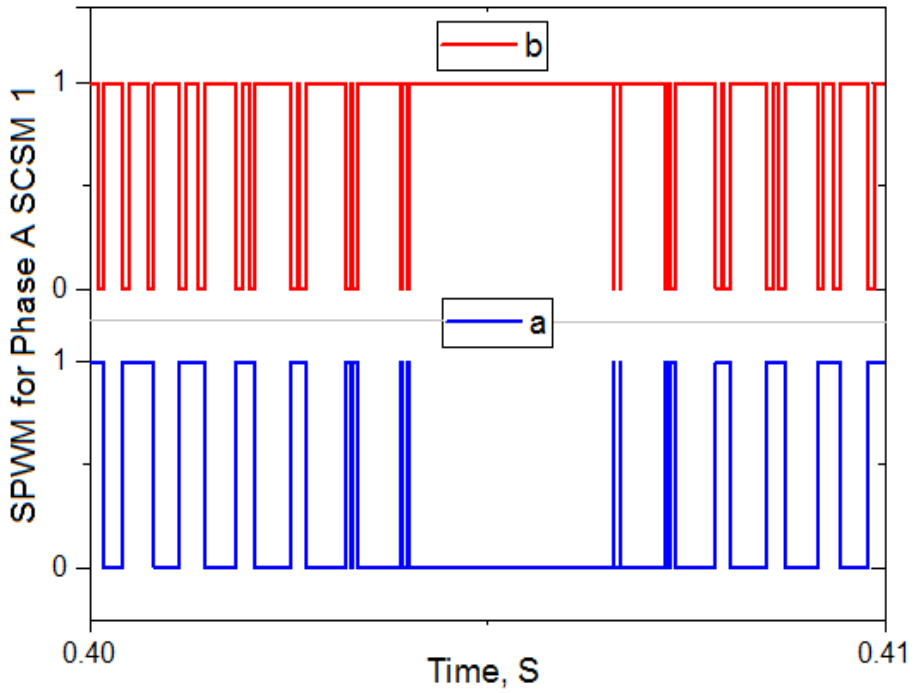



FIGURE 3.33: PWM signals for Phase A (SMua1)

## 3.9 Chapter Summary

This chapter discusses the comprehensive operational details of Switched- Capacitor Sub-Module (SCSM) as suitable for 09-level MMC with DC fault blocking capability. Working principle of Half-bridge based MMC is also discussed so that

its control can be interfaced with SCSM based power stage using a PWM converter for SCSM . Generation of Gate-pulse for SCSM has been explained using all required logical truth tables. Later the models discussed in earlier sections in this chapter, are presented towards by simulation models developed in Matlab/Simulink 2018a for each SCSM converter topology.

# Chapter 4

# Simulation Model & Results

## 4.1 Introduction

This chapter involves the discussion of the results evaluated by the simulation trial of the designed architecture as discussed in previous chapters. The results are produced using Matlab/Simulink 2018a environment where a case study is developed to test the normal as well as faulty cases of the SCSM based power stage interface with 09- level MMC using logic gate converter. Moreover to verify the lacking capability of half-bridge based MMC controller towards the DC side fault blocking, an initial trial is also simulated and presented which has used the conventional half-bridge based power stage with the 09-level MMC controller. Results are produced and presented regarding the related parameters for all cases.

## 4.2 Model Description

For the investigation of conventional HBSM based and SCSM architecture based 09-level MMC, a model case is developed by using the HVDC converter station operating in inverter mode of operation. To make study more practical and realistic, a 220 kV, 50 Hz AC grid is also interfaced with the converter through a phase reactor and a coupling transformer. DC link of voltage Vdc of 100 kV equally

divided to $V_{dc}/2$ of 50 kV are used to provide a DC bus as an input of the converter. The Phase reactor $R + jL = 0.04\Omega + 0.129H$ is used to allow the interface for the converter and the transformer. Moreover it also minimizes the harmonics from the converter output voltage and current waveforms [77]. The coupling transformer with Wye grounded Delta ($Y_g\Delta$) configuration is used between phase reactor and point of common coupling (PCC) as an interface between converter and grid terminal to provide suitable voltage levels for the converter [78]. The primary side voltage $V_{nompri}$ 220 kV (Grid) is stepped down by the transformer secondary voltage $V_{nomsec}$ equals to 52 kV (converter) [1].

The AC grid is designed by using a symmetrical three phase voltage source with 220 kV (r.m.s) voltage and 50 Hz nominal frequency. Initially the power circulating in grid is 100 MW when the converter is in standalone mode. Two loads with equal power rating of 50 MW are used in parallel connection with two transmission lines of 10 km distance in between and from grid. Both converter topologies i.e. HBSM based and SCSM based are used and tested through the developed approach.

A carrier wave with high frequency $f_{sw}$ of 1650 Hz is used for the switching of both converter topologies therefore the sampling frequency $f_s$ of $100 \times 1650$ Hz is chosen for the sampling of the entire system signals. The sampling time $T_{spower}$ is therefore chosen to be $6.06e^{-6}$ s for the sampling of power signals while $T_{scontrol} = 6.06e^{-5}$ s is chosen for the sampling of control signals.

The bus C1 represents the converter station output bus where converter output voltages and currents are measured, bus C2 represents the Grid terminal i.e. point of common coupling (PCC) which is link between grid and converter. Bus C3 represents the grid side bus where grid voltages and currents are measured. The single line diagram of the described case is presented in Figure 4.1. The simulation parameters of the entire system for Matlab/Simulink are summarized in Table 4.1.

TABLE 4.1: Overall simulation parameters for Matlab/Simulink model [10, 23, 76]

| Description | Symbol | Value |
|---|---|---|
| DC Voltage Bus | $V_{dc}$ | 100 kV |
| Line Reactance | $R + jL$ | $0.04\ \Omega + 0.129H$ |
| Arm Inductance | $L_{arm}$ | 3 mH |
| Arm Resistance | $R_{arm}$ | 1 Ω |
| AC Grid Voltage | $V_s$ | 220 kV (r.m.s) |
| Grid Frequency | $f$ | 50 Hz |
| Total AC Load | $2 \times L$ | $2 \times 50$ MW |
| Transmission Lines | $2 \times \pi$ | $2 \times 10$ MW |
| SCSM Capacitor | $C$ | 6 mF |
| Number of SCSM per arm | $(N-1)/2$ | 04 |
| Total number of SCSM | $(N-1)*3$ | 24 |
| Output peak voltage | $V_t$ | 50 kV |
| Voltage across SCSM capacitor | $E$ | 6.25 kV |
| Number of HBSM per arm | $N-1$ | 08 |
| Total number of HBSM | $2(N-1)*3$ | 48 |
| Transformer nominal voltages | $V_{nomsec} : V_{nomprim}$ | 52 kV:220 kV |
| Converter Switching Frequency | $f_{sw}$ | 1650 Hz |
| Sampling time for power GUI | $T_{spower}$ | $6.06e^{-6}$ s |

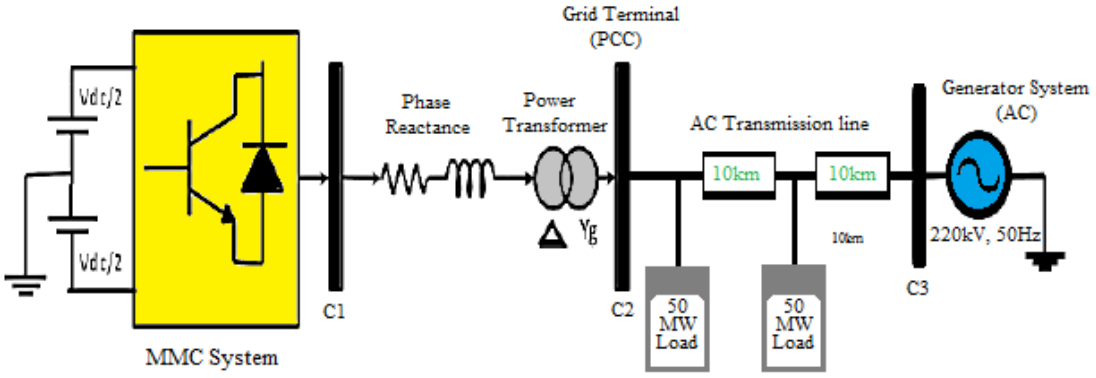



FIGURE 4.1: Single line diagram of the developed model

## 4.3 Simulation Model in Matlab/Simulink 2018a Environment

On the basis of the modeling and study being done in the previous chapter, a simulation model has been developed for 220 kV Grid tied three-phase 9-level

MMC using HBSM and later SCSM as a MMC cell with designed logic converter and conventional cascaded half bridge SPWM controller in Matlab/Simulink 2018a environment using Simscape Simpower library.

Measurement of all grid voltages and currents is made. Required synchronization with grid has been achieved by feeding all grid voltages to phased locked loop (PLL). After this abc-to-dq transformation is used to get direct and quadrature components for grid voltages and currents. Proportional-integral (PI) based current controller is fed with the real values of direct and quadrature currents. The direct and quadrature components of the inverter voltages are then created using the produced output from the current controllers. Then these components are used by employing dq-to-abc transformation again to get the three-phase reference voltages.

For 09-level converter four SCSM are used per arm as single SCSM gives output double of the HBSM and total twenty-four modules are used as compared to the forty-eight sub modules when half bridge sub module configuration is used. Initially, conventional system based on cascaded HBSM is simulated to justify the use of proposed architecture. Afterwards two simulation modes normal and faulty using SCSM based power stage along with the designed architecture are simulated.

The Power GUI is used with sampling time $Ts = 6.06e^{-6}$ s for the both of the entire Simulink models. The simulation run time for both of the models is $t_{run} = 1.2$ s. Figure 4.2 represents the corresponding Simulink model for 09-level MMC with inner current control, scope section and fault generation block. The converter control block presents the inner current control implemented by using PI compensator in *dq* reference frame as discussed in chapter 3, whereas scope section block is used to analyze and record the behavior of model parameters during the entire simulation period. The fault generation block comprises of a switch which provides a pole-to-pole short circuit at DC bus as and when required by using a pulse generator.

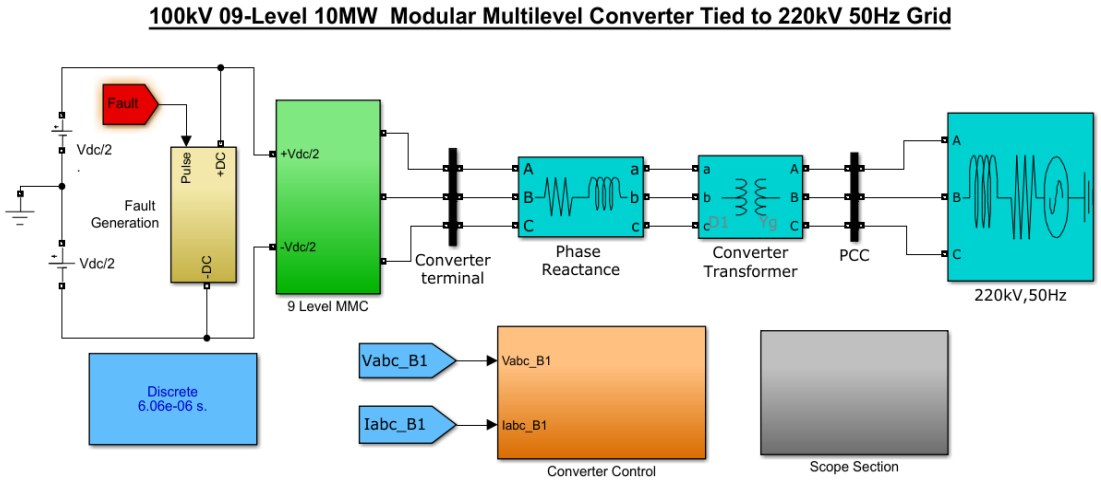



FIGURE 4.2: Simulink model of 09- Level MMC with control, scope and fault generation sub systems

## 4.4 Cascaded Half-bridge based conventional Converter

In order to further verify the need of Switched-Capacitor Sub-Module for DC fault blocking capability, initially simulation model of MMC is operated with power stage based on cascaded half bridge sub modules using eight sub-modules per arm and total of forty-eight sub modules. Following sub sections demonstrate the normal and abnormal modes of HBSM based MMC simulation results which shows the lacking capability of DC fault blocking and hence raise the requirement of such topology which can handle DC side faults.

### 4.4.1 HBSM Converter power tracking and Grid power

Reference active power of 10 MW is injected into the AC grid however the reference reactive power is zero MVAR. 10 MW power injection reduces the grid power burden to 90 MW. Converter power is tracking the reference power smoothly and grid power remains to 90 MW from $t = 0.1$ s to $t = 0.4$ s. At $t = 0.4$ s a point-to-point fault has been introduced and removed at $t = 0.45$ s. After the detection

of DC side fault, all PWMs are turned off but the converter allowed the reverse power from AC grid to flow towards the DC side fault which makes the grid power flow unstable despite the fact that reference power is set to zero. This is due to the freewheeling diodes of IGBTs for reverse voltage protection which are essential to avoid any negative voltage across the switch. Corresponding simulation results of tracking power of MMC and AC grid power during normal and fault period is shown in Figure 4.3 and Figure 4.4 respectively.

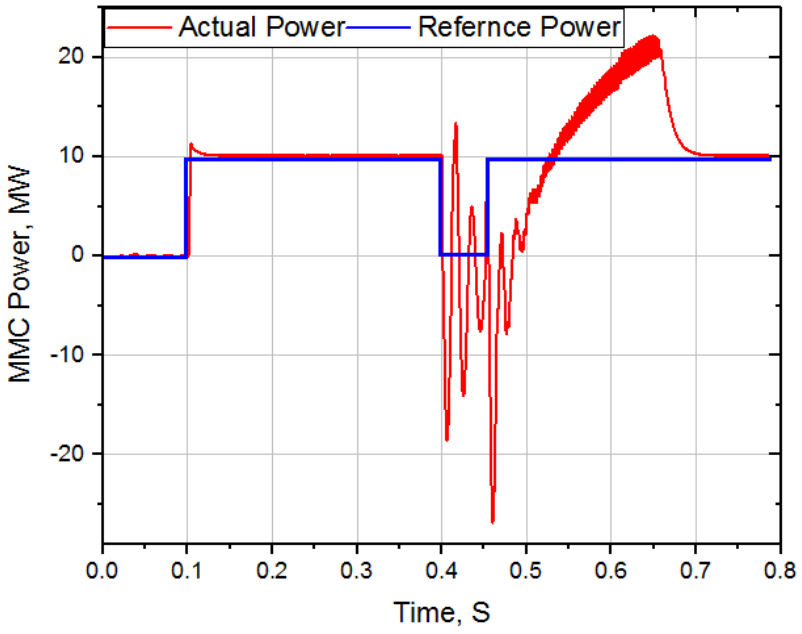



FIGURE 4.3: HBSM MMC power tracking during normal and fault period

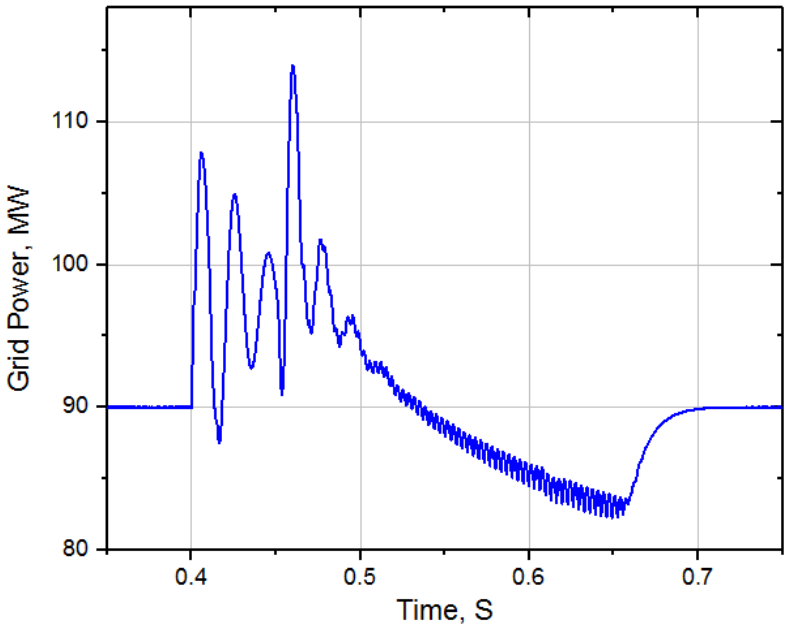



FIGURE 4.4: AC Grid power during normal and fault period

### 4.4.2 HBSM Converter terminal voltage and current

Voltages and currents are measured at converter terminal. Normal voltage of 50 kV peak is observed during the normal period with a stable rated current of approximately 110 A peak which remains stable from $t = 0.1$ s to $t = 0.4$ s. When fault is generated at $t = 0.4$ s, The converter terminal voltages becomes almost zero while highly unstable current is observed during the fault period due to the AC grid current contribution towards the fault. This condition remains for the fault period till $t = 0.45$ s but even after the fault is removed, notable unstable transients in current waveform are occurred. Converter terminal voltage has also gained the stability after $t = 0.65$ s which is 0.2 seconds later then the fault has been cleared. Waveform of converter terminal voltage and current during the normal as well as fault period is shown in Figure 4.5 and Figure 4.6 respectively.

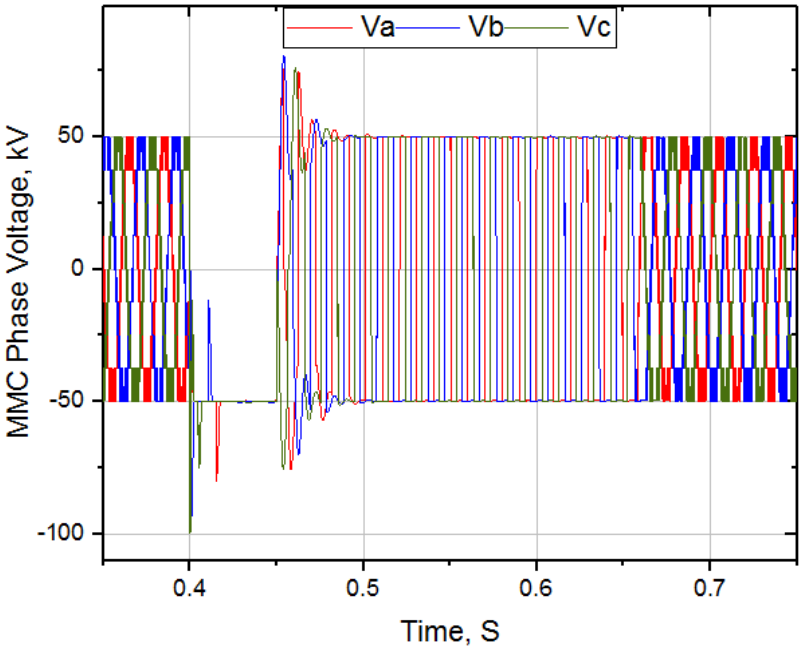



FIGURE 4.5: HBSM MMC terminal voltage during normal and fault period

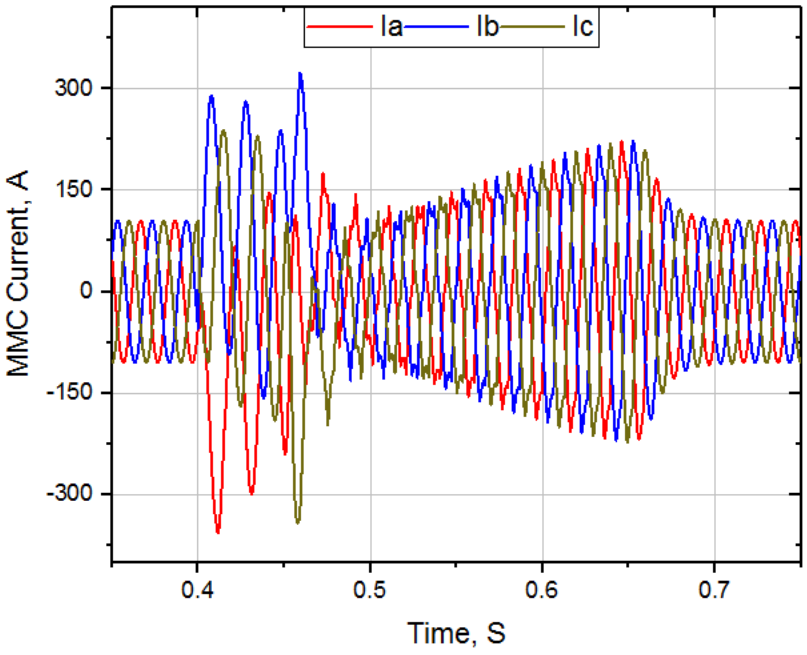



FIGURE 4.6: HBSM MMC terminal current during normal and fault period

### 4.4.3 Grid terminal (PCC) voltage and current

Voltages and currents are measured at grid terminal i.e. point of common coupling (PCC). Normal voltage of 220 kV peak to peak that is synchronized with the

grid voltage is observed during the normal period with a stable rated current of approximately 25 A peak which remains stable from $t = 0.1$ s to $t = 0.4$ s. Voltage is stepped up by the transformer while the current is stepped down to keep the power constant. When fault is generated at $t = 0.4$ s, The converter voltages at grid terminal (PCC) remains stable due to the fact that grid is bearing and compensating all the fault current and transients so the voltage at infinite bus remains stable. However unstable current is observed during the fault period due to the AC grid current contribution towards the fault. This condition remains for the fault period till $t = 0.45$ s, but the unstable transients remained in current waveform and lasts for 0.06 seconds after the fault has been removed. Waveform of converter terminal voltage (magnified) and current during the normal as well as fault period is shown in Figure 4.7 and Figure 4.8 respectively.

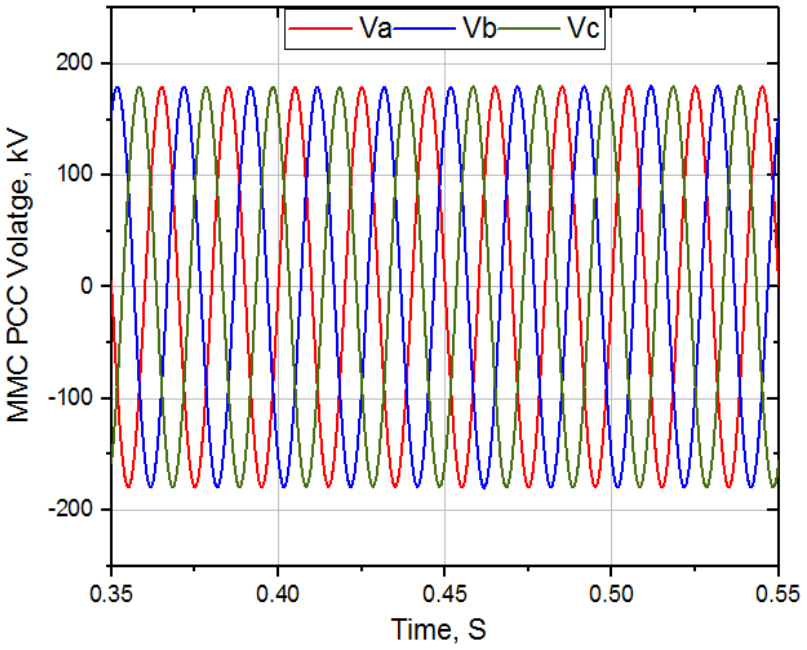



FIGURE 4.7: HBSM MMC voltage at grid terminal (PCC) during normal and fault period

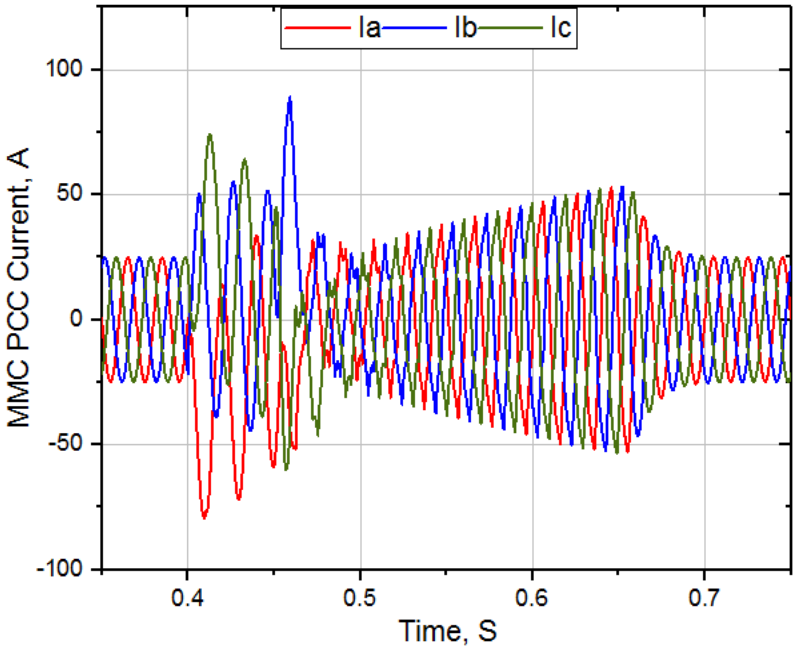



FIGURE 4.8: HBSM MMC current at grid terminal (PCC) during normal and fault period

### 4.4.4 HBSM Converter DC current

DC current is also measured using a series measurement block and respective wave forms are recorded using scope. During the normal period from $t = 0.1$ s to $t = 0.4$ s, smooth DC current of value approximately 75 A (dc) is noted. When at $t = 0.4$ s DC side fault is initiated, negative peak of DC fault current of approximately -50 kA is observed even though the converter is switched off. This negative DC fault current is due to the AC side contribution towards fault via freewheeling diodes of half bridge sub modules. At $t = 0.45$ s, when the DC fault is cleared a similar peak but in opposite polarity is observed due to the transient instability of converter. Figure 4.9 shows the DC current waveform during the normal and fault period. Magnified waveform is also presented to analyze the exact DC current during the normal mode.

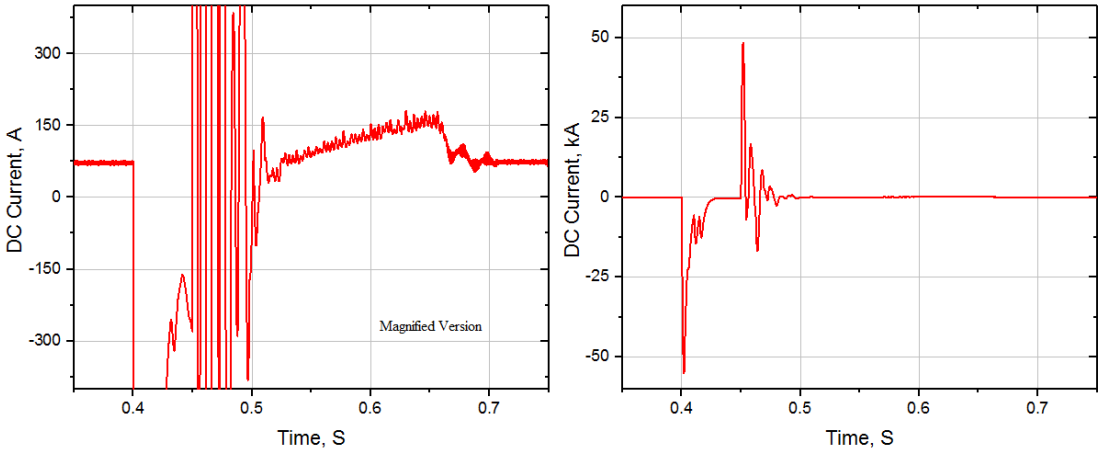



FIGURE 4.9: HBSM MMC DC current during normal and fault period

## 4.5 SCSM based MMC normal operational mode

Conventional Grid tied MMC controller which is previously used with half-bridge based power stage is now interfaced with switched-capacitor sub-module (SCSM) based power stage using the designed logic converter. All the tests of logic converter are verified in previous chapter, that is why only the simulation results of MMC are presented at this time. Power stage is composed of twenty-four SCSM cells where one arm consist of four SCSM cell. Each SCSM cell requires two merged PWM inputs from the controller side which are converted into six required pulses by the logic converter for the desired operation. Following sub-sections demonstrates the simulation results during the normal operational mode of SCSM based MMC using the designed architecture.

### 4.5.1 SCSM Converter power tracking

To verify the full controllability of SCSM based architecture, initially a step reference of active power of 8 MW at $t = 0.23$ s is given to the converter. The step reference was tracked by the converter efficiently. After $t = 0.3$ s reference power is stepped down to 5 MW which has been also tracked by the converter. Finally at $t = 0.38$ s a reference power of 10 MW is injected into the Grid having 100 MW

total load. Corresponding simulation results are shown in Figure 4.10. Reference reactive power is zero MVAR. This result shows the delivering output power of MMC which is tracking the different referenced active powers perfectly.

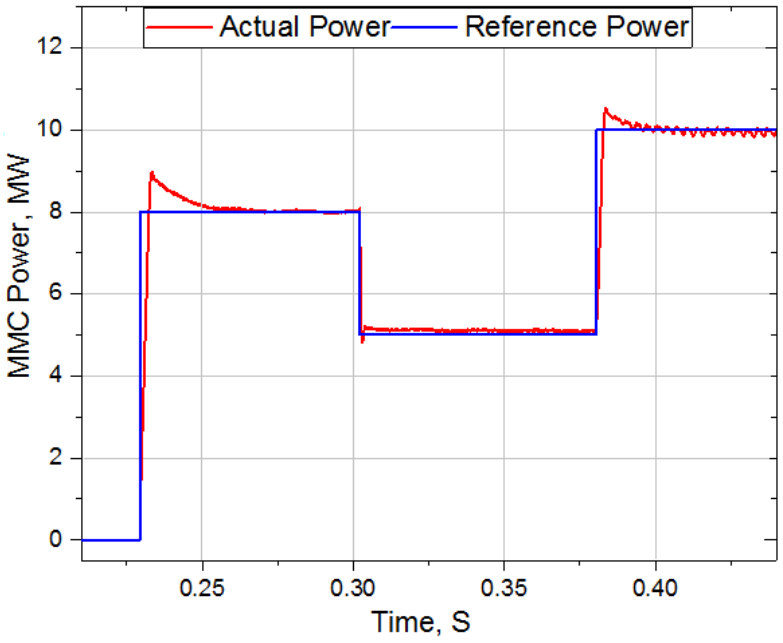



FIGURE 4.10: SCSM MMC power tracking during normal period

### 4.5.2 SCSM Converter terminal parameters

Voltages and currents are measured at converter terminal. Normal voltage of 50 kV peak is observed during the normal period with a stable rated current of approximately 110 A peak. Results presented for period $t = 0.4$ s to $t = 0.44$ s shows the satisfactory expected output of MMC with using the designed architecture. SCSM based MMC terminal voltage and current during normal mode is presented in Figure 4.11 and Figure 4.12 respectively where nine voltage levels can be observed in terminal voltage waveform.

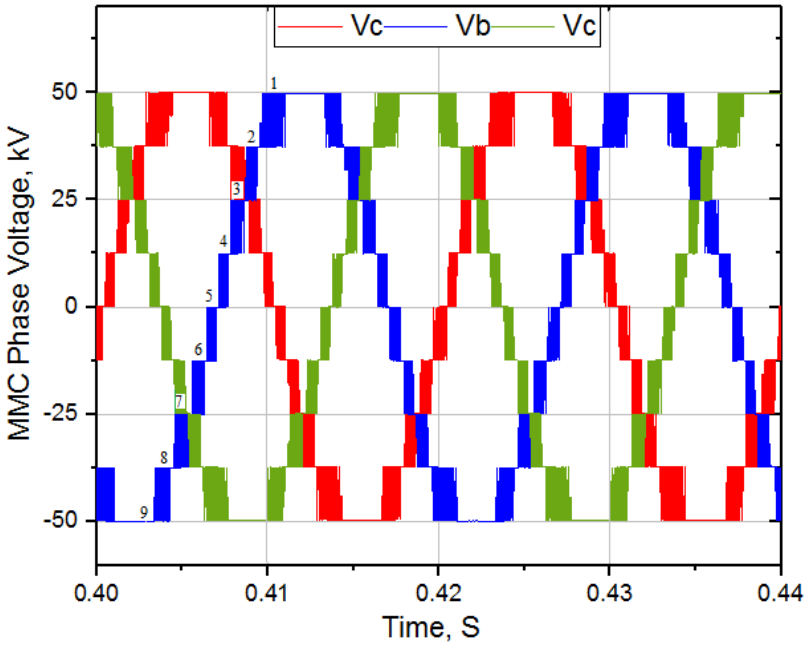



FIGURE 4.11: SCSM MMC terminal voltage during normal period

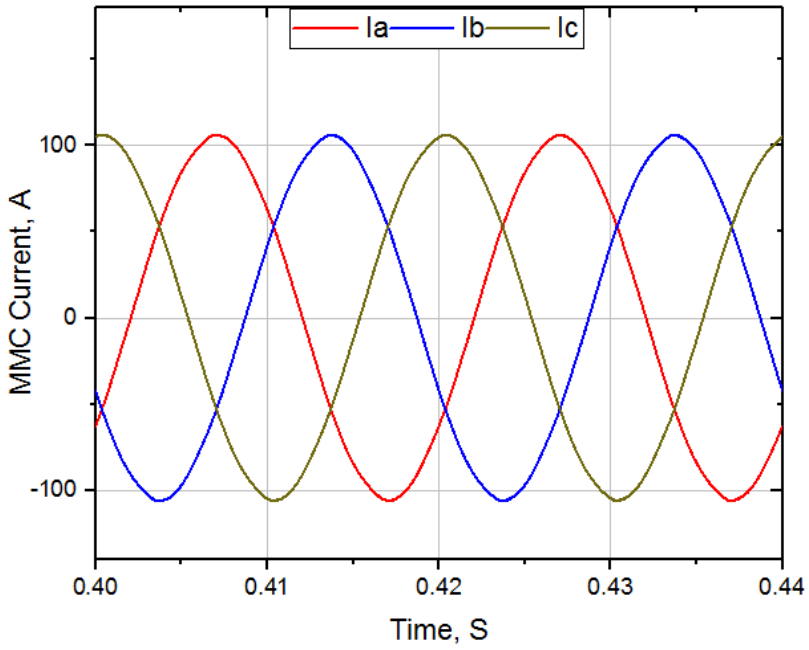



FIGURE 4.12: SCSM MMC terminal current during normal period

After the verification of power tracking, 10 MW rated power is injected into the grid from $t = 0.38$ s onwards. This power is correspondingly measured at MMC terminal and results are presented accordingly. DC current is also measured using

a series measurement block and respective wave forms are recorded using Simulink scope.

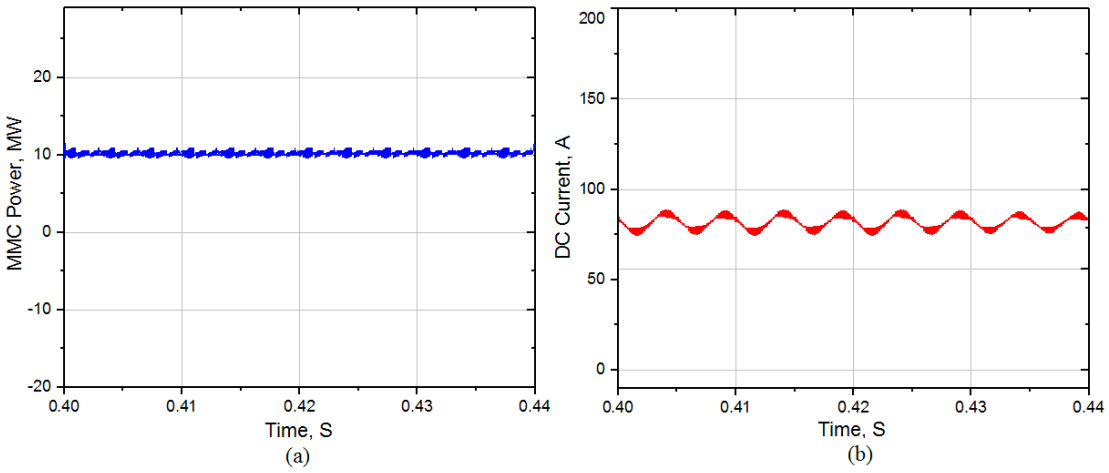



FIGURE 4.13: SCSM MMC terminal parameters during normal period: (a) Converter power and (b) DC input current

During the normal period of 10 MW power injection, stable DC current of value approximately 75 A (dc) is noted. SCSM based MMC terminal power and DC input current during normal mode is shown in Figure 4.13a and Figure 4.13b respectively.

### 4.5.3 Grid terminal (PCC) parameters

Voltages and currents are measured at grid terminal i.e. point of common coupling (PCC). Stable and sinusoidal voltage of 220 kV peak to peak, synchronized with the grid voltage is observed during the normal period with a stable rated current of approximately 25 A peak which remains stable during the normal period from $t = 0.4$ s onwards. MMC terminal voltage of 50 kV is stepped up to the grid voltage by the transformer when the PLL is synchronizing the grid voltages, whereas current is stepped down from 100 A to 25 A (peak) to keep the power constant. Waveform of converter stepped up voltage at PCC and current injected to the grid during the normal period is presented in Figure 4.14 and Figure 4.15 respectively.

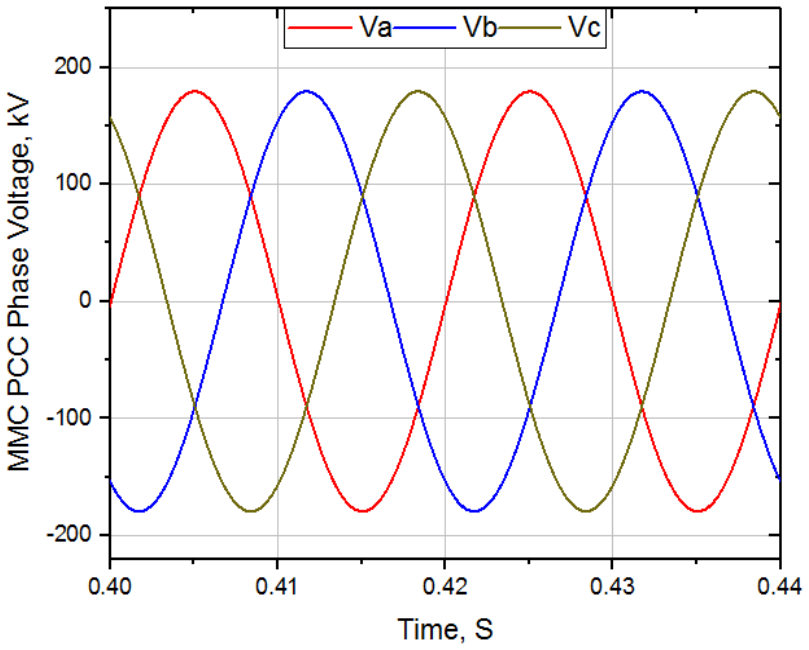



FIGURE 4.14: SCSM MMC voltage at grid terminal (PCC) during normal period

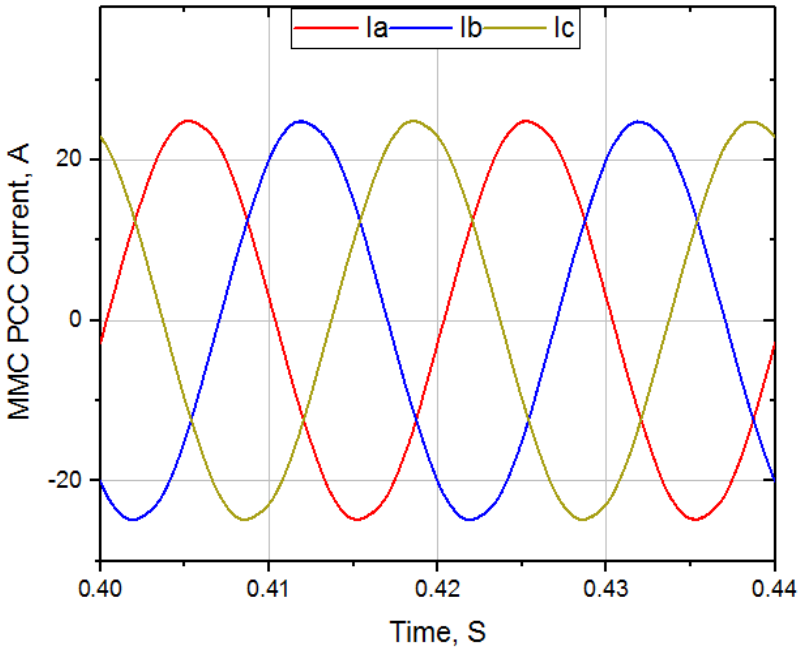



FIGURE 4.15: SCSM MMC current at grid terminal (PCC) during normal period

Grid power burden has reduced from 100 MW to 90 MW by the power injection of 10 MW from converter. Converter power is measured at grid terminal (PCC) using 3-phase power monitor in Simulink and is presented in Figure 4.16. Converter

power is tracking the reference power seamlessly as presented in the above sections so the grid power remains to 90 MW from $t = 0.4$ s onwards. Grid power is also measured at grid side terminal and is shown in Figure 4.17a. Moreover the PLL is keeping the MMC frequency synchronized with the grid frequency to 50 Hz which is presented in Figure 4.17b.

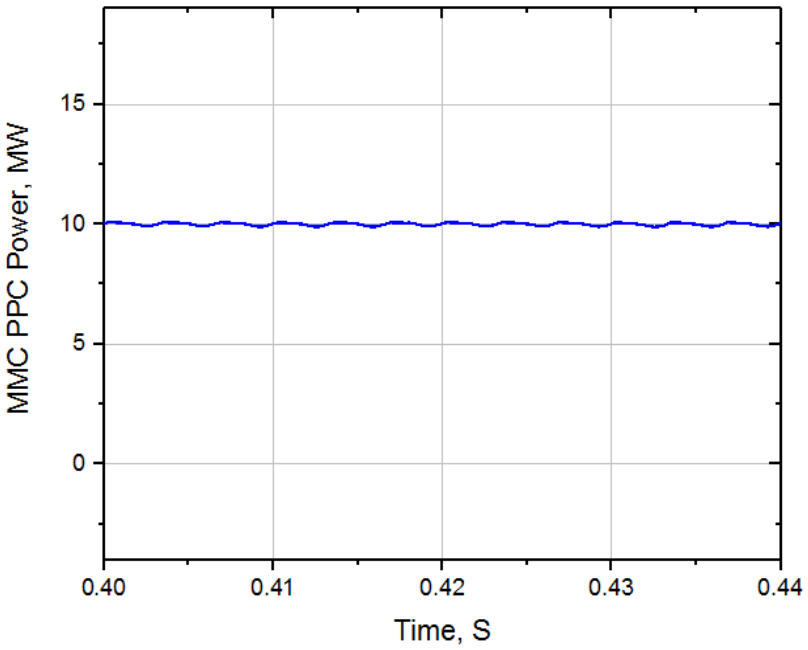



FIGURE 4.16: SCSM MMC power at grid terminal during (PCC) normal period

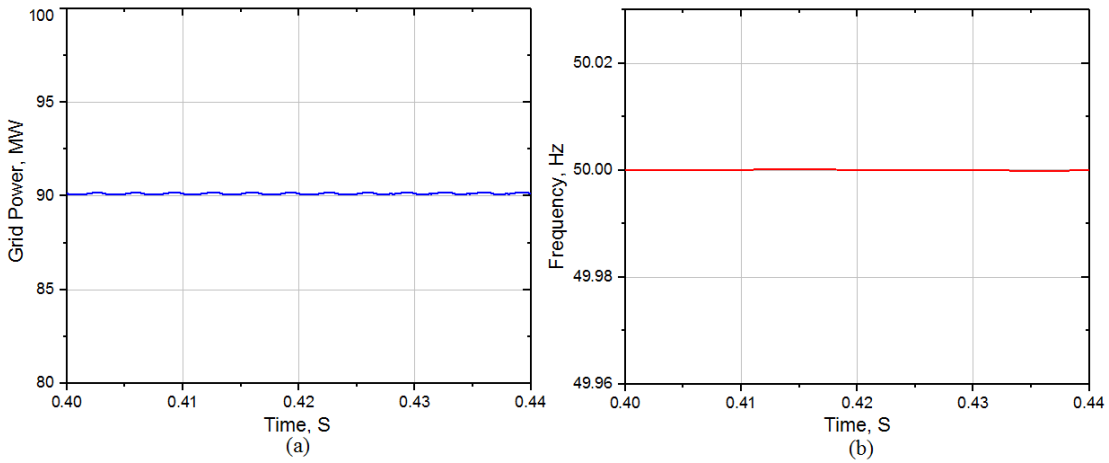



FIGURE 4.17: SCSM MMC Grid terminal parameters during normal period: (a) Grid Power and (b) Synchronized Grid frequency

### 4.5.4 PWM and Reference modulation signals

The three phase reference modulation signals, having fundamental frequency of 50 Hz and amplitude varying between 1 and -1, are compared to the carrier waves, with frequency 1650 Hz and amplitude swinging between 1 and -1, by the PWM generator. As a result switching pulses are generated for the control of each IGBT in each half-bridge sub-module, and two of these pulses are merged together for switching of single SCSM afterwards. Three phase reference signals and two PWM signals for the first SCSM of phase-A along with enable signal (magnified) during the normal period is demonstrated in Figure 4.18 and Figure 4.19 respectively.

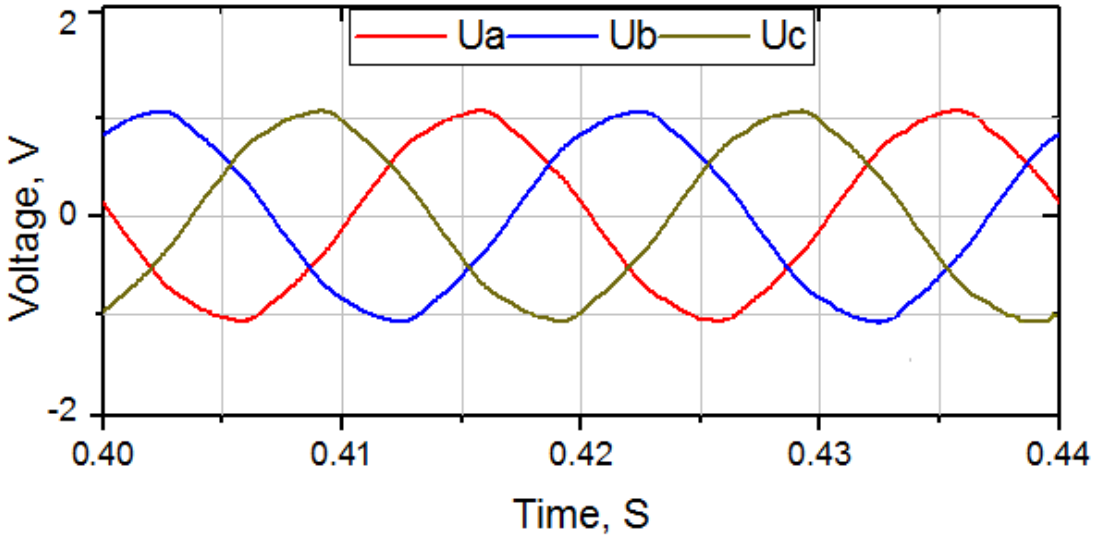



FIGURE 4.18: Three phase reference signal for PWM during normal period

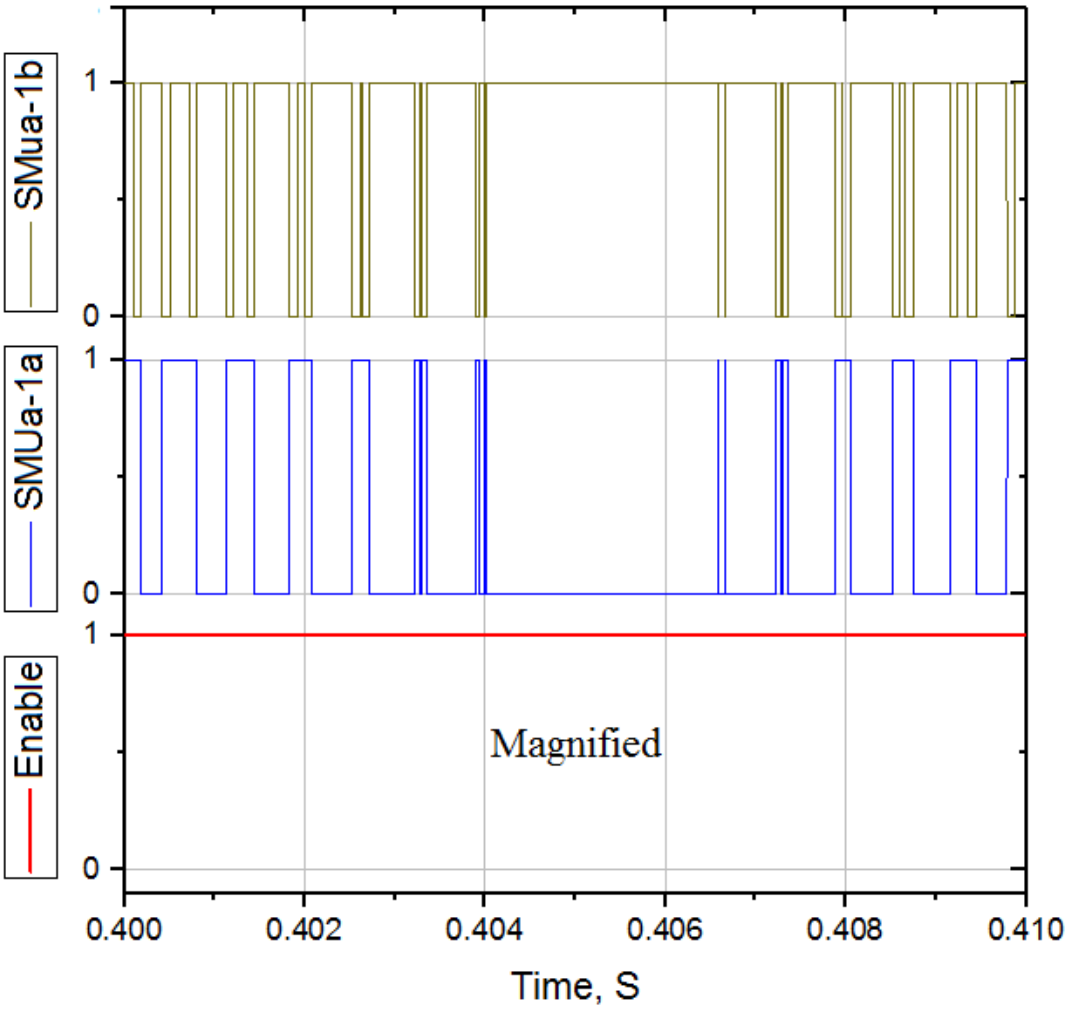



FIGURE 4.19: SCSM-1 (Phase-A) 2x PWM signals with Enable during normal period

## 4.6 SCSM based MMC DC Point-to-point fault

To demonstrate the DC blocking capability of the SCSM based MMC with the logic gate convertor, a point-to-point fault at DC bus has been introduced at $t = 0.8$ s and removed at $t = 0.85$ s using the fault generation block implemented in Simulink. After the detection of DC side short circuit fault all IGBTs are turned off using the enable input of logic converter and reference power is also set to zero to turn off the converter. Following sub-sections demonstrates operational mode of SCSM based MMC during the fault period.

### 4.6.1 SCSM Converter power tracking

Converter is tracking the reference power of 10 MW and this power track is measured at grid terminal (PCC). As soon as the fault is discovered (at $t = 0.8$ s) reference power is set to zero immediately and the converter power has followed the set referenced power instantly and remains zero during the fault period. As soon the fault is removed, power is restored by setting the reference power again to 10MW and the converter again starts tracking the reference power capably. Converter power track waveform recorded from $t = 0.76$ s to $t = 0.92$ s is demonstrated well by Figure 4.20.

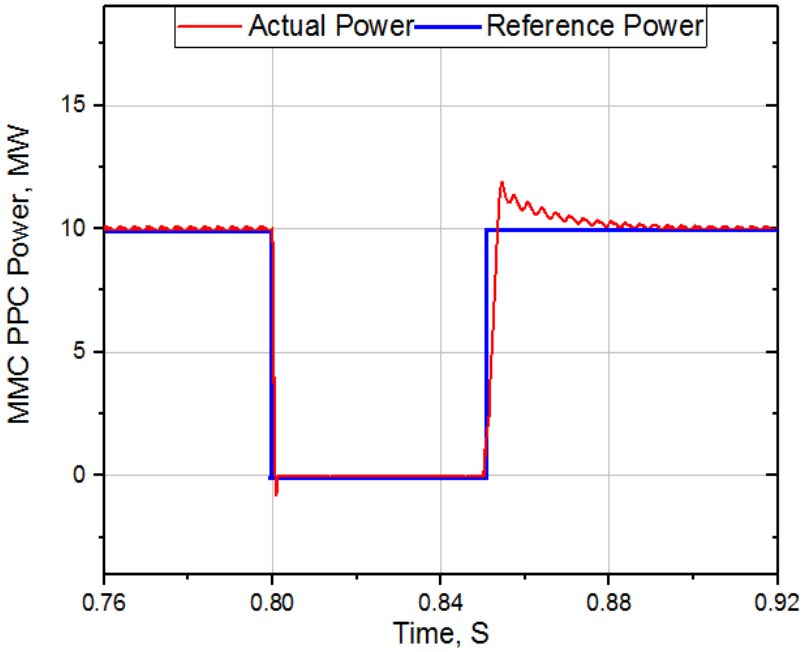



FIGURE 4.20: SCSM MMC power tracking during fault period

### 4.6.2 PWM and Reference modulation signals

After the detection of DC fault all IGBTs of SCSM need to be switched off. Enable signal is used to make all the PWMs to zero to turn off all the switches of sub module. Reference power is set to zero and current controller is generating zero control signal. PWM signal of first sub module of phase-A and reference signal during the fault period is shown in Figure 4.21 and Figure 4.22 respectively.

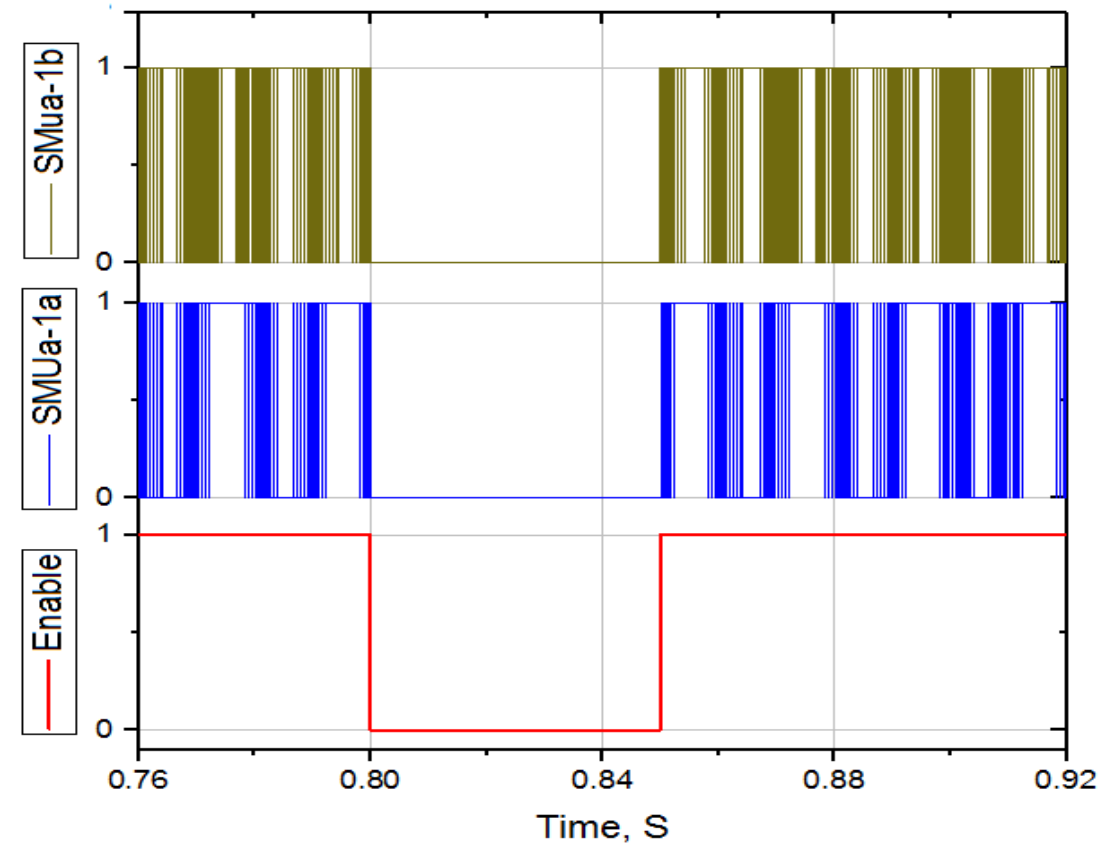



FIGURE 4.21: SCSM-1 (Phase-A) 2x PWM signals with Enable during fault period

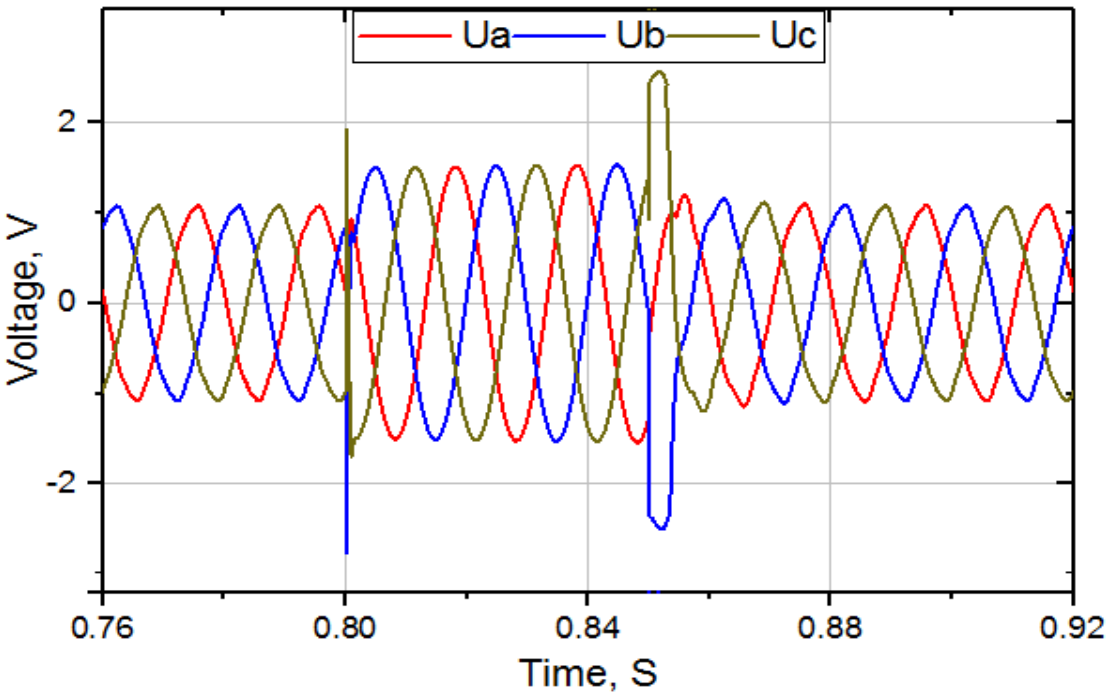



FIGURE 4.22: Three phase reference signal for PWM during fault period

### 4.6.3 SCSM Converter terminal parameters

Voltages and currents measured at converter terminal are also analyzed for DC fault period. Normal voltage of 50 kV peak with a stable rated current of approximately 110 A peak is noted before the fault period. After the detection of fault, converter is turned off so all the three phase currents comes to be zero and no current is observed from either side i.e. grid or converter side. As the converter is switched off, so grid voltage with down scaled and negative offset is noted at converter terminal. As soon as the fault is removed voltages and currents are restored again to the set values instantly without any transient instability. SCSM based MMC terminal voltage and current during the fault mode is presented in Figure 4.23 and Figure 4.24 respectively where voltage and zero current can be observed in respective waveforms.

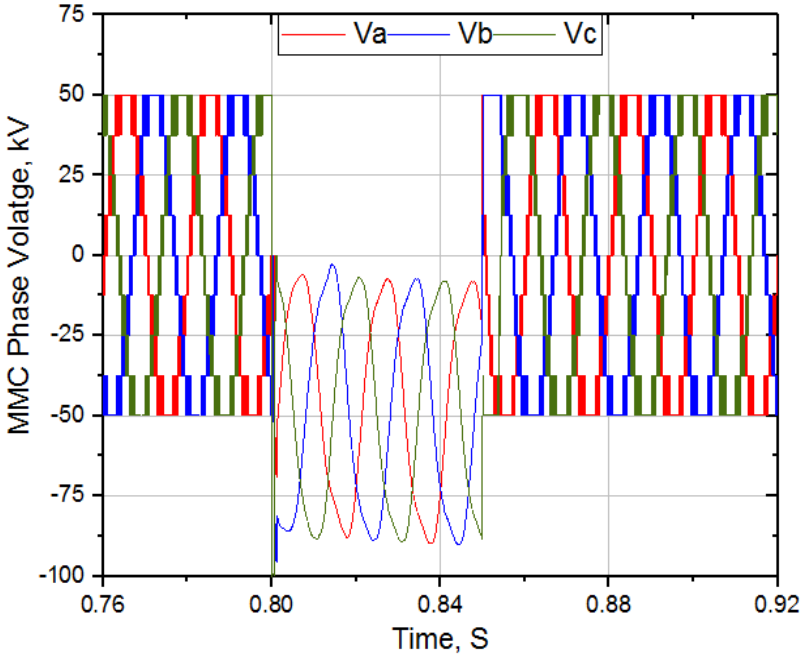



FIGURE 4.23: SCSM MMC terminal voltage during fault period

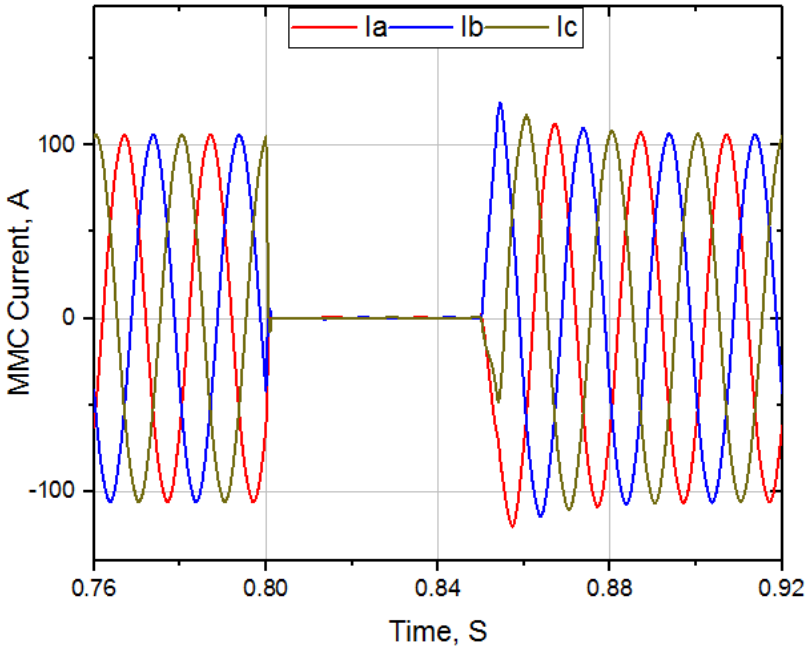



FIGURE 4.24: SCSM MMC terminal current during fault period

The power measured at MMC terminal remains under control and stable until the fault is introduced. When at $t = 0.8$ s fault is initiated, converter is switched off and the power delivered by the converter is set to zero and no power either positive or negative is noted in this mode during fault period. Power is restored again immediately as the fault is cleared. Figure 4.25a illustrates the converter terminal power during this mode.

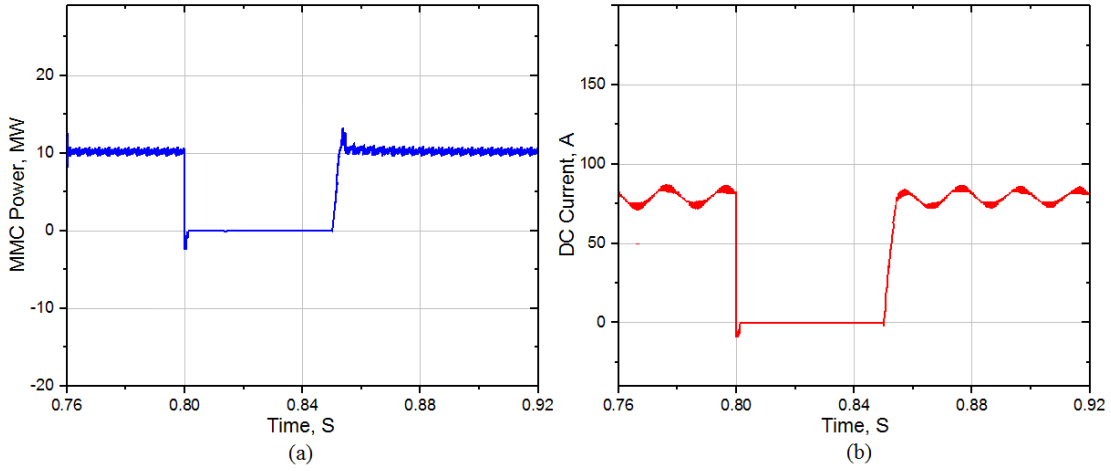



FIGURE 4.25: SCSM MMC terminal parameters during fault period: (a) Converter power and (b) DC input current

During the normal period of 10 MW power injection, stable DC current was noted which also remained stable until the fault period. When the fault is detected, DC current becomes zero instantly due to the immediate turnoff of the converter and zero DC fault current is observed. Results has witnessed the zero contribution of AC grid towards the DC fault as the designed architecture has successfully blocked the DC fault current. DC input current during fault mode is shown in Figure 4.25b.

### 4.6.4 Grid terminal (PCC) parameters

Voltage measured at grid terminal i.e. point of common coupling (PCC) is stable and sinusoidal voltage of 220 kV peak to peak which is synchronized with the grid voltage during the normal as well as fault period due to the infinite bus, with a stable rated current of approximately 25 A peak which remains stable during the normal period. When fault is initiated, current at grid terminal follows the converter terminal current and becomes zero immediately which shows the zero power flow via converter towards DC fault. Waveform of Grid terminal voltage at PCC and current at this point during the fault period is presented in Figure 4.26 and Figure 4.27 respectively.

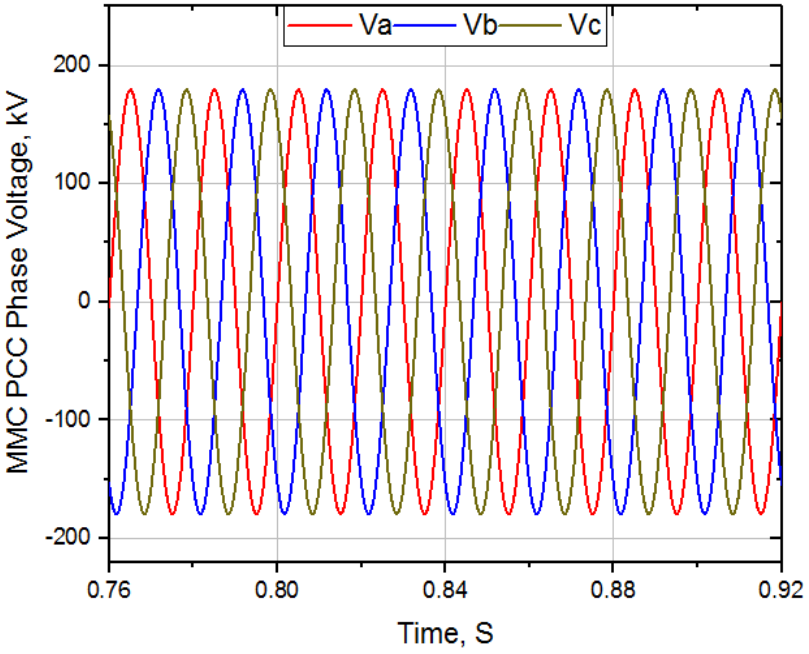



FIGURE 4.26: SCSM MMC voltage at grid terminal (PCC) during fault period

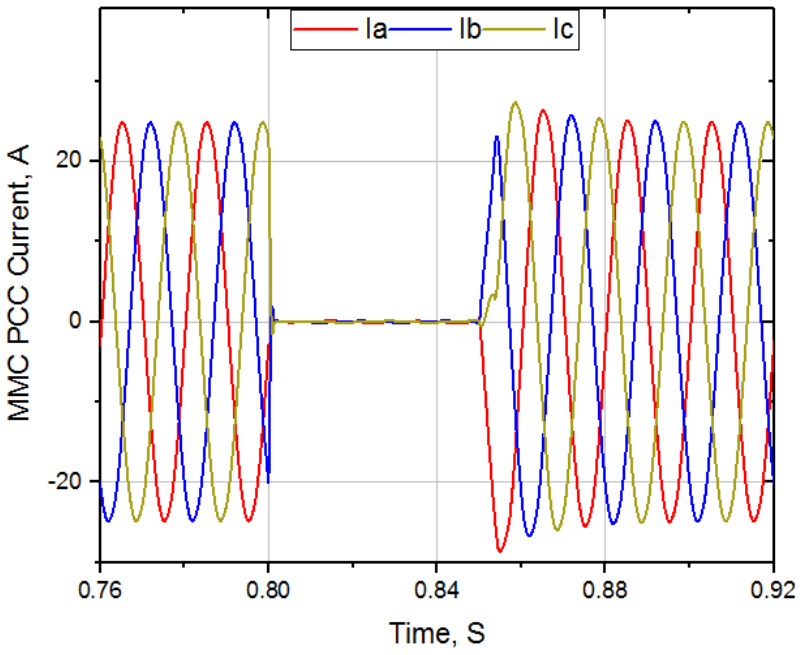



FIGURE 4.27: SCSM MMC current at grid terminal (PCC) during fault period

Grid power burden had reduced from 100 MW to 90 MW due to the power injection of 10MW by converter. As the fault is detected, converter has been turned off and stopped its power sharing because of the DC fault. The grid has taken the power burden of 10 MW immediately as shown in Figure 4.28a. It is clear that during the

fault condition, grid is only compensating that part of power which was previously injected by the converter to the grid and there is zero contribution of grid towards DC side fault. As the power sharing of converter is restored after the fault has been removed, grid power burden is again reduced to 90 MW.

PLL is synchronizing the frequency of converter with the grid frequency and it remains locked to 50 Hz during the normal operation. When the power sharing of converter is stopped suddenly due to the DC fault, frequency drops for a very short period and is restored during the fault period. As the converter power sharing is restored, frequency is raised again for a short span. This nominal frequency fluctuation is due to the intrinsic property of AC systems when load or generation is suddenly changed. It has no impact unless they are out of range [79]. Frequency of grid during the fault period is shown in Figure 4.28b.

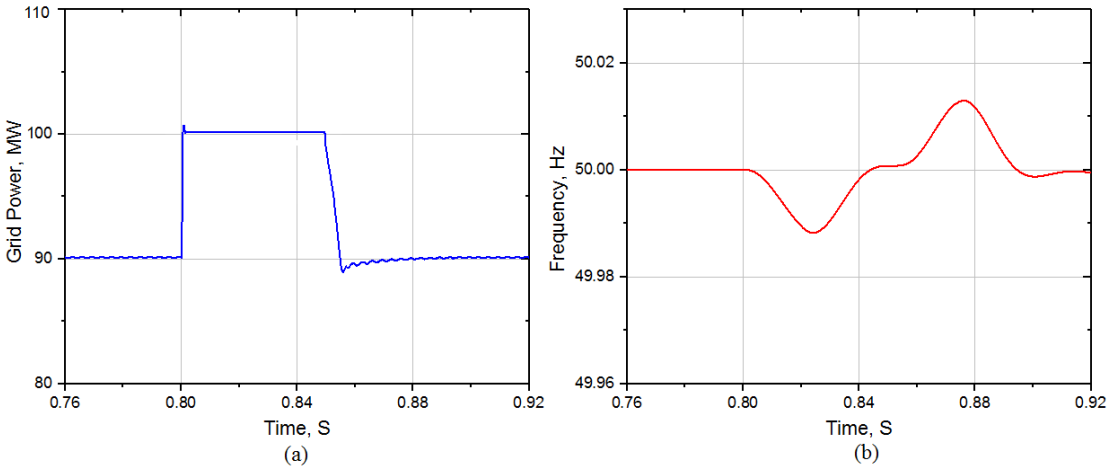



FIGURE 4.28: SCSM MMC Grid terminal parameters during fault period: (a) Grid Power and (b) Grid frequency

## 4.7 Deduction from Simulation Results

Half bridge sub module based MMC has the lowest number of cells but results have proved that this cell cannot block DC faults which can permanently damage the converter if not used with expensive DC circuit breakers. This inability raised an opportunity for other cells to be used which have DC fault blocking capability. Similar controller can be used with Full-bridge sub modules but at the cost

TABLE 4.2: HBSM-FBSM Vs. SCSM in 09-level MMC

| Cell type | HBSM | SCSM | FBSM |
|---|---|---|---|
| **Total Number of IGBTs** | 96 | 144 | 192 |
| **Total Number of Cells (SMs)** | 48 | 24 | 48 |
| **Total Number of SM capacitors** | 48 | 48 | 48 |
| **DC Fault blocking capability** | No | Yes | Yes |
| **Cell level control complexity** | Simple | Complex | Normal |
| **Post Fault transient response** | Poor | Excellent | Not Tested |

of double number of switches. So among others, switched-capacitor sub-module (SCSM) has been tested along with the designed logic converter, and found to be appropriate for the use with multilevel modular converters. The designed logic gate converter disables all PWMs during the fault condition thus turns off all the switches to avoid any contribution of grid towards the DC side fault. Results have shown the proper turning off of the converter during the fault condition where no grid contribution towards the DC side fault has witnessed. Power injection is easily restored by resetting the controller and enabling the PWM when the fault is removed. Stable and controllable response has been witnessed during the fault and normal conditions. Deductions can be summarized as in Table 4.2.

## 4.8 Chapter Summary

In this chapter a simulation model of 100 kV 09-level MMC tied to a 220 kV AC grid is built in Matlab/Simulink environment for the testing and verification of the designed architecture. Half-bridge based MMC is tested initially and found to be ineligible for handling DC side faults. Afterwards SCSM based power stage is simulated along with the designed logic converter using the same model. The results of final simulation shows the satisfactory response of the converter during the normal and DC side fault period. Results have also verified the full controllability on the converter during all modes of operation.

# Chapter 5

# Conclusion and Future Work

This work aimed at the study for the choice of sub-module to analyze its performance and suitability on the basis of components used in a single cell for the selection of appropriate sub-module for HVDC modular multilevel converter application. Therefore to achieve this goal different sub-modules are compared on the basis of number of semiconductors, required voltage sensors and DC fault blocking capability. HVDC application has been considered for the converter due to the fact of changing trend of power requirements from HVAC to HVDC. Advantages of HVDC over HVAC, emergence of multilevel modular converter and its structure is presented along with the selection criteria of sub-module. For further motivation, demand of HVDC systems and the contribution of voltage source converters in commercial HVDC systems has also studied.

DC side faults along with their solutions are identified where the DC fault blocking capability of sub-module is highlighted. Among all, the switched-capacitor sub-module (SCSM) is selected as an appropriate cell to be used with HVDC MMC. In order to implement this cell in MMC, its operational details are studied and tested. After the selection of sub-module, the aim is to interface it with the conventional half-bridge based MMC controller for which a gate logic controller is designed to interface the selected sub-module directly with controller. Later, for modelling of nine level modular multilevel converter, mathematical model for AC side dynamics of MMC are studied in view of literature and based on this mathematical

model the converter control is considered which involves dq0 transformations, grid synchronization and inner current closed loop control.

As per author‘s knowledge, the novelty of this work is to provide the comparison of different MMC sub-modules for the selection of SCSM and its logical interface with the conventional MMC controller. This work encloses all the aspects for which switched-capacitor sub-module along with its logical designed interface should be considered as a promising candidate, among other sub-modules to be utilized in N-level HVDC MMC systems.

## 5.1 Conclusion

After analyzing the results obtained through the simulation model of grid tied 09-level MMC using the HBSM based power stage and later SCSM as a sub-module along with the designed architecture, this entire work is concluded in the subsequent paragraphs as follows;

Modular Multilevel Converters (MMCs) is now very attractive for all power applications due to its several advantages however DC fault protection remains major challenge. DC side fault blocking of sub-modules has given a substantial importance in research domain in recent years due to the fact that this ability allows the engagement of the MMC in power systems without expensive HVDC circuit breakers The choice of the sub-modules generally depends on the voltage rating, number of semiconductors, sensors required for the voltage measurement of cell capacitor and ability to block DC side faults.

Based on the study switched-capacitor sub-module is selected and found to be appropriate for the use with grid tied MMC because of having medium number of semiconductors, less number of voltage sensors, inherently capacitor balancing and DC fault blocking capability when compared with different sub modules. However the SCSM has increased number of IGBTs and a unique switching pattern when compared with cascaded half-bridge sub module therefore, a logical interface is

required which can convert the merged PWM of cascaded HBSM to the pulses required for SCSM for use with conventional controller.

Gate logic converter based on simple logic gates is thus designed to modify the nine-level MMC HBSM conventional controller for its direct interface with SCSM based power stage. The logic converter is initially tested autonomously with SCSM using PWM generator, and simulation results showed the desired conversion is successful for the four possible states against two merged PWMs. All logical truth tables regarding the whole PWM conversion process which are also presented in this work have agreed with the simulation results.

The designed architecture is tested and verified using a simulation model of 100 kV 09-level MMC tied to a 220 kV AC grid. Half-bridge based power stage is used with the modeled MMC to test its response towards the DC side faults. Simulation results have shown the inability of Half-Bridge sub module for handling DC faults. Afterwards SCSM based power stage is simulated along with the designed logic converter using the same model. The results of final simulation shows the satisfactory response of the converter during the normal and DC side fault period. The designed architecture is successfully operated with the conventional MMC controller which has also eliminated the requirement of heavy lookup tables for the switching of SCSM. Results have also confirmed the full controllability on the converter during all modes of operation with the less number of voltage sensors (50%) and used 48 PWM signals instead of 144 PWM signals from the controller side when used without the designed logic gate converter. This in results reduces the computational burden and complexity of controller so the reliability of system is enhanced. Therefore it is concluded that SCSM based power stage when used with the designed architecture provides a feasible and reliable solution for use with HVDC MMC systems along with the elimination of expensive DC circuit breakers, but at the cost of more number of logic gates and semiconductors when compared to HBSM based power stages.

## 5.2 Future Work

The work performed in this thesis provides a base for number of future works such as the designed logic gate converter may be implemented in the controller without changing the control philosophy which will provide a software based solution instead of using logic gates in hardware. Other topologies, such as three-level modified switched capacitor sub module [80] for MMC can also be implemented by designing a new converter for interfacing with conventional HBSM based MMC controller.

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