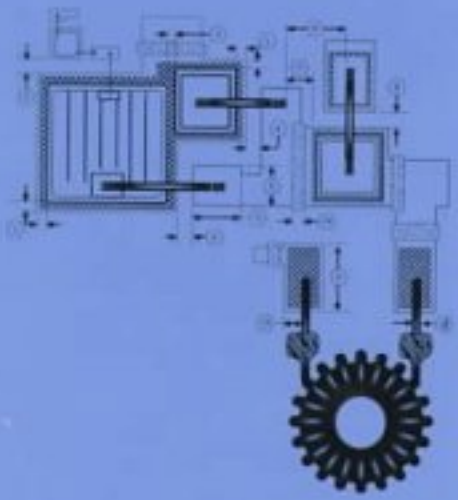
Power Hybrid Circuit Design and Manufacture



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To
my parents, Jehoshua and Fania
my wife, Bela
my children, Rina and Lilac
and grandma Doba

Preface

The trend of continuous efforts to achieve a higher degree of integration while maintaining overall reliability of military, aerospace and commercial systems resulted in higher power and current densities at chip levels. Hybridization became a major factor in the acceleration of this trend. Designers of hybrid circuits are faced with increasing demands to create unique custom and off-the-shelf standard high power hybrid functions, which cannot be achieved by using any other packaging approach. High current and power densities require special consideration related to die size, total chip power, maximum junction temperature, as well as methods of layout, packaging and mounting, thermal characteristics of materials, and type of external cooling.

This handbook concentrates on a variety of design and manufacturing techniques and materials used in high reliability military and commercial power hybrids, and is an attempt to distill my experience into a conveniently compact, readable, and yet authoritative reference. It was developed to provide a hands-on approach to learning the necessary tools and techniques to those who wish to understand the theory and practice of hybrid microelectronics. Some of it is addressed to the engineer who has had little experience with hybrid microelectronics, and to the advanced engineering student. Other parts of the text are intended for engineering managers, systems designers and hybrid development engineers.

The first chapter contains a general introduction into hybrid microcircuit

technology and provides comparisons of alternative electronic packaging techniques. Chapter 2 describes a vast variety of components used in power hybrids: principles of their operation and guidelines for selection. Chapter 3 is dedicated to materials used in the construction of power hybrids with practical recommendations for their selection and use. Chapter 4 focuses in detail on design issues: process flow, system partitioning, package selection and design guidelines with step-by-step instructions to assure performance, reliability, and manufacturability of the power hybrid microcircuits. The information discussed in Chapter 5 is needed to understand the thermal characteristics of materials used in power hybrid construction, guidelines for their selection and methods of process control and hybrid performance evaluation. Chapter 6 provides a description of current manufacturing processes and methods used in production. They include substrate fabrication, assembly and testing. The last chapter contains information on advanced applications of power hybrids and modules.

HAIM TARASEISKEY

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1—
Hybrid Microcircuit Technology

1.1—
Introduction

The ever-changing global marketplace has had an impact on materials suppliers, hybrid manufacturers, and customers in terms of competition, technology innovation, and applications. Power hybrid manufacturers are making advances in packaging, circuit design, and performance that promise to spark new market growth where users require high voltage, high current, and more reliable circuitry. The increasing limitations on space and weight in military and aerospace systems have increased demands to achieve a higher degree of integration while maintaining overall reliability and performance. The development of complex monolithic integrated circuits, while increasing component density, did not solve this problem since simultaneously systems became more sophisticated. Today's high-performance military equipment is literally packed with electronic systems that must be designed to provide the most efficient volume utilization with required performance.

The electronics industry is undergoing a profound change. Converting technologies across boundaries — especially from defense to commercial applications — is a complex process. As with any market, especially commercial, customer demands and expectations are different, delivery is critical, and reliability and cost become differentiators. The industry demands production of a quality product on time and within the budget.

As the electronic technology matures, the system complexity grows, the technology requires new packaging techniques aimed at a higher density of circuit elements operating at high voltage and current levels with high power dissipation. Increased operating speed, current, and power levels present new challenges to hybrid designers who are developing new materials, processes, and packaging techniques to cope with these factors. The unique requirements of power hybrids place special demands on selection of materials, processes, and packaging techniques.

Power hybrids require new techniques that, although similar to conventional hybrids, require equipment and approaches that many hybrid manufacturers are not comfortable with nor are equipped to handle. The heavy wire sizes and larger die that have to be mounted using precision controlled processes, as well as static sensitive components, i.e., power metal oxide semiconductor field effect transistors (MOSFET) and complementary metal oxide semiconductor (CMOS) logic, provide new challenges to hybrid manufacturers. These manufacturers traditionally mount smaller components and die, concerned more with parasitics affecting signal level processes. Isolation and mounting techniques that provide high power, high current, and high-voltage isolation are often demanded in power hybrids, and, specifically, power supply hybrids provide new considerations for manufacturers. Power hybrids must be constructed to be able to dissipate large amounts of heat, handle high input/output currents with minimal internal losses, and be mechanically sound and hermetically sealed when used in military applications. Despite the enormous diversity in requirements for power hybrids and their applications, consistency must be maintained relative to the design, manufacture, and test of final products.

1.2—
Electronic Packaging Techniques

Packaging is often cited as one of the most performance limiting aspects of advanced power semiconductors. Power hybrids overcome the limitations of conventional packaging and interconnection schemes and extend the operating range of semiconductor devices. At the same time, the use of power hybrids allows the designer to optimize performance by combining discrete devices from different manufacturers into unique application specific circuits. Hybrid circuit technology takes advantage of the latest advances in integrated circuits (ICs) and so is able to increase the number of functions available in a single package.

Hybrid circuits have long been answering the ever-shifting demands of a wide range of applications. Efficient assembly techniques, such as surface mounting, help produce more complex hybrids and hold power dissipation down. The hybrid circuit's enduring charm lies in its ability to bring several technologies together in one package without the compromise in performance often exacted by monolithic designs. Hybrids also avoid the problems of interconnec-

tion, reliability, and size that are encountered when an intricate circuit is executed on a printed circuit board.

There is a mixing of the relationship between printed wiring boards and hybrids. The continuing evolution of integrated circuits and printed wiring board technologies have steadily converged on hybrid applications. What was once exclusively hybrid technology is moving to board facilities. Solder screening for surface mount devices (SMD) is only one example. The reduction in the size of the board assemblies is also requiring techniques that were developed for hybrids. Surface mount technology (SMT), combined with high density, low-power circuitry is currently reducing the size of electronics. For their part, packaging and interconnect technologies have had their own revolutions to keep up with the information processing technologies. Circuit boards are continuing the evolutionary process with finer lines and more layers. New processes such as laser drilled holes and thin film deposition have pushed this generic technology farther up the evolutionary tree. Although integrated circuit technology has advanced to an extremely high level of integration, it is certain that hybrid technology will continue to complement IC technology by providing complex packaging solutions. Hybrid technology allows the integration of semiconductors of various types as CMOS, Bipolar, and Gallium Arsenide with precision passive components such as power resistors, inductors, and capacitors. Such total integration is not possible on a single integrated circuit with known or forecasted IC technologies.

The selection of a power hybrid to solve a circuit problem often takes place after a designer has evaluated other available techniques. The discrete designs often prove too costly and cumbersome and cannot meet some performance requirements particularly where temperature extremes may be encountered. Heat removal capability or dissipation is the primary performance criterion for the power hybrid package. Besides thermal considerations, packaging can play a part in defining electrical performance capabilities. For instance, design may be simplified by the use of the hybrid circuit technique because of the reduction in size, stray capacitance, and the shielding provided by the package. It is also possible to design a high-speed power device which will exceed the high-frequency capabilities, particularly due to lead inductance in the pins.

However, the hybrid technology expands and remains an ever-present tool in marketplaces as diverse as military electronics, automotive controls, industrial equipment, and consumer goods. Surface mount techniques are being applied to hybrids to increase densities and improve reliability. This increased density also provides new opportunities as hybrids no longer provide only a single function, but a multiplicity of functions on a single carrier. The integration of logic and power on single ICs eliminates certain hybrids, but provides new opportunities for increased function in hybrids. New materials provide renewed potential in the hybrid marketplace. Low-cost materials such as polyamide on aluminum in

applications that are high-volume and low-cost provide new market in roads for the hybrid manufacturer. Innovations in aluminum nitride and the widespread use of such materials provide the potential for performance enhancements not available with today's technology, and will push higher performance, and increased power densities in smaller and smaller spaces.

1.3— Hybrids in Electronic Systems

The successful development and application of a hybrid circuit starts at early stages of system design and requires interactions of representatives of several technical disciplines on various management levels. The effects of hybrid packaging upon subsystem performance, size, weight, and reliability must be determined by the systems engineer while program management must be aware of the impact upon costs, schedules, and overall program goals when selecting hybrid packaging as an alternative to a discrete assembly. The circuit designers must be able to isolate groups of electronic functions within the subsystem to ensure effective performance and efficient packaging. Concurrently hybrid engineers and technologists will select the optimum combination of components, materials, and processing techniques to provide a reliable efficient and cost effective product.

Fundamentally, hybrid microcircuits result from combining various electronic components, materials and manufacturing technologies and techniques into miniaturized electronic interconnections and packaging. By definition, a military hybrid is any hybrid which has an operating temperature range of –55°C to +125°C, is hermetically sealed, and generally is fabricated to the criteria of MIL-STD-883 and MIL-M-38534. Since military hybrids are primarily specified and purchased to form, fit, and function requirements, they may be fabricated using different substrate technologies, assembly methods, and test procedures. Substrates may be patterned with either thin-film or thick-film, and add-on components may be attached by either chip-and-wire or soldering techniques. Test procedures may be selected from MIL-STD-883, but usually minimum requirements include stabilization bake, thermal cycle, acceleration, fine and gross leak, and burn-in. Until recently, almost all military hybrids were fabricated with metal packages. However, today a new generation of ceramic packages is proving to be a reliable and lower cost alternative to the metal package. The majority of these hybrids are assembled with chip-and-wire methods. Large-area substrates with surface mounted passive devices and hermetic chip carriers are growing in size, and are expected to significantly impact future subsystem designs. Military hybrid circuits are most commonly recognized as having either standard or custom functions. Most applications for standard hybrids are building block designs, generic in nature, which can be configured with other components to comprise a custom subsystem. Military custom circuits exhibit a truly unique set, primarily

utilized in a single end-use application, or by a single customer. They offer the best attributes in package density, precision performance, and high reliability. However, custom hybrids are much more expensive than standard hybrids since they exhibit peculiar characteristics and typically are manufactured in lower volumes.

While inherently smaller-sized monolithic technologies are striking in concept, the performance levels and pricing required to reach parity with power hybrids will not be reached in the near future. Even then, it is expected that power hybrid producers will maintain a strong market niche where applications call for high-power, and custom high-reliability, and military designs. Some power hybrids will eventually be replaced by monolithics, however, power hybrids hold space-savings, cost, and thermal-management attributes that will make them practical choices for future electronics systems. Those systems will be pushing to higher frequencies and greater device densities that can be best achieved through application of power hybrids which have lower technical risk, bolster reliability, and reduce systems cost, when compared to monolithics, or in some cases discretes. For systems solutions to power networks, where electrical isolation and thermal management are paramount, the hybrid approach will pay dividends because of improved control between interconnects resulting in lower spike noise and coupling, as well as lower logic circuit temperatures that are not achievable with discretes or on a monolithic where logic and control functions are married on a single chip.

So-called power hybrid modules are the simplest forms of commercial power hybrids and include a variety of combinations of discrete components. These devices typically handle from a few hundred watts up to tens of kilowatts. In addition, hybrid modules provide thermal dissipation, electrical isolation and other performance features which are not possible using discrete components. For example, in high power, high frequency power switching circuits such as high current inverters, parasitics such as stray inductance in the connections between components must be carefully controlled. Power hybrid modules provide a cost-effective solution to this problem. In addition, the use of hybrid modules allows the integration of different types of devices such as Schottky rectifiers, bipolar power transistors and power MOSFETs in various circuit configurations which are not possible using discrete-packaged devices.

On the commercial marketplace side, these new hybrids require high current, high voltage, and high power dissipation packages, and allow more in-depth systems integration. Not only is system noise a particular problem, but now system thermal management issues must be addressed, along with mechanical design. All are crucial to the performance of the product. The industry will continue to require hybrid support at the stable level of the industry in the no-man's-land between requirements too stringent to use discretes, and volumes too low to demand full integration.

Typical market fields and applications for power hybrids and modules are shown in Table 1-1.

Perhaps the greatest mystique surrounding the so-called power hybrid is its very definition. Power hybrids being designed and produced primarily as a custom or "application specific" device rather than off-the-shelf solutions to power management and thermal control needs of a variety of products including: power supplies, motor drives, automobile and electrical systems, and industrial controls. Definitions of what exactly a power hybrid is has not been agreed upon industry wide. Some definitions are quantitative. They group power hybrids according to power density in watts/in^2 into several symbolic categories:

• Low level - less than 20 watts/in^2

• Medium level - 20 watts/in^2 to 100 watts/in^2

• High level - more than 100 watts/in^2

Others are strictly functional and use the amount of power delivered to the load by a given package. Such a definition may categorize an efficient solid state switch or a DC-to-DC converter, which may not actually dissipate very much power, as a power hybrid. For the purpose of further analysis, we shall define a power hybrid as an electronic circuit consisting of two or more devices mounted on a single or multiple substrates and packaged in a single case or subassembly using materials and techniques necessary to provide the following performance:

Table 1-1 Typical applications of power hybrids

Market field	Application
Space	Satellites, space station
Avionics	Commercial and military aircraft, RPV's and drones, missile systems, rocket boosters
Navy	Ships, submarines, torpedoes
Industrial	UPS, induction heaters, medical equipment
Consumer	Air conditioners, computer systems
Factory automation	Numeric controls, robotics
Automotive	Electric vehicles

- A path for efficient removal of heat generated by internal power dissipation
- A low resistance path for high current flow in interconnects and I/O leads
- Electrical isolation of high voltage sections
- External leads or lugs for electrical connection to the system components
- Mechanical construction with provisions for torque mounting on heatsink

The selection of a power hybrid to solve a circuit problem often takes place after a designer has evaluated other available techniques. The discrete designs often prove too costly and cumbersome and cannot meet some performance requirements, particularly where temperature extremes may be encountered. The power hybrid provides a small, rugged, and reliable solution to the designer's problem in performance, where nothing else will do. Advanced developments of new hybrid materials also provide new capabilities, in terms of performance criteria and potential cost reductions for major products.

The resulting increase in viable options of integrating ICs into more densely populated hybrids makes the hybrids themselves more powerful as tools for designers trying to squeeze improved performance and/or improved power density into designs.

2—
Components Parts

2.1—
Introduction

The design and performance of a power hybrid circuit largely depend on the selection and characteristics of the component parts — both passive and active. The definitive characteristics of these components are: large size, high power dissipation, high operating currents and voltages, and unconventional means of assembly, and testing. This chapter describes major characteristics, application guidelines, and precautions to be considered in selection of component parts and materials for use in power hybrid microcircuits.

2.2—
Passive Chip Components

The passive devices used in power hybrids include resistors, capacitors, inductors and transformers. Until recently, most of the large value capacitors and transformers were excluded from hybrids due to size limitations. New developments in materials and manufacturing technology resulted in significant size reductions of these components. Concurrently advances in new circuit topologies at higher frequencies of operation also made use of smaller magnetics possible in hybrids. Giving a new dimension of possibilities for new designs, these developments also demanded new materials and techniques of assembly and presented new challenges to hybrid designers in use and selection of new parts.

2.2.1— Resistors

Resistors are probably the most widely used components in electronic circuitry. They are used to limit the current or create voltage drops in limitless configurations. It is usually the only discrete component produced by hybrid manufacturers and therefore requires understanding of the technology and processing parameters by both system and hybrid designers. They can be formed directly on the substrate using thick-film or thin-film technologies, or in a chip form and mounted in the hybrid using adhesives. When justified, discrete resistors are also used in hybrid circuits. In more demanding applications, where resistors are dissipating more power, a special consideration has to be given to resistor material, manufacturing technology, and dimensions.

Thick-film resistor materials are available in standard values in a 1, 3, 10 progression from 0.1 to 10 MΩ/□. The resistors are normally formed directly on the ceramic substrate by a screening operation. The resistive ink is applied to the substrate via a screen with a photographically generated resistor pattern. A rubber squeegee passes over the pattern and forces the ink through the openings in the screen onto the substrate. Then the created pattern is dried and fired. Figure 2-1 demonstrates this process.

In general, thick-film compositions are dispersions of glass and metal powders in an organic vehicle, which is composed of a resin dissolved in one or more high boiling solvents. During extended storage the solid constituents of the paste tend to settle. Before using, the paste must be adequately stirred to redisperse the solids. Designers of electronic circuits are interested in a variety of resistor performance specifications. Table 2-1 lists typical characteristics of thick-film resistors. There are numerous manufacturers of thick-film pastes with varied performance. It is necessary to consult the specific data sheet to obtain accurate resistor characteristics for your application. After resistor is printed on the substrate, the print is dried in an oven or belt dryer. During drying, the solvent in the

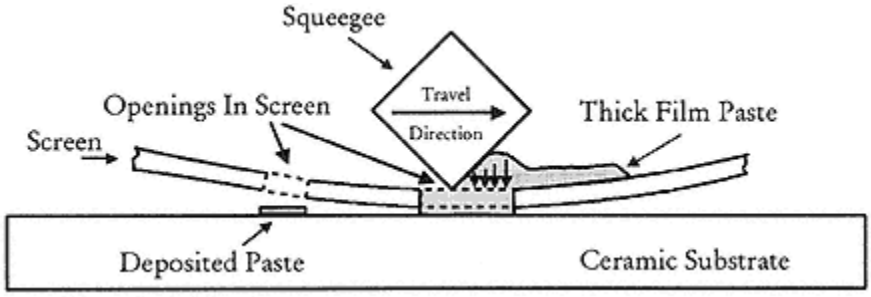


Figure 2-1
Screening thick-
film resistor paste onto a ceramic substrate.

vehicle evaporates. This process is repeated until all materials are deposited onto the ceramic substrate. During the next phase the deposited materials are fired in a furnace at temperatures near 1000°C. A typical furnace profile is shown in Figure 2-2.

Electrical performance of a thick-film resistor is strongly influenced by the firing process. When the screened resistor paste pattern passes through the furnace, the mixture of glass binder and conductive phase particles undergo sintering. The best results are obtained when sintered conductive particles are uniformly distributed in the fired resistor film. The main parameters of the firing profile: temperature rise and descent rates, peak firing temperature and process duration, vary from paste to paste and depend upon the manufacturing technology. When the process conditions are not tightly controlled, the resultant sintered resistor film is non-homogeneous and particles appear in a random distribution. It is demonstrated in the Figure 2-3.

Table 2-1 Typical parameters of thick-film resistors

Resistor characteristic	Typical range	Units	Application
Sheet resistivity	0.1 - 10M	Ω/□	
Tolerance	0.1 min	%	
Thermal stability	<0.1 >0.1	%ΔR	High-rel Commercial
Thermal coefficient of resistance (TCR)	50 - 150 > 150	ppm/°C	High-rel Commercial
TCR tracking	10 - 50 50 - 5000	ppm/°C	High-rel Commercial
Voltage gradient	2 - 200 > 200	V/mm	Standard High voltage
Voltage stability	< 0.1	%ΔR	
Voltage coefficient of resistance (VCR)	-200 min	ppm/V/mm	
Maximum rated power dissipation	20 - 1000	mW/mm	

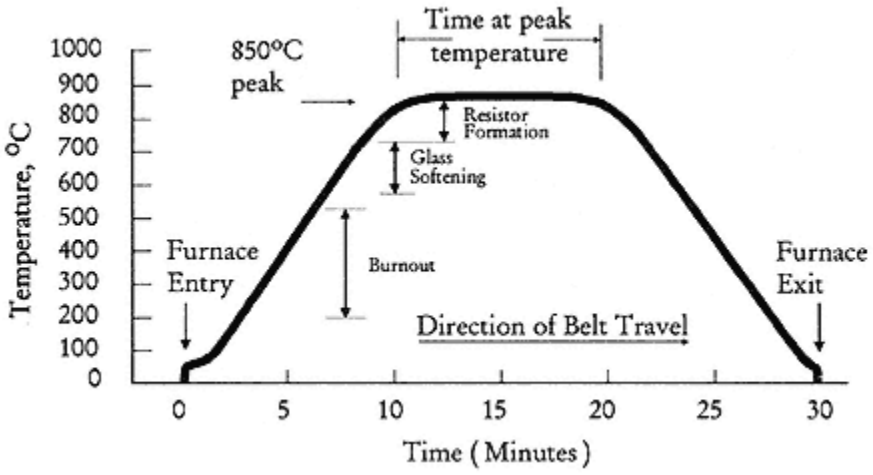


Figure 2-2
Typical furnace profile for firing thick-film resistor compositions.

When fired in a pattern a) the resistor shall function properly with application of electric field to its terminations. In case b) some very high gradients of electrical field shall be present across some parts of the resistor, affecting the conductor-glass boundaries. That may result in permanent changes in resistor value and stability, local hot spots and resistor breakdown. It is not unusual for a substrate to have 5 to 7 separate screening operations. They may include several conductor, dielectric and resistor inks. Large variety of materials, final thickness, pattern sizes and dependability on direction of screening have strong influence on distribution of resistor values. The as-fired values typically fall within boundaries shown on Figure 2-4, and may be up to 50% off the designed value. In order to achieve the specified value, resistor has to be adjusted using laser or abrasive trimmer. The latter is used only in limited applications when the volume is very

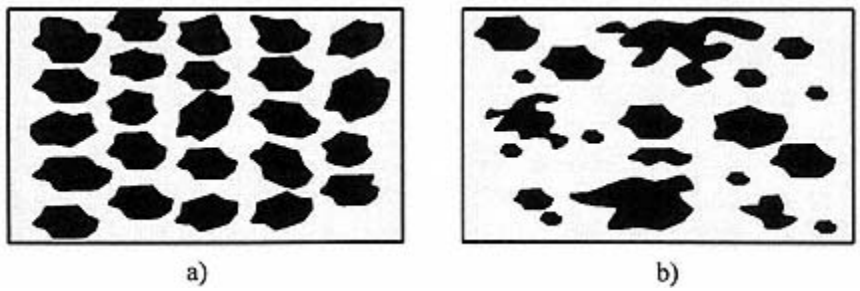


Figure 2-3
Distribution of conductive particles in a fired resistor film:
a) uniform sintering pattern, b) random sintering pattern.

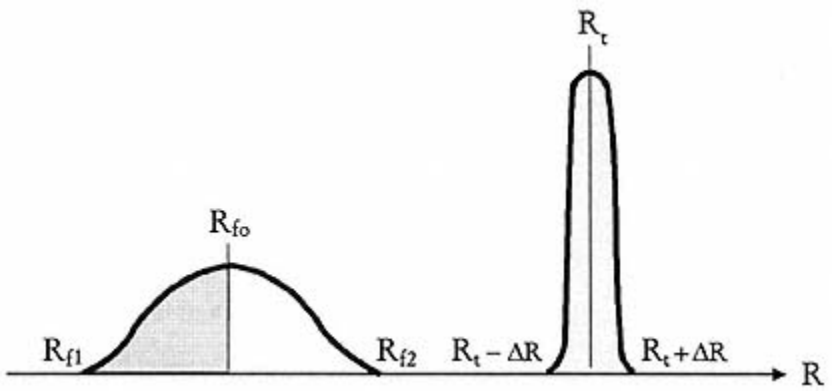


Figure 2-4
Distribution of resistor values as-fired and after trim.

small, or there are critical noise requirements. After trim, resistor values are tightly distributed around nominal values within tolerance requirements. To allow trim adjustment of the resistor its dimensions are designed so, that the asfired nominal value Rf lower than specified for application Rt ± ΔR. It is easily

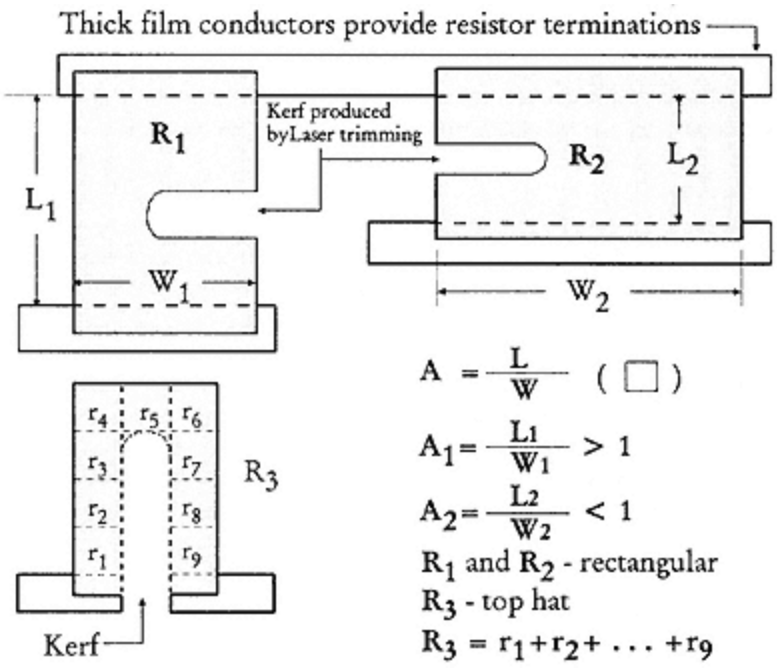


Figure 2-5
Typical configurations of thick-film resistors.

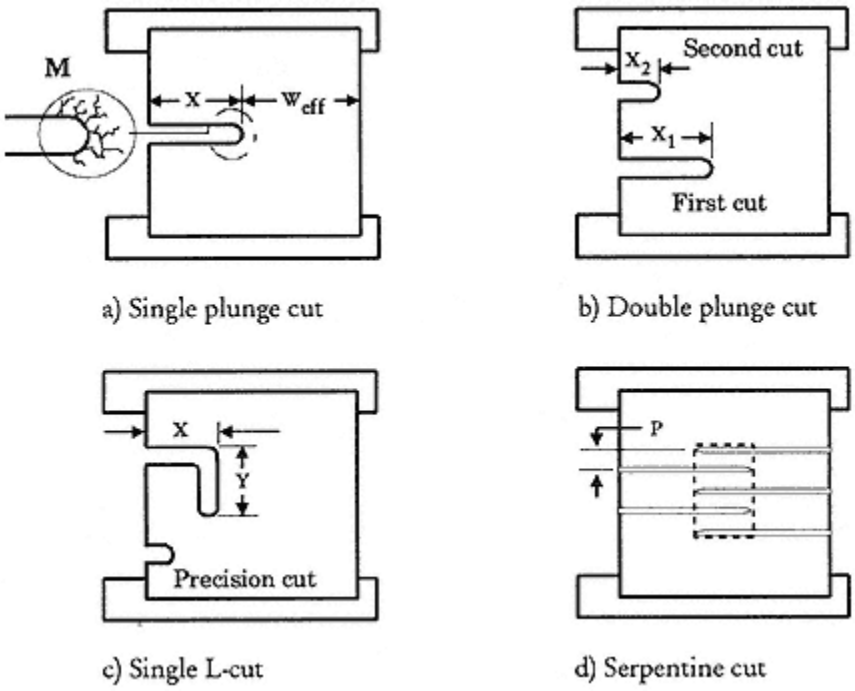


Figure 2-6
Typical laser cuts in thick-film resistors.

observed from the graphs that resistors located in the shaded area (as-fired) shall require more trimming than the other half. Deeper trimming shall leave less resistor body and may lead to very high current densities and power dissipation, causing permanent damage. Careful design and tight process control shall minimize the required adjustment of the resistor value R_{adj} and ensure reliable performance.

There are two basic resistor configurations, rectangular and top-hat (see Figure 2-5). Rectangular resistors may be designed with aspect ratio $\mathbf{A} < 1$ or $\mathbf{A} > 1$ and are used to produce resistors in entire spectrum of values. The top hat configuration yields a larger number of squares in a small area and is used when a large trimming dynamic range is required. As the count of resistor inks per substrate increases, so does the difficulty of manufacturing. At present, it is recommended not to exceed the maximum of three resistor inks and try to eliminate an additional printing by blending standard values of ink, or use discrete chip resistors. The number of inks can be increased if the resistor tolerances are 10% or higher.

There are several ways to trim the effective resistance. Most popular trims are shown in Figure 2-6. During trim, part of the resistor material is removed in

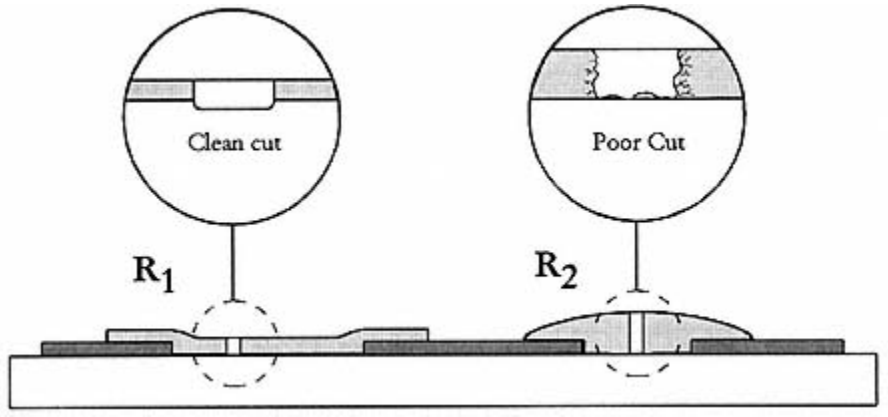


Figure 2-7
Effect of resistor thickness on laser trim quality.

order to increase its value. A high energy laser beam is focused on resistor surface and travels along the programmed path. At the focal plane, where beam's diameter is smallest, the laser energy is sufficient to vaporize the resistor material and cut all the way through it

A number of parameters related to laser system must be considered and adjusted when the equipment is set up. They include sharpness of focus, peak and average power density in the beam, spot size, pulse tracking response, and measurement bridge settling time. The channel cut by laser beam is called kerf. When the beam is poorly focused, the energy may be insufficient to evaporate the resistor material, causing damage to the walls of the laser kerf as a result of thermal shock. That produces microcracking of the resistor material into the current path, as shown in detail M of Figure 2-6(a). During trim, resistor value is increased by small increments. The system bridge is connected to resistor termination via probes, and tracks the value between laser pulses. It is very important to maintain accurate balance between trim speed and bridge settling time to achieve high accuracy trim. Such dependency may be somewhat reduced by a second plunge cut which is required to adjust the resistor value within 1–3% after the first cut is completed and the resistor has stabilized, Figure 2-6(b) and 2-6(c). A serpentine cut in 2-6(d) is used, when a larger dynamic range in resistor value change is required. Resistor performance characteristics and long term stability are strongly influenced by the quality of the kerf. Ideally, a kerf should penetrate the substrate by at least 5 μ in order to ensure adequate insulation resistance and stability. It is very critical for high voltage applications, when a poorly cut kerf functions as a parallel distributed resistor. It is recommended to keep the resistor size large enough to ensure thin and flat surface, Figure 2-7 (R_1). When the dis-

tance between the conductors is too small, the surface tension of the wet ink shall create a spherical face and prevent formation of a clean kerf, Figure 2-7 (R2). It has been found that when substrate penetration was insufficient, resistor values drifted when later subjected to elevated temperatures and stresses of the screening process of power hybrids

2.2.2— Capacitors

Capacitors are available in a large variety of types, sizes and values. Their functions include, but are not limited to, blocking of direct current, coupling of ac circuits, transient suppression, and charge-discharge characteristics in timing circuits.

Size constraints of power hybrids set a limit to the types of capacitors that can be used effectively.

2.2.2.1— Thin-Film Capacitors

Produced by vacuum deposition of thin-film dielectric such as silicon monoxide, silicon dioxide, or tantalum oxide these capacitors are sandwiched between two layers of evaporated aluminum on glass or ceramic. Primary use for high accuracy timing circuits with low time constant.

2.2.2.2— Thick-Film Capacitors

Constructed as a normal parallel plate capacitor by screen printing of thick-film dielectric ink between two or more screened electrodes on the substrate surface. Characterized by low cost with very limited range of values and performance parameters.

2.2.2.3— Single Layer Ceramic Capacitors

Raw materials in powder form are mixed, pressed and cast into shape. That process is followed by sintering to a dense ceramic with application of electrodes, leads and protective coating.

2.2.2.4— Multilayer Ceramic Capacitors

They are manufactured by mixing the ceramic powder in an organic binder and casting into thin layers of 3 mils or thinner. Metal electrodes are deposited onto green ceramic layers which are then assembled into laminate stacks. Sintering at high temperature completes the formation of the capacitor block. In the final phase the end termination metallization is applied to exposed electrodes at each end of the capacitor. See Figure 2-8 for details. Typical materials used for termi-

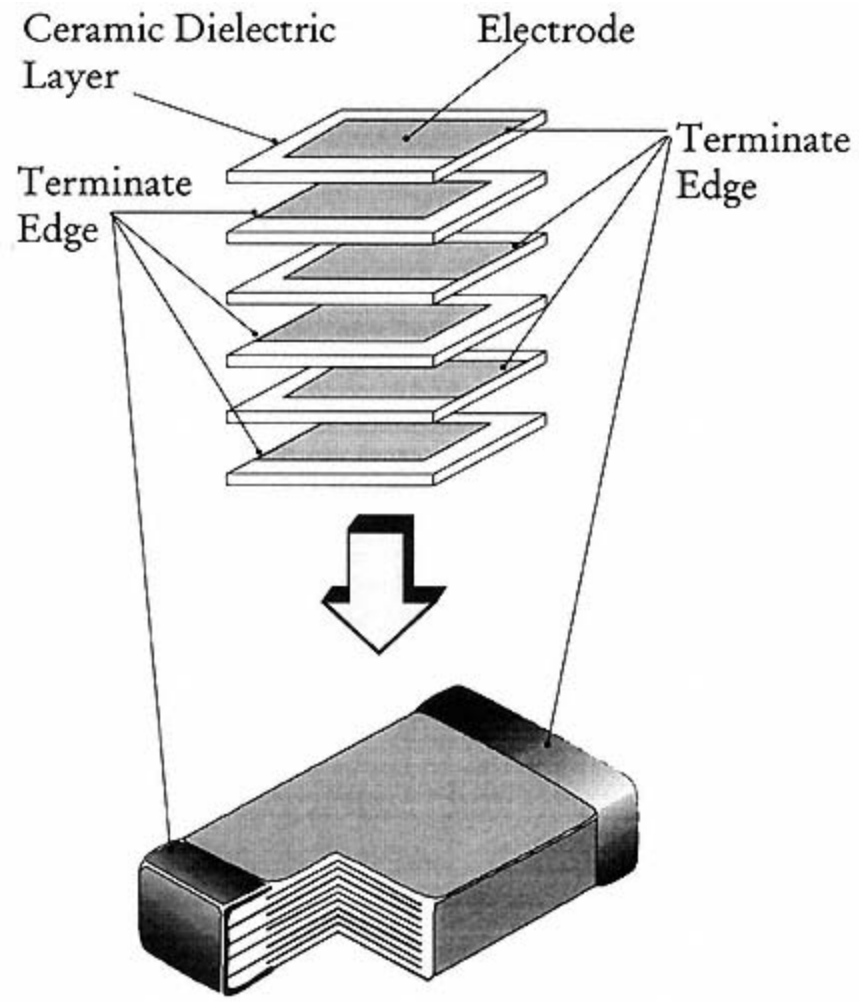


Figure 2-8
Construction of ceramic multilayer chip capacitor.

nation are PdAg, PdAg with nickel plated barrier, and Sn. The latter can be dipped solder coated using 60/40 SnPb solder. Other custom terminations are available.

Most frequently used capacitors in hybrid applications cover a wide range of values, voltages and other performance characteristics.

2.2.2.5—
Solid Tantalum Capacitors

The dielectric used in tantalum capacitors is tantalum pentoxide (Ta_2O_5) compound, which has high dielectric strength and high dielectric constant. The electrolyte is manganese dioxide, which is formed on the tantalum pentoxide dielectric layer. The pellet is coated with graphite which is followed by a layer of metallic silver, which acts as a solderable surface between the pellet and the enclosure can. This construction is shown in Figure 2-9.

Tantalum capacitors have highest capacitance/volume efficiency compared with other types of capacitors used in power hybrids. They offer excellent performance and reliability for use in military and commercial applications.

Multilayer ceramic chip capacitors and solid tantalum capacitors form the most popular group used in power hybrid microcircuits. They offer wide capacitance value selection, high voltage ratings, tight tolerances and low leakage over military temperature range. Table 2-2 summarizes the most popular types and their major characteristics.

Capacitor parameters are strongly dependent on variables such as temperature, voltage and frequency. The parameter change depends on material, type of dielectric, construction and packaging. Figures 2-10 through 2-16 demonstrate such dependence and compare capacitor dielectrics and types.

It is very important to select the right capacitor for use in the hybrid, particularly since the electrical schematic frequently does not specify all performance

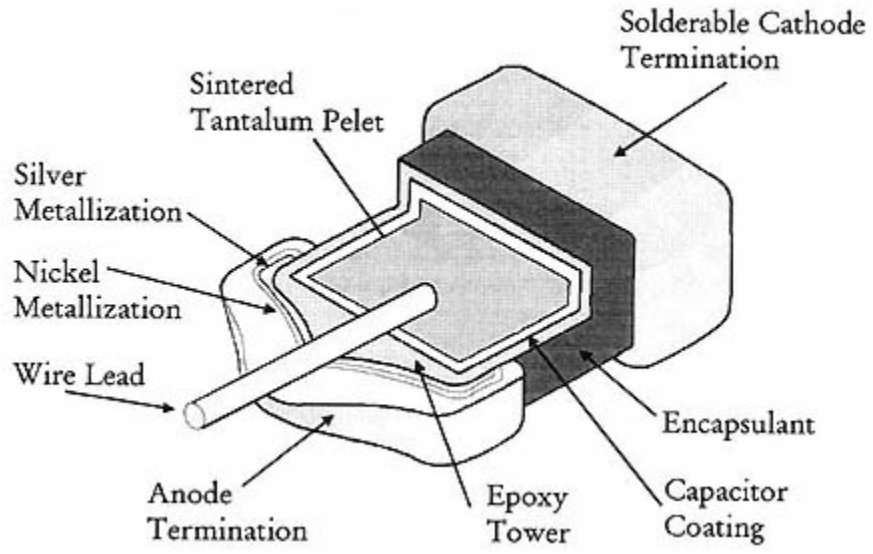


Figure 2-9
Construction of a solid tantalum capacitor.

Table 2-2 Typical characteristics of chip capacitors

Characteristic	Ceramic chip capacitors			Solid electrolyte tantalum capacitors
Dielectric type	NPO	X7R	Z5U	
Capacitance range	1 pF to .039 µF	100 pF to 5 µF	2700 pF to 1.5 µF	0.1 µF to 330 µF
DC rated voltage range	50 V to 5000 V	50 V to 2500 V	25 V to 50 V	2 V to 50 V
Dimensions (mils)	50 × 40 to 360 × 400	50 × 40 to 360 × 400	80 × 50 to 220 × 250	100 × 50 to 235 × 23.

characteristics and is limited only to the value and rated voltage. Listed below are important factors involv in the selection of capacitors:

- Capacitance value and tolerance
- Rated voltage - DC, AC, peak, and surge
- Physical dimensions
- Temperature limits
- Equivalent series resistance (ESR)
- Temperature coefficient of capacitance (TCC)

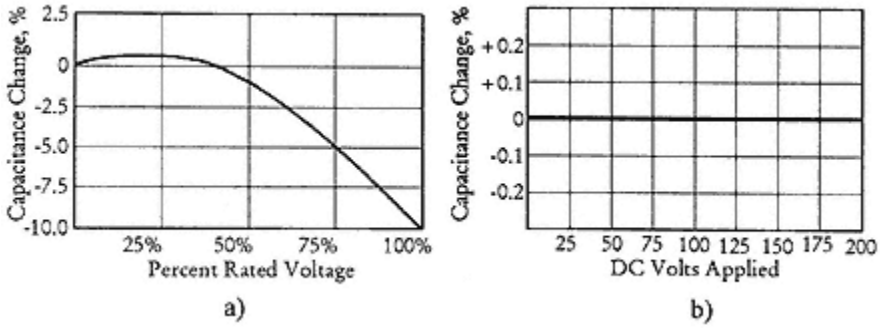


Figure 2-10
Variation of capacitance with applied DC voltage:
a) X7R dielectric, b) NPO dielectric.

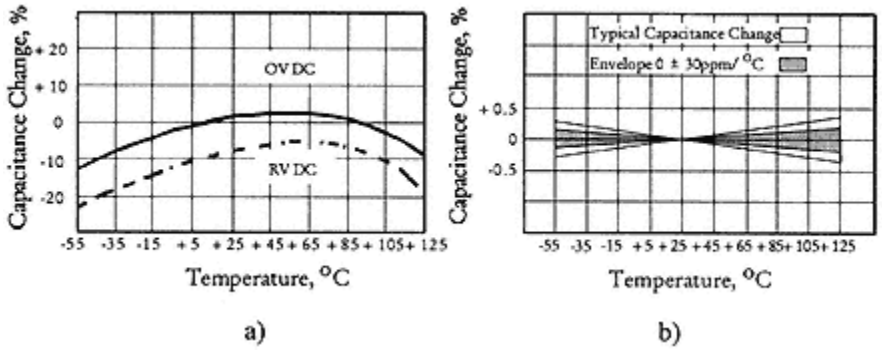


Figure 2-11
Variation of capacitance with temperature: a) X7R dielectric,
zero volt applied (——), rated voltage (— · —), b) NPO dielectric.

- Voltage coefficient of capacitance (VCC)
- Capacitance change with frequency
- Leakage current
- Maximum ripple current
- Maximum ripple voltage
- Aged stability

The graphs in Figure 2-10 demonstrate significant decrease in capacitance with application of DC voltage for X7R dielectric vs. almost no change for NPO

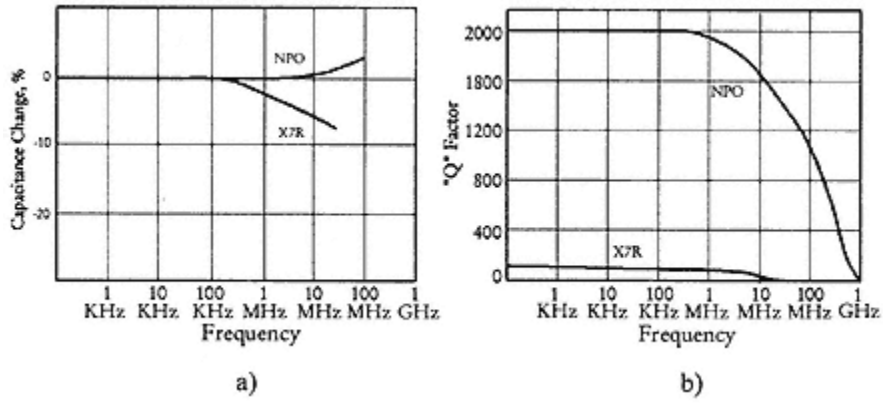


Figure 2-12
a) Variation of capacitance with frequency, NPO, and X7R,
b) variation of "Q" factor with frequency, NPO, and X7R.

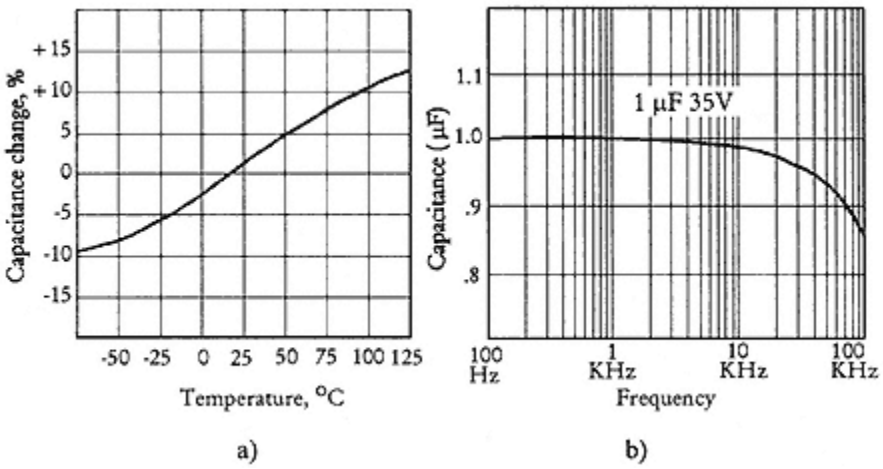


Figure 2-13
Tantalum capacitors: a) variation of capacitance with temperature,
b) variation of capacitance with frequency.

dielectric. The voltage coefficient is more pronounced for higher K dielectrics. Both capacitance and dissipation factor (DF = 1/Q) change with frequency. This variation may become significant in high frequency applications and must be

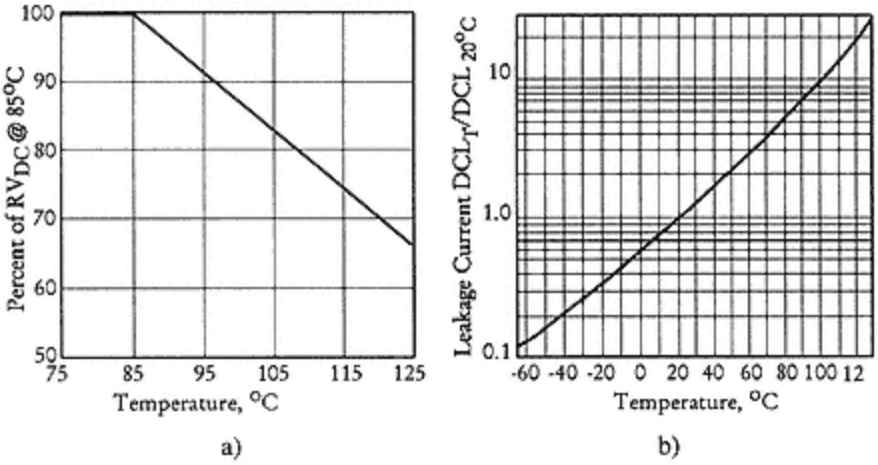


Figure 2-14
Tantalum capacitors: a) derating of maximum working voltage with temperature,
b) temperature dependence of leakage current.

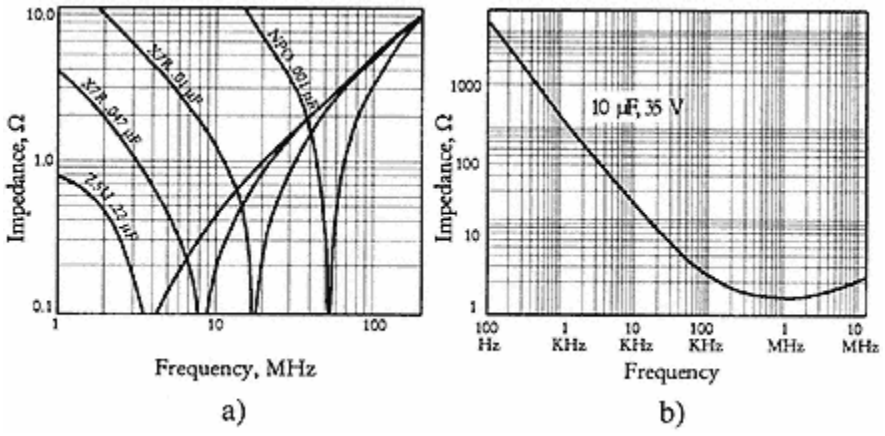


Figure 2-15
Typical variations of impedance with frequency:
a) ceramic capacitors, NPO/X7R/Z5U, b) tantalum capacitors.

carefully considered during component selection. The capacitance of a tantalum capacitor changes with temperature as shown in Figure 2-13a. The rate of change is also dependent on capacitor side and rated voltage.

Rated working voltage is a maximum continuous voltage that may be applied to the capacitor. It is usually ratedat 85°C and then linearly derated to 2/3 of rated voltage at +125°C - the upper limit of military temperature range. The variation of leakage current with temperature is shown in Figure 2-14. In addition, it also depends on applied voltage and rapidly increases with increase of

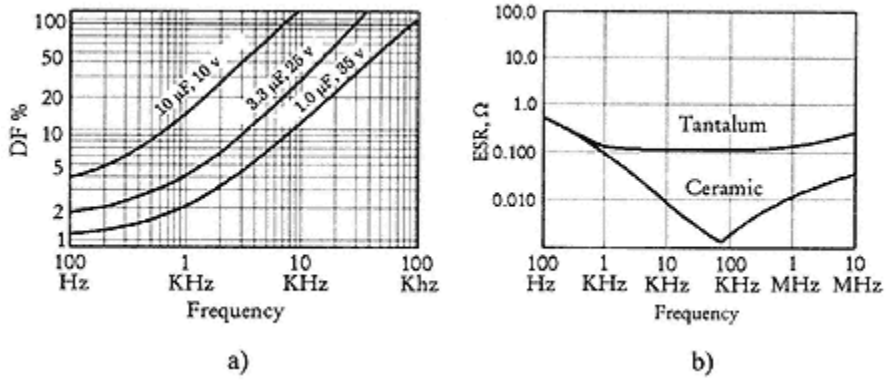


Figure 2-16
a) Dissipation factor vs. frequency, tantalum capacitors,
b) ESR vs. frequency, ceramic and tantalum capacitors.

voltage. Total impedance of capacitors consists of series resistance Rs, capacitive reactance X_C and inductive reactance X_L and is equal to

$$Z = \sqrt{R_S^2 + (X_C - X_L)^2}$$

Every capacitor shall exhibit a complex impedance, which will be resistive in one frequency range, capacitive in another and inductive in still another. At very low frequencies, the capacitor is primarily resistive and the impedance is determined by leakage current through the shunt resistor. As the frequency increases, the current starts flowing through series resistor and capacitor and the impedance decreases. The series resistance may be due to resistance of leads, metallization, contact resistance and the assembly itself. At the resonant frequency the impedance has the lowest value and is controlled by its effective resistance. At higher frequencies, the inductive reactance increases and the capacitor starts behaving as an inductor. When the voltage is applied to an ideal capacitor, the charging current flows and the phase difference between voltage and current is equal exactly to 90°. But the real dielectric is not a perfect insulator and is characterized by leakage and polarization losses. Dissipation factor (DF) is the tangent of the angle by which the current lags from the 90° vector to the voltage and is usually expressed as percent dissipation factor. It can also be defined as a ratio of energy dissipated to energy stored. This parameter is frequency sensitive as shown in Figure 2-16a. Equivalent series resistance (ESR) is the sum of the electrode resistance and loss tangent of the dielectric. It is frequency dependent and must be given serious consideration when used in applications which require low losses.

2.2.3— Inductors and Transformers

The advanced research and development in ferrite industry over the last decade has produced a large selection of magnetic components. They come in a broad range of electrical properties and mechanical sizes and shapes. Magnetics are widely used in numerous applications of power circuits. With significant improvements of power semiconductors — MOSFETs, IGBTs and MCTs, and development of circuit topologies operating at higher frequencies and increased efficiencies, use of smaller magnetics in power hybrid circuits became practical.

The relatively new and very rapidly evolving electronic field, such as high frequency power conversion, quickly became the domain for applications of magnetic components in power hybrids. Ferrite components are used in filters to suppress electromagnetic interference (EMI) or radio frequency interference (RFI) in order to protect sensitive analog and digital systems. The final size and shape depends on the application parameters: inductance, current level, allowable core losses, mounting, shielding, environmental stresses, etc. Ferrite materials have very high electrical resistivity, which results in extremely low eddy current

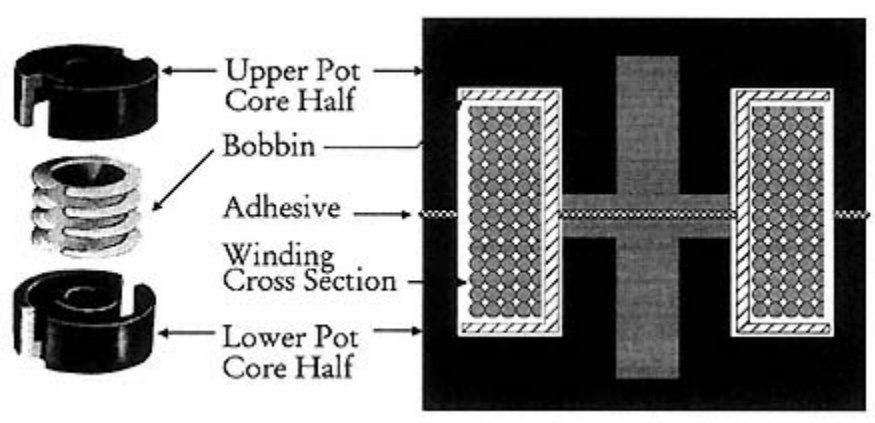


Figure 2-17
Pot core construction.

losses at high frequencies. That makes them an excellent choice for transformers in high frequency switchmode power supplies.

Ferrites are ceramic ferromagnetic materials with high electrical resistivity. Basic simple ferrite materials in very pure form are mixed, calcined, milled, granulated, formed by pressing and sintered at temperatures over 1000°C. Variations in magnetic characteristics are achieved by controlling the proportions of the materials in the mixture and by modifying the firing process. Manganese-zinc (Mn-Zn) ferrites can effectively be used at frequencies up to several megahertz. and nickel-zinc (Ni-Zn) ferrites as high as several hundred megahertz. One serious limitation for use of ferrites in power hybrids is their brittleness; they can easily chip or break during handling or environmental stresses — constant acceleration and temperature cycling. A typical pot core assembly is shown in Figure 2-17. The wire is wound on a bobbin with a single or multiple sections. The number of windings depends on application and may vary from 1 to 6 or more. An insulating layer is placed between the adjacent windings and the windings and core. After the bobbin is wound, it is placed inside both halves of the core. Ferrites are carefully aligned with each other and glued together using extra low grain adhesive. Some applications may require that the core assemblies be impregnated in vacuum to improve thermal characteristics. The ferrite pot core represents one of the most popular magnetics operating in a wide range of frequencies up to tens of megahertz. They are used in power hybrids as signal transformers, pulse transformers, power transformers and input/output filter chokes. As shown in Figure 2-17 the windings are completely enclosed inside the magnetic material with low loss, high permeability and high resistivity. Self shielding property of the pot core helps to minimize cross coupling and interference with closely positioned external circuitry. Other advantages of using pot cores include

easy winding, assembly and mounting in the hybrid.

When the core assembly is used in a high reliability military or space system, careful consideration must be given to materials used in its construction. The following parameters must be considered when selecting a core for use in high frequency power hybrid circuits:

1. Operating temperature range

2. Frequency of operation

3. Required inductance of windings

4. Change of initial permeability with frequency

5. Change of initial permeability with temperature

6. Maximum current flowing in the winding

7. Primary-secondary winding isolation

8. Physical dimensions, where height is particularly critical for hybrid assemblies

9. Core losses

10. Wire losses

11. Temperature rise of the core

12. Outgassing of materials used in assembly-adhesives, insulators, etc.

13. Ability of the core materials to trap moisture

Cores are manufactured with a preset, machined air gap by grinding the center post of the core as shown in Figure 2-17, or without it. When the DC current flows through the winding of an ungapped core, the flux in the core may reach saturation, significantly reducing the permeability of the core. Introduction of an air gap in the magnetic path reduces the effective inductance of the core, improves the tolerance of initial permeability and provides better stability with temperature variations or aging.

Types of ferrite cores that are similar in construction to pot cores include:

• RS (round slab) cores are modified pot cores with a section cut off on either side of the skirt

• RM (square design cores) can be used in assemblies with insufficient room for pot cores or RS cores

Other magnetics available for use in power hybrids are E-cores and toroids. As the switching frequency of switchmode power supplies increases, the losses

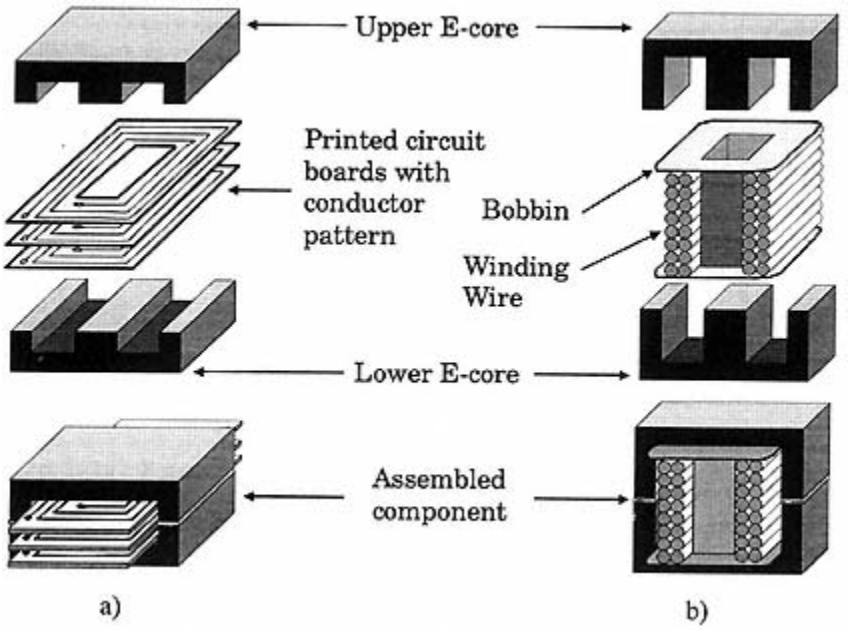


Figure 2-18
Planar magnetics and conventional approach using E-cores.

in copper conductors in the windings are growing. Current flowing through the conductor, tends to migrate towards the surface layers, as the frequency increases, creating a "skin effect". As the skin depth decreases with the square root of frequency it rapidly becomes a significant factor affecting inductor performance. With decrease of conductor cross-section, the resistance of windings increases, and so does the power loss. Two different approaches to build a transformer or inductor using E-cores are demonstrated in Figure 2-18. The traditional approach shown on the right (Fig. 2-18b) is using round copper wire wound on a bobbin. To combat the problems caused by skin effect, designers use Litz wire or foil conductors. Both methods are expensive and require almost twice the winding window area. The other, "bobbinless," approach (Fig. 2-18a) utilizes the concept of planar magnetics. The windings are spirals of copper conductor foil formed on the surface of a single or double-sided printed circuit board. For heavier currents a thicker stamped or etched copper foil is used. The windings are insulated from each other by kapton or mylar film. The advantages of this construction include high efficiency, low weight, very low profile, high power density, good copper utilization at high operating frequency, easy manufacturing and assembly. Some disadvantages are high nonrecurring costs, limited core selection, and difficulty to remove generated heat. Table 2-3 summarizes some important considerations for selection of magnetics used in power hybrids.

Table 2-3 Ferrite core comparison

Core type	Core cost	Winding complexity/cost	Shielding	Heat dissipation
Pot cores	High	Low / Low	Excellent	Poor
E-cores	Low	Low / Low	Poor	Good
Toroids	Low	High / High	Good	Good

2.3— Semiconductor Chip Components

Active devices used in power hybrid circuits essentially cover the whole spectrum of devices manufactured by the semiconductor industry. They include diodes, transistors, linear and digital integrated circuits, custo monolithic circuits. Most semiconductor devices are available in the chip form — bare unpackaged die, which are electrically probed primarily for DC parameters prior to scribing and breaking of the wafers. Dynamic characteristics, which strongly depend on packaging, voltage drops, and saturation voltages, whi depend upon device mounting and interconnections, cannot be guaranteed by the manufacturer. Power rating and thermal characteristics published by the manufacturers are related to the devices assembled in a standard package and shall be different, when assembled in a hybrid package using different materials and construction. Detailed knowledge and understanding of device construction, electrical performance characteristics and technology of assembly, interconnection, and testing are key for successful design, manufacturing, and use of power hybrids.

2.3.1— Diodes

One primary characteristic is common to all diodes, the ability to block voltage in one direction and allow flow of current when a voltage of opposite polarity is applied. Dependent on semiconductor technology an application, diodes used in power hybrids are divided into the following categories:

- General purpose rectifiers
- Fast recovery rectifiers
- Schottky barrier rectifiers
- Transient voltage suppressors
- Zener diodes

2.3.1.1—
Fast Recovery Rectifiers

A good understanding of diode's characteristics and operation allows the designer to determine correctly the stress and power losses in the circuit. By choosing the best available device he can minimize the stress and improve the reliability. The performance characteristics of diodes are discussed below. An ideal diode would be one, which completely blocks the voltage of reverse polarity and allows the current flow without losses when voltage of an opposite polarity is applied. It would have no reactive components and follow the simple voltage — current relationship developed by W. Shockley. Figure 2-19 illustrates the I/V characteristics of ideal diode. In reality the diodes do not follow the ideal behavior.

Leakage Current

When a p-n junction of semiconductor is reverse biased, a leakage current flows through the diode. Three components contribute to this current:

• I_D diffusion current, which is caused by minority carrier transfer through the junction by high electrical field. This current strongly depends on tem-

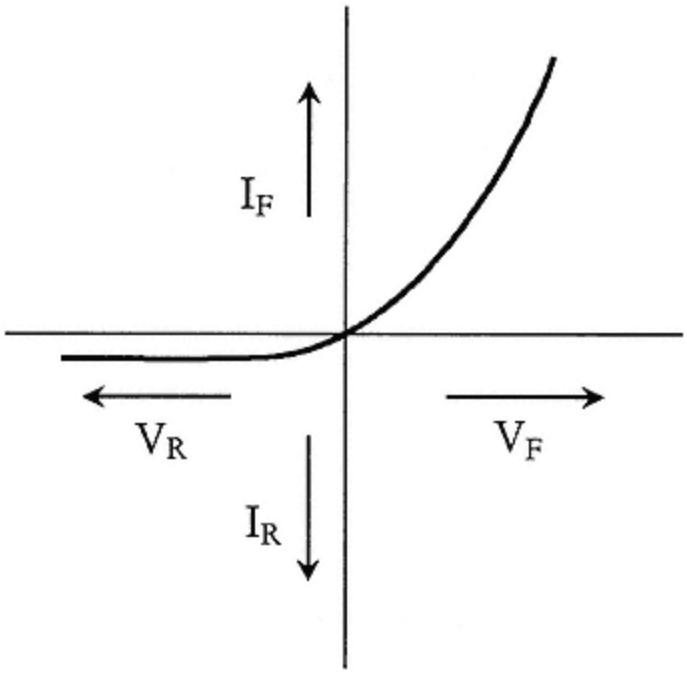


Figure 2-19
I/V characteristics of ideal diode.

perature and represents the dominant portion of leakage current in germanium and Schottky devices.

• I_G charge generation current, is due to impurity ions in the depletion layer and is a dominant portion of leakage current in silicon p-n junction devices.

• I_S surface leakage current, results from a resistance path across the junction and increases considerably at high voltages.

As a "rule of thumb," leakage current I_R roughly doubles for every 10°C increase in junction temperature, and the voltage coefficient of V_F is -2.0 mv/°C.

Breakdown Voltage

When the reverse voltage applied to the diode is increased, the current through the junction also increases. When the voltage approaches the avalanche breakdown level V_{BR}, the current starts increasing very rapidly, without limit and eventually results in damage to the device. This effect is attributed to the fact that electric field across the depletion layer of p-n junction accelerates moving particles. When they are moving fast enough, there is sufficient energy to free additional particles producing a multiplication of carriers, which causes the current to increase and may result in breakdown, which usually occurs in the bulk of the material.

Forward Voltage Drop

When the current flows through the diode, it produces a voltage drop across the bulk resistance. This voltage drop is significantly higher than one could anticipate using the ideal diode theory. Practically, the voltage—current characteristic is incrementally exponential and the curve slope varies with current density, semiconductor material, and manufacturing technology. Figure 2-20 shows forward current I_F versus forward voltage V_F curves at various temperatures for a fast recovery power rectifier 1N6305. The bulk resistivity of silicon grows with increase of the avalanche breakdown voltage. Therefore, as the reverse voltage rating of the rectifier is increased, it's forward voltage drop will also increase if the diode size remains the same.

Junction Capacitance

Charged particles of opposite polarity exist at the p-n junction. That results in a capacitive effect, creating a transition capacitor C_T similar to that of parallel plate capacitor. Additional stray capacitance may be introduced by the mounting technique or case. As the applied reverse voltage increases, the depletion layer widens and causes the capacitance C_T to decrease. This capacitance is not temperature dependent in a wide temperature range. In most applications the transition capacitance has a small effect. It has to be taken into consideration

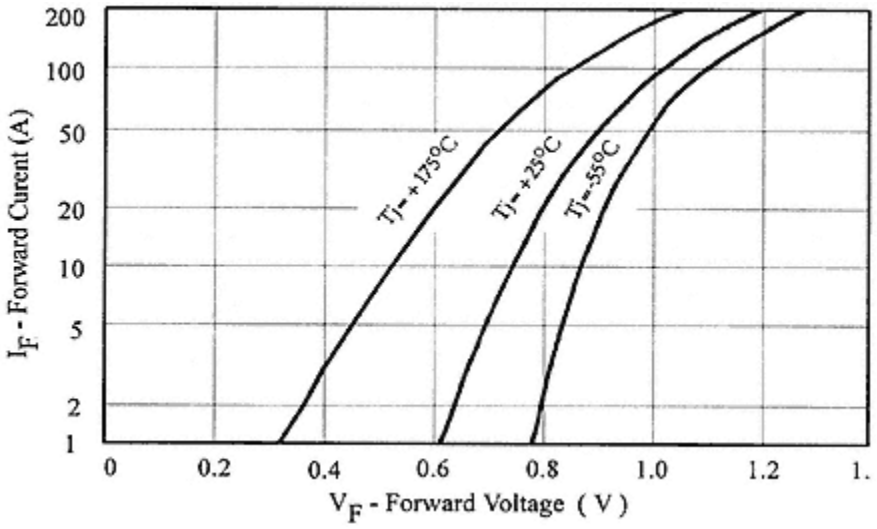


Figure 2-20
Forward current vs. forward voltage, diode type 1N6305.

when using Schottky diodes in high frequency applications, because these devices do not exhibit reverse or forward recovery transients.

Reverse Recovery

Another deviation of the real diode from ideal performance is reverse recovery caused by charge storage in the junction. When a forward current flows through the diode a carrier gradient is developed across the high resistivity region of the junction resulting in storage of charge. When the polarity of applied voltage is suddenly reversed, the current carriers which have become mobilized and diffused in the region of the junction due to forward current, shall support the current flow against the reverse field until the charge is depleted by internal recombination of carriers and opposite current caused by reversed bias. How long this current will flow depends on the reverse recovery time of the diode. But the reverse recovery time will also depend on how much forward current was flowing originally.

The reverse recovery waveform and stored charge vs. di/dt for a fast recovery rectifier are shown in Figure 2-21. During the first part of reverse recovery period t_1 the charge stored in the junction is sufficient to provide excess of current so that the diode behaves as a short circuit. The transition from t_1 to t_2 occurs when the accumulated charge has been depleted to the point, where it can no longer support the increase of $I_{RM(Rec)}$ current. During the second phase t_2, the device regains a high impedance and allows buildup of the reverse voltage. while

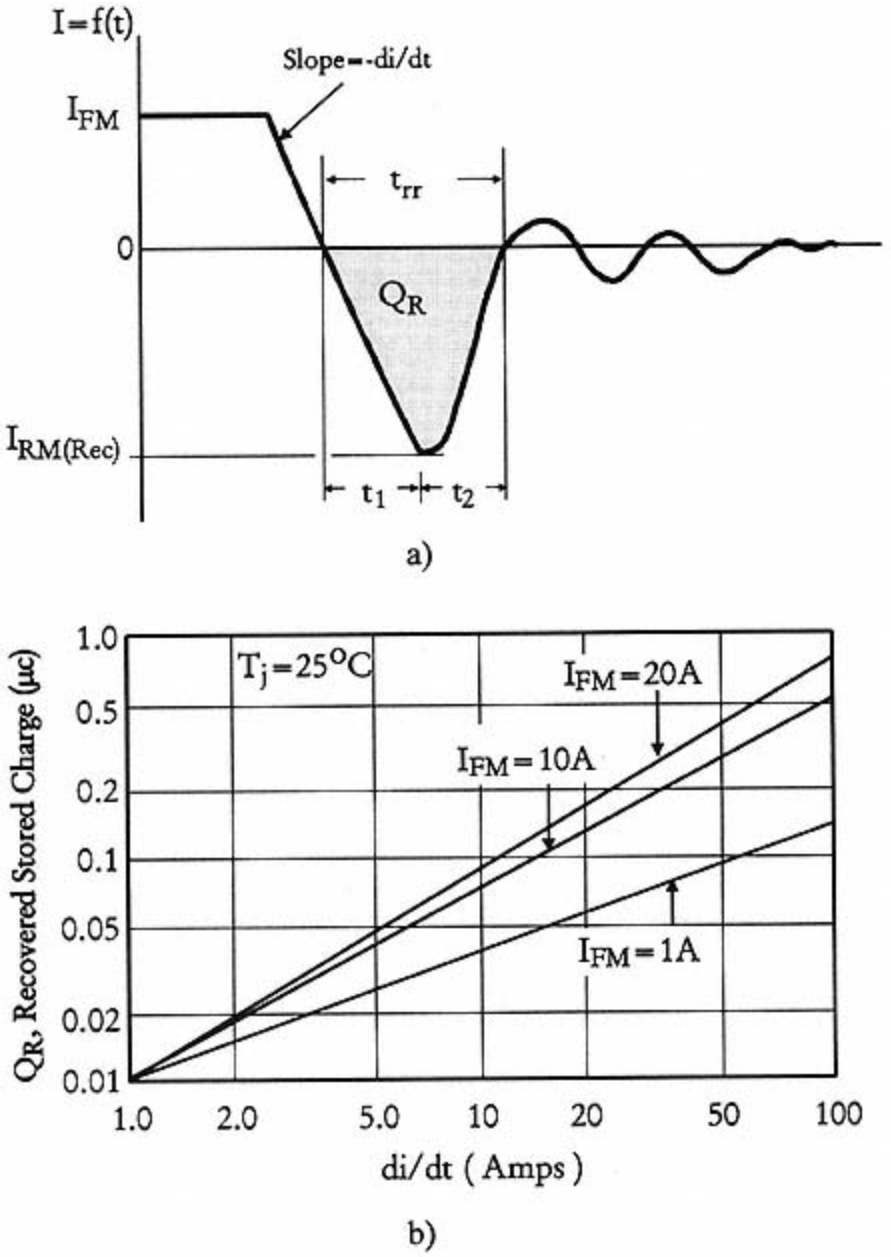


Figure 2-21
Fast recovery rectifiers: a) reverse recovery waveform,
b) typical recovered stored charge data.

still conducting the reverse recovery current. For a given forward current I_F and slope di/dt the parameters Q_R, $I_{RM(Rec)}$ and t_{rr} all increase with temperature.

The reverse recovery time t_{rr} and peak reverse recovery current $I_{RM(Rec)}$ can be calculated from:

$$t_{rr} = 1.41\left(\frac{Q_R}{R_i}\right)^{1/2},$$

where:

Q_R = recovered stored charge,

R_i = di/dt – rate of change of current from forward level to reverse peak.

If the diode is used with a transistor in a high frequency switching circuit, it should be carefully selected with t_{rr} much smaller (3 to 4 times) than the rise time of the transistor to minimize losses.

The reverse recovery time of a rectifier is measured by applying a specified forward current, then periodically reversing the bias voltage using pulses with very short rise time and specific amplitude, sufficient to cause reverse current flow. The time duration of reverse current flow will be the reverse recovery time of the diode.

Forward Recovery

When used in switching applications, diodes exhibit another undesirable phenomenon known as forward recovery t_{FR}, time required for the voltage across the diode to reach a specified level V_{FR} after application of a forward voltage pulse. For a short time after application of the forward bias pulse, the impedance of the diode is higher than its normal "on" value, because the diode cannot build a full concentration of carriers in the area of junction instantaneously. As a result a given forward current will cause a high forward voltage drop as shown in Figure 2-22. The magnitude and duration of the overvoltage depends on the application and design of the diode and may vary from no significance to a few microseconds at the worst.

Forward recovery is measured the same way as the reverse recovery time — from some point on the leading edge of the turn-on pulse to a specified point on the curve near the end of the overvoltage transient across the diode.

2.3.1.2—
Schottky Diodes

Schottky rectifiers are widely used in power hybrids due to an extremely low forward voltage drop compared with silicon p-n junction devices, even at high currents. Their construction is fundamentally different, even though it is hard to distinguish them from a conventional diode by physical appearance. The Schottky diode is a majority carrier device and doesn't have reverse recovery characteristics due to storage of minority carriers, when switching from forward

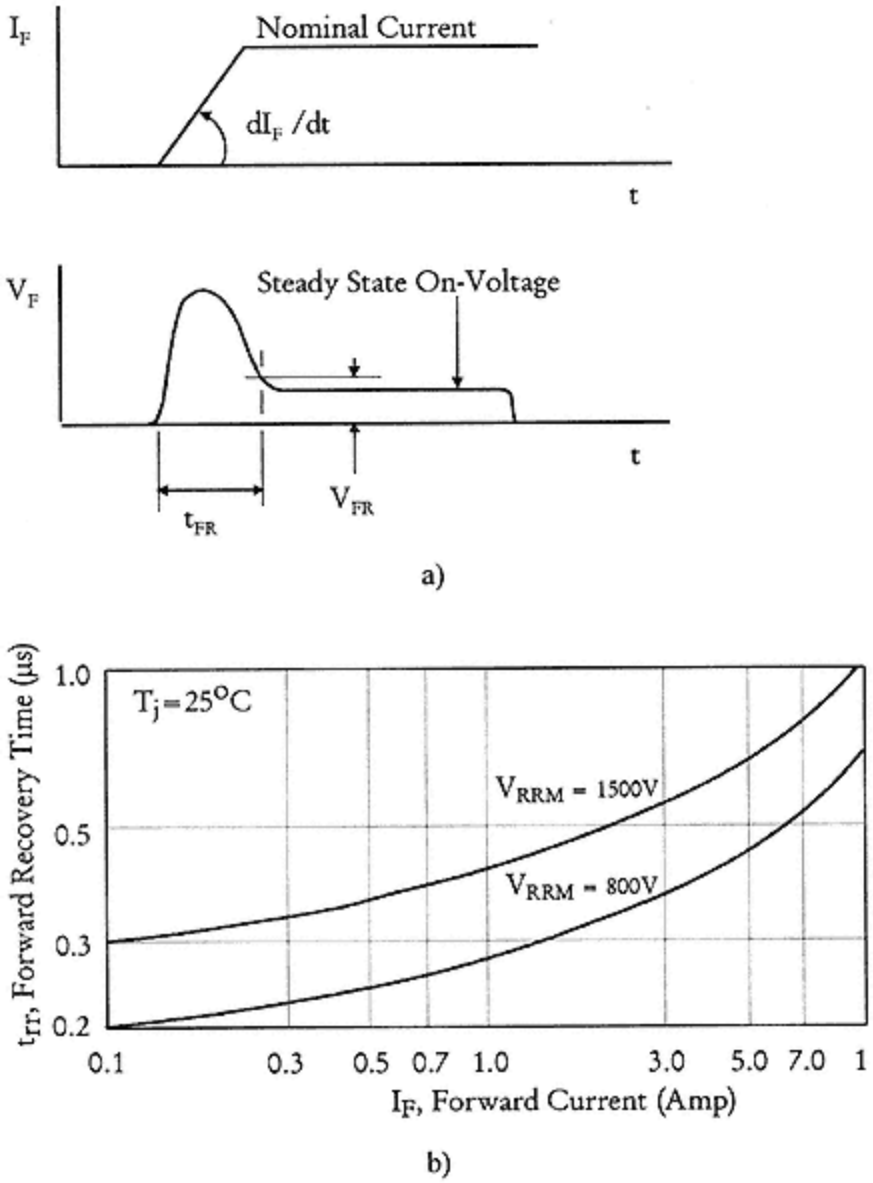


Figure 2-22
Fast recovery rectifiers: a) forward recovery waveform, b) typical recovery time vs. forward current for diodes with different breakdown voltages.

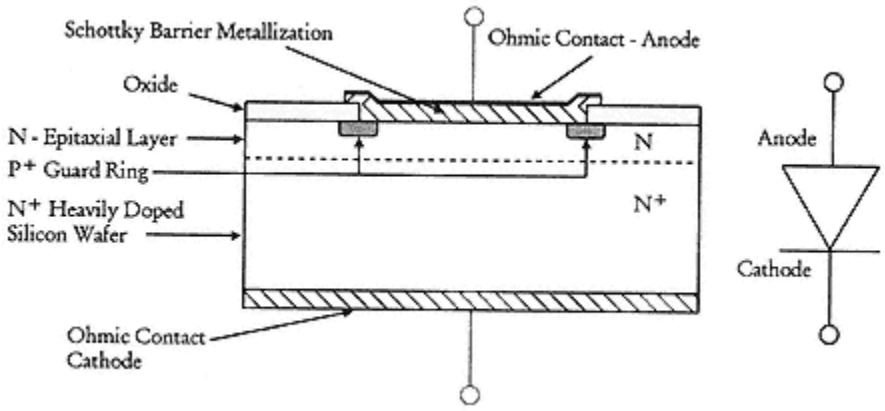


Figure 2-23
Construction of a Schottky barrier rectifier.

conduction to reverse. However, power Schottky diodes have a large junction capacitance and will exhibit a short reverse recovery time similar to a very fast p-n junction diode. Since reverse recovery effect is due largely to junction capacitance, it is virtually independent of the reverse di/dt. Figure 2-23 shows the con-

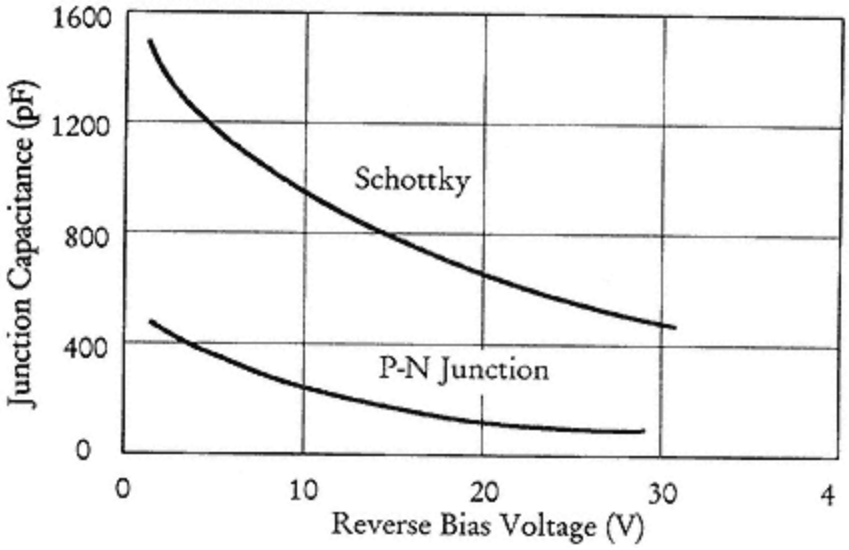


Figure 2-24
Junction capacitance vs. reverse bias voltage. Comparison of ultra-fast p-n junction rectifier with comparable Schottky rectifier.

Table 2-4 Comparison of the performance characteristics of the Schottky and fast recovery rectifiers

Type	V_R	V_F		I_R	
		25°C	150°C	25°C	150°C
1N6304	50 V	0.975 V @ 70 A	0.840 V @ 70 A	25 μA	30 mA
75HQ045	45 V	0.710 V @ 70 A	0.600 V @ 70 A	150 μA	100 mA

struction of the Schottky rectifier. N-type epitaxial layer is deposited on a heavily doped N^+ silicon wafer. The rectifying effect is achieved by the Schottky barrier, formed by deposition of a metal layer on the epitaxial layer. The characteristics of the formed rectifier, such as forward voltage drop and leakage, are affected by the type of barrier metal used. The commonly used materials include chromium, platinum, nickel platinum, and molybdenum-tungsten. A guard ring which consists of a P^+ region diffused into the epitaxial layer protects the Schottky junction from voltage transients. There are two major drawbacks related to Schottky barrier rectifiers. First, their maximum reverse blocking voltage doesn't exceed 120 volts. Second, they have higher leakage current, which rapidly increases with temperature. Table 2-4 show the noticeable differences in performance of two popular power rectifiers:

- 1N6304 - fast recovery rectifier

- 75HQ045 - Schottky barrier rectifier

Two graphs shown in Figure 2-24 demonstrate how junction capacitance changes with applied reverse bia voltage to ultra-fast p-n junction rectifier compared with comparable Schottky barrier rectifier.

2.3.2— Transient Voltage Suppressors

All semiconductor devices used in modern electronics have specified maximum ratings of allowable curre and voltages across their terminals. These ratings may be repetitive or nonrepetitive. Power hybrids are employed in circuits, where high currents from high voltage supplies are switched at high frequency. This produces high energy transients, which can exceed the maximum rated values and cause component failur The sources of transients may be internal to the hybrid circuit, such as switching of inductive loads, abrup turn-off or turn-on of the power supply, etc. They may be caused externally by system faults, switching of large inductive loads such as relays and solenoids, electromechanical devices

and lightning surges. Voltage transient in power hybrids represent a major source of semiconductor failures. Due to their small size, it is essentially impossible to shield the components or use large filters to attenuate the transients inside hybrids. Transient voltage suppressors provide significant protection against high voltage transients. When used in chip form, they are small enough to be placed in close proximity to protect sensitive devices. A list of major advantages of transient voltage suppressors are listed below:

• Protection against fast high energy transients by effective clamping

• Very low loss under normal operating conditions

• Simplification of protection circuitry

• Extremely fast clamping speed

• Immediate recovery

A range of available semiconductor transient voltage suppressors is presented in Table 2-5. The listed characteristics form the basis for selection of a transient voltage suppressor. The graph shown in Figure 2-25 helps to define these parameters:

• V_{WM} - stand-off voltage is maximum working voltage when suppressor remains virtually nonconducting. When selecting the device, the stand-off

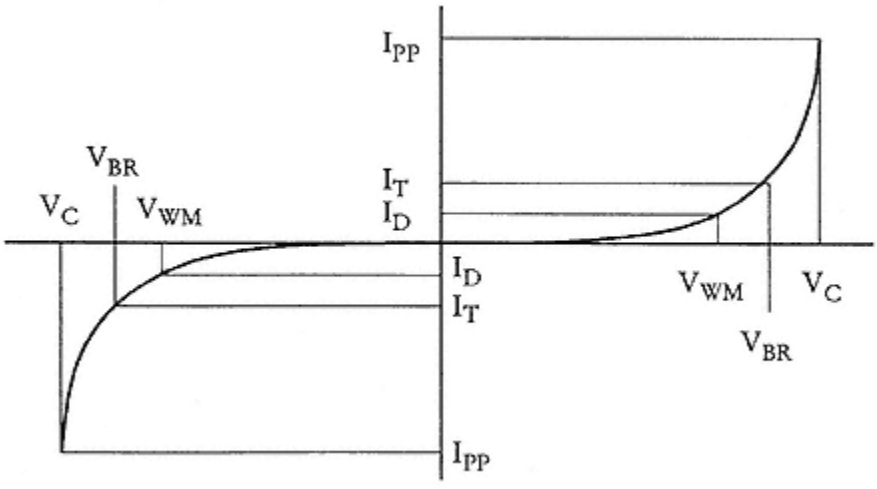


Figure 2-25
Typical characteristic curve for bidirectional transient voltage suppressor.

Table 2-5 Summary of typical transient suppressors used in power hybrids

Parameter	Stand-off voltage DC & AC V_{WM}	Maximum clamping voltage V_C @ Ipp (1 ms)	Maximum peak pulse current Ipp (See Fig. 2-25)	Response time	Maximum junction temperature
Range	5—400 V	500 V	500 A	10^{-12}s	150°C

voltage must be equal, or lower than maximum normal operating voltage of the circuit.

• V_C - clamping voltage is the maximum voltage that shall occur across the suppressor during transient condition. This voltage must be selected below levels that may damage the protected device.

• I_{PP} - peak pulse current is the maximum surge current that follows the curve on Figure 2-26. The maximum peak surge power. Peak surge power depends on pulse duration and has to be derated in accordance with manufacturer's data.

• V_{BR} - breakdown voltage is a nominal zener breakdown voltage and is specified at a certain test current level.

• I_D - maximum leakage current is defined as leakage measured at maximum DC working voltage V_{WM}.

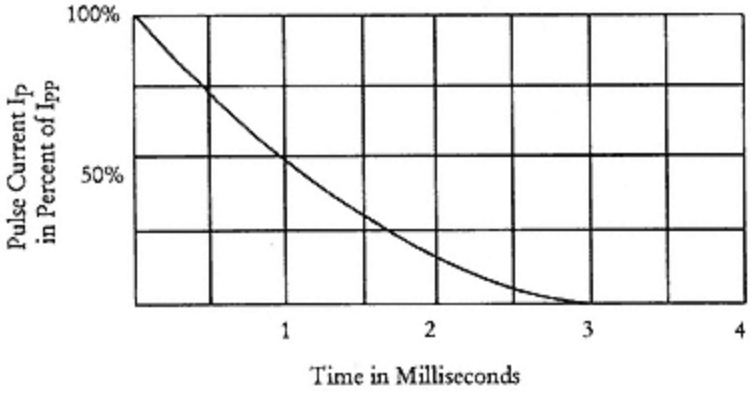


Figure 2-26
Transient suppressor, pulse current vs. pulse time duration.

• I_T - test current is zener current for measurement of breakdown voltage V_{BR}.

Transient suppressors are available in two configurations: unidirectional and bidirectional. When used in power hybrids, the unidirectional suppressor is implemented by a single chip. The bidirectional device has two chips assembled back-to-back. During clamping the suppressor absorbs the energy stored in the transient. The ability to dissipate this energy is limited by rated maximum peak pulse power dissipation, which is derated with increase of transient pulse width. Power ratings published in data books relate to a packaged device – usually in an axial leaded glass or molded case. Therefore, it is very important to carefully analyze the operating conditions in the hybrid and select the appropriate assembly technique to provide low thermal impedance for reliable operation of suppressor.

2.3.3— Transistors

Since invention of the first junction transistor by William Shockley of Bell Telephone Laboratories in 194 the semiconductor technology was rapidly progressing to meet the needs of electronic industry. The origin transistor has been constructed from a single germanium crystal with two n-type regions (collector and emitter) separated by a p-type region (base). Since then, the bipolar transistors have been made using both germanium and silicon. The majority of power transistors were constructed from silicon, due to obvious advantages: lower leakage and higher operating temperatures. That eventually led to a demise of germanium as a material for power bipolar transistors. Silicon became the industry workhorse for power transistor applications and will remain in the next decade. The properties of silicon have been thoroughly explored, resulting in nearly perfect transistors. However, the limitations of material properties of silicon present a barrier to development of future devices. Recent advanced developments in material technology wide bandgap semiconductors GaAs, SiC, and diamond

Table 2-6 Power transistor types used in power hybrids

Type\range	Bipolar transistor	MOSFET	IGBT	MCT
Voltage (V)	40 - 1500	25 - 1000	400 - 1200	600 - 1200
Current (A)	2.5 - 100	2 - 100	5 - 55	75 - 1000
Typical switching times	0.1 - 4.0 μs	20 - 200 ns	35 - 1500 ns tr << tf	200 - 1500 ns tr << tf

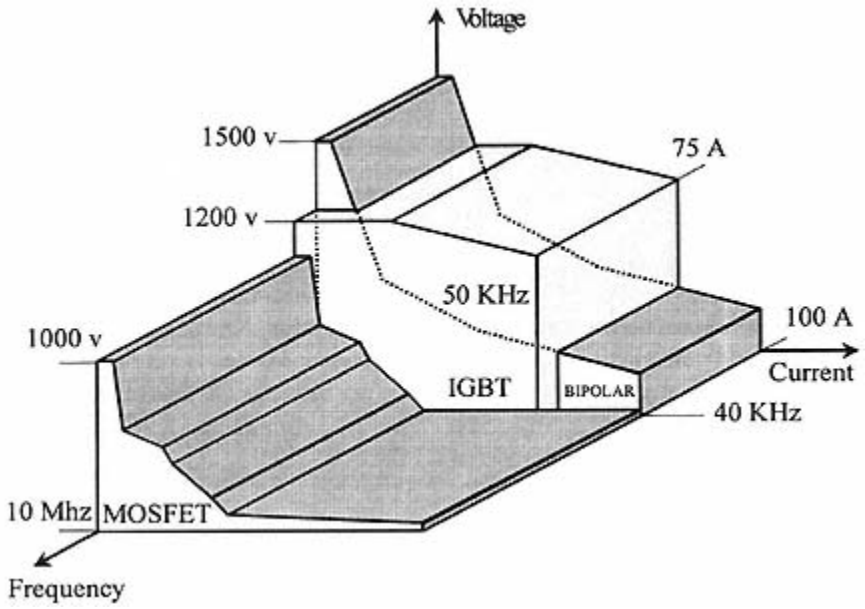


Figure 2-27
Voltage/current/frequency domain of MOSFETs, IGBTs,
and bipolar transistor applications.

films will make a significant impact on future power circuits. Power hybrids quickly adopted the technological innovations in the semiconductor field of the last decade. It came naturally, since hybrid technology offers the advantage of using a variety of technologies in a single package. Table 2-6 lists the power transistors and a range of some significant parameters. Comparison of application fields for MOSFETs, IGBTs and bipolar transistors in Figure 2-27 demonstrates advantages and limitations of modern power semiconductors. Operation of MOSFETs in extended frequency range may have to be traded for higher voltage capability of IGBTs or efficiency of bipolar transistor at lower frequency.

Superior performance characteristics made rapid acceptance of MOSFETs and IGBTs for use in high current, high voltage and high frequency switching applications of power hybrids possible. Some of their advantages are:

• High power efficiency

• Low on-losses

• Low switching losses

• Low gate drive requirements

• High current density

• High operating voltage

• High operating frequency

• Self protection

• Ruggedness

Although both MOSFETs and IGBTs have been used by engineers for a number of years, many hybrid designers use them with incomplete or inaccurate information regarding their construction and operation. Knowledge of the basic operation and construction of power semiconductor devices is very important to the designer of complex power hybrids. They are discussed in the following paragraphs.

2.3.3.1—
MOSFET

Power metal oxide semiconductor field effect transistors (MOSFET) offer unique performance characteristics and capabilities that are not available from bipolar transistors and differ from them in operating principles. In general, performance of MOSFETs is superior to bipolar transistors. They are majority carrier devices with much faster switching speeds. That allows their operation at much higher frequencies leading to a significant reduction of weight and size of reactive com-

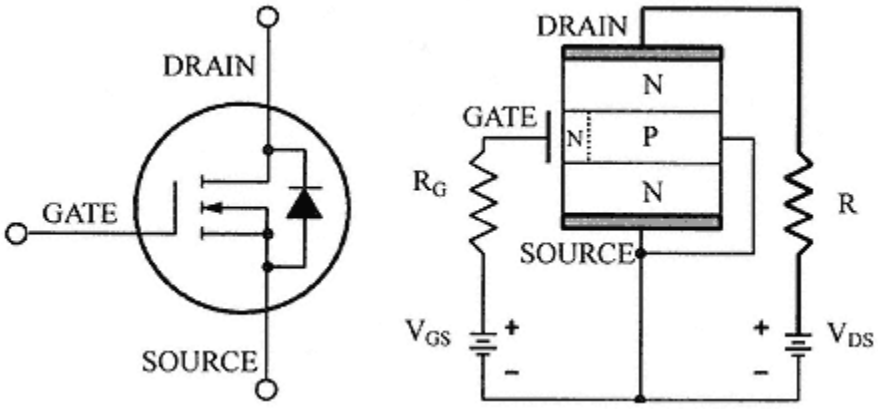


Figure 2-28
Graphical symbol and junction diagram of N-channel power MOSFET.

ponents in the system. Without minority carriers generating a charge stored in the base region, MOSFETs do not exhibit storage time, as it is common in bipolar transistors. Switching times in a MOSFET are primarily determined by charging and discharging of parasitic capacitance and therefore practically do not change with temperature. Advantages of power MOSFETs:

• High input impedance voltage controlled device

• No storage time

• Nanosecond switching speed

• Reduced complexity of drive circuit

• Easy to parallel

• High current capability

• High power switching capability

• Linear transfer characteristics

• High operating temperatures

Power MOSFETs are self-blocking transistors with three terminals: gate, drain and source as shown in Figure 2-28.

As with bipolar n-p-n and p-n-p transistors, there are N-channel and P-channel MOSFETs. N-channel devices are driven with a positive gate-to-source voltage and block positive drain-to-source voltage. Bias arrangement is shown in Figure 2-28. For P-channel types the voltage polarities are reversed. There is a much larger selection of N-channel MOSFETs than P-channel, mostly due to the fact that P-type transistors exhibit much higher drain-source on-resistance when compared to an N-type with the same die size and blocking voltage. MOSFET has a vertical design structure as shown in Figure 2-29. Drain metallization is attached to N^+ substrate. Above the N^+ substrate is an N^- epitaxial layer, whose width defines the doping concentration and the drain-source breakdown voltage. The gate structure is implemented using polysilicon imbedded in an isolating silicon dioxide (SiO_2) layer. The source metallization covers the entire structure, thus paralleling individual cells on the chip. It provides a short circuit between N^+ and P source regions. Vertical design ensures high performance of the transistor-effective dissipation of heat, high breakdown voltage, low on-resistance, and optimal utilization of silicon.

When a positive voltage V_{GS} of appropriate magnitude is applied to the gate of an N-channel MOSFET (Figure 2-28), the polysilicon gate induces an inversion layer (P-type region converted to N-type region) at the surface of the diffused channel region beneath the gate. This inversion layer allows the current to

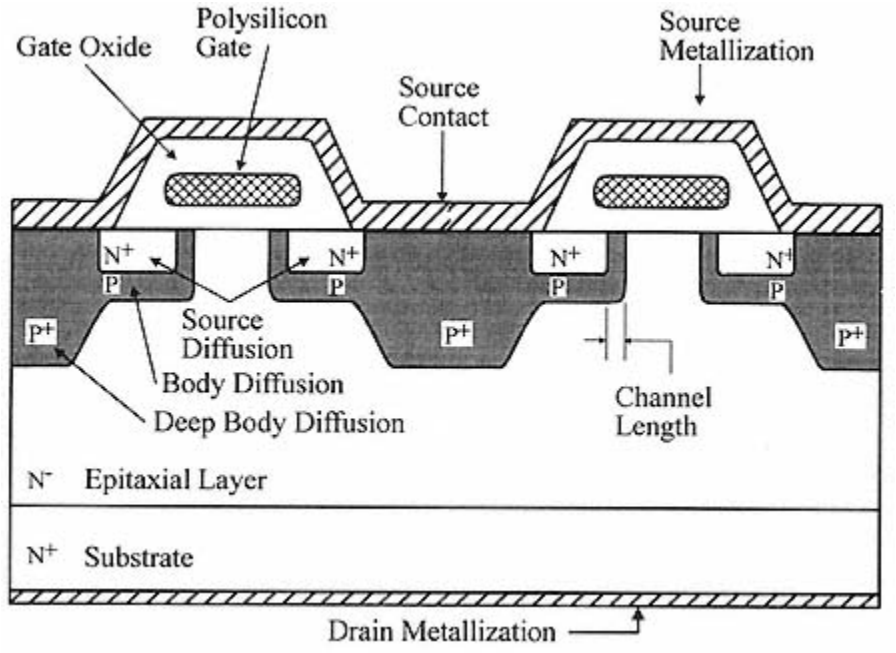


Figure 2-29
Construction of a double-diffused N-channel power MOSFET.

flow between the drain and the source as shown in Figure 2-30. During the turned-on state the behavior of a MOSFET can be represented as a drain to source resistor, which mainly consists of the sum of N- epi layer resistance and inversion channel resistance.

Each MOSFET cell has a number of inherent parasitic elements that reside in it. These are shown in Figure 2-31. The base-emitter junction of the parasitic bipolar transistor is practically shorted by the source metallization $R_{BE} = 0$ (Fig. 2-31b). This is essential to prevent the transistor from turning on during dynamic conditions. MOSFETs are free from secondary breakdown phenomena, that is, present in bipolar transistors, because they are majority carrier devices. However, during high rate of commutation in the body diode formed by p-n junction between drain and source, the base-emitter junction may become forward biased. Its breakdown voltage, BV_{CER}, will fall below breakdown voltage of MOSFET-BV_{DSS}. If the drain to source voltage applied to MOSFET shall exceed the BV_{CER} value, the bipolar transistor may go into secondary breakdown and result in device failure. The intrinsic parasitic capacitances are shown in Figure 2-31a. Gate-to-source capacitance (C_{gs}) and gate-to-drain capacitance (C_{gd} known as Miller capacitance) result from MOS structure of the cell and are formed by SiO_2

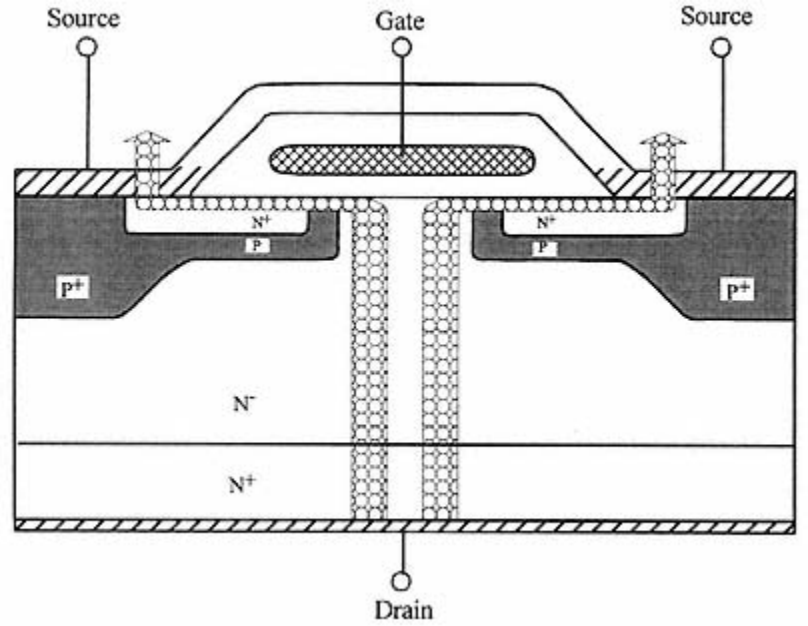


Figure 2-30
Current flow in power MOSFET.

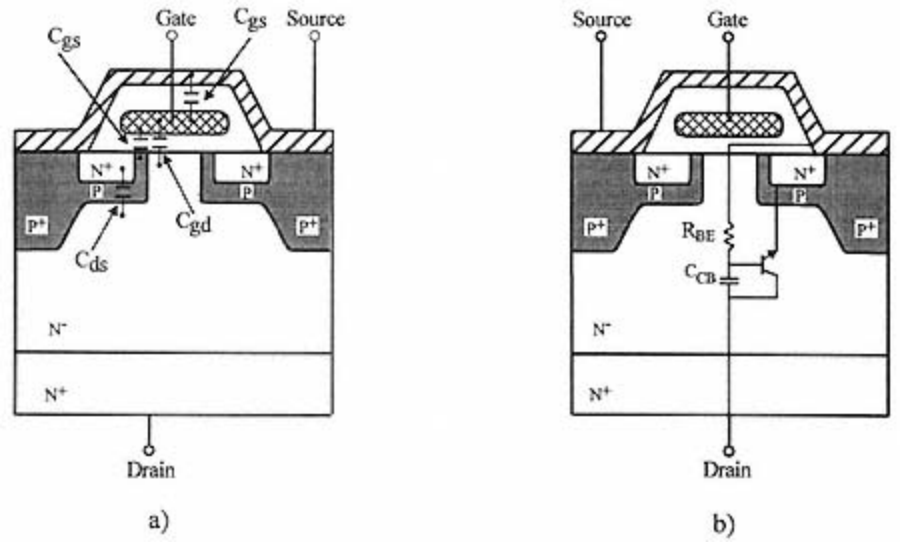


Figure 2-31
Parasitic elements shown in cross section of N-channel power MOSFET.

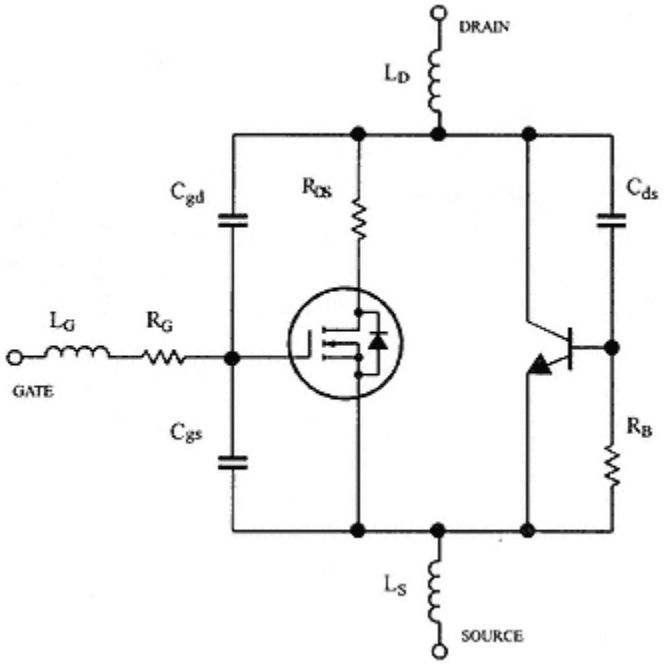


Figure 2-32
Equivalent circuit of a packaged power MOSFET.

insulator. They are very stable and practically do not change their value with temperature. The C_{ds} drain-to-source capacitance is formed by p-n junction and has the same characteristics as any other planar junction capacitance.

The capacitances shown in Figure 2-31 and 2-32 cannot be measured individually and relate to datasheet specifications as follows:

Input capacitance $C_{iss} = \dfrac{C_{gd} \times C_{gs}}{C_{gd} + C_{gs}}$ (C_{gd} in parallel with C_{gs})

Output capacitance $C_{oss} = \dfrac{C_{ds} \times C_{gd}}{C_{ds} + C_{gd}}$ (C_{ds} in parallel with C_{gd})

Reverse-transfer capacitance $C_{rss} = C_{gd}$

All three capacitances are nonlinear functions of voltages V_{GS} and V_{DS}. One of the distinct advantages of power MOSFET is its high switching speed. Switching transitions of less than 10 ns can be achieved if great care is taken during design of the hybrid layout and material selection.

Figure 2-32 demonstrates parasitic elements associated with the chip design

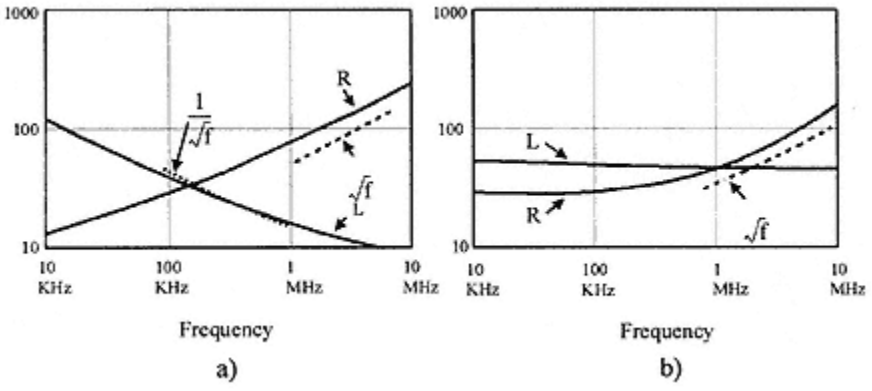


Figure 2-33
Frequency dependence of Ls and Rs: a) metal hermetic package with steel base/copper slug — TO-204 (formerly TO-3), b) plastic package — TO-220. (From Ref. 27).

C_{dg}, C_{gs}, C_{ds}, R_B, R_{DS}, R_G, and L_S, L_G, and L_D almost entirely due to package lead, wire-bond and conductor inductance. The materials used in package construction such as kovar, steel, and copper with nickel overplate define strong frequency dependence of inductance as demonstrated in Figure 2-33. Strong frequency dependence, particularly at lower frequencies for package with magnetic base material (TO-204) can be observed by comparing both graphs.

The maximum allowable power dissipation in a power MOSFET P_D is limited by the maximum junction temperature T_J, which varies from type to type between 150°C and 175°C. That power dissipation is given by:

$$P_D = \frac{T_J - T_R}{R_{\Theta JR}}$$

where

P_D - power dissipation in watts
T_J - junction temperature in °C
T_R - reference point temperature in °C
$R_{\Theta JR}$ - thermal resistance between transistor junction and the reference point in °C/watt.

The effect of junction temperature variations on the drain-to-source breakdown voltage and on-resistance is shown in Figure 2-34a and b. The positive temperature coefficient of on-resistance plays a very important role by providing its own protection against temperature fluctuations and thermal run away. Figure 2-34c is a current derating curve and Figure 2-34d is the maximum safe operating area (SOA), that apply to a specific package, in this case TO-204. When the transistor die is assembled in a power hybrid package, both graphs c) and d) have to

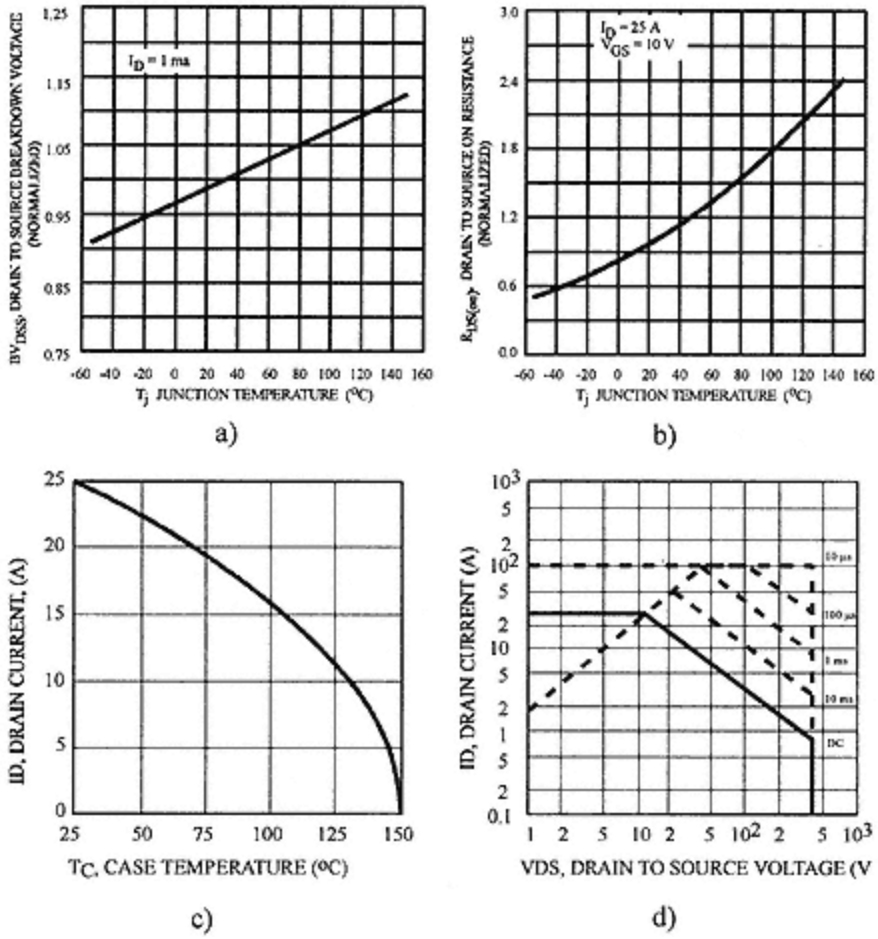


Figure 2-34
Performance characteristics of power MOSFET type IRF360: a) normalized breakdown voltage vs. junction temperature, b) normalized on-resistance vs. junction temperature, c) drain current vs. case temperature, d) maximum safe operating area.

be modified to take new variables into consideration.

A typical power MOSFET die is show in Figure 2-35. Electrical connections to two aluminum bonding pads (gate and source), located on the top surface, are made with Al wire using an ultrasonic wire-bonding technique. Drain – contact metallization on the bottom of the chip is usually chromium-nickel-silver, which is suitable for mounting with soft solder preform or conductive silver bear-

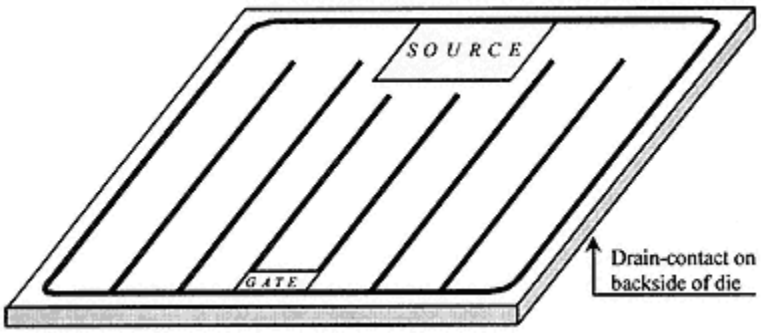


Figure 2-35
Power MOSFET die.

ing epoxy for low power applications. Alternate metallizations for drain contact are available for custom applications.

2.3.3.2—
IGBT

Power insulated gate bipolar transistor (IGBT) is another prominent member of power transistor family. It combines high input impedance and high speed switching characteristics of MOSFET with low saturation voltage and high breakdown voltage of a bipolar transistor. The IGBT model in Figure 2-36 and junction diagram show terminal designation and biasing arrangement for an N-channel transistor Main features include:

• High breakdown voltage

• High current density

• Low saturation voltage

• High input impedance voltage controlled device

• Easy to parallel

• High power switching capability

• High operating temperatures

• Efficient utilization of silicon

• Much faster than bipolar transistors

The construction of IGBT in Figure 2-37 is similar to one of a MOSFET, except that it uses a P^+/N^- substrate instead of N^+/N^- substrate. However the operation of IGBT has more in common with bipolar transistor than with a MOSFET. It is attributed to addition of the P^+ region, which results in conductivity modula-

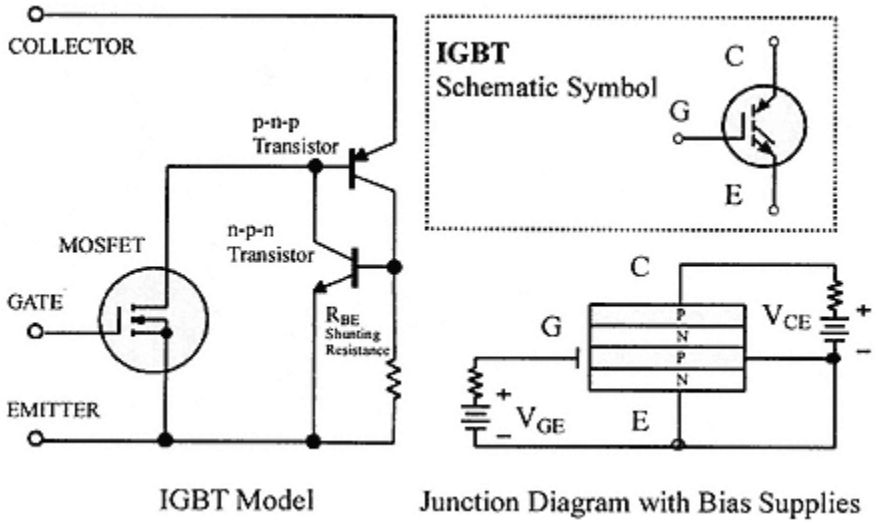


Figure 2-36
Schematic symbol, junction diagram and model for N-channel IGBT.

tion. When a positive voltage is applied to gate of N-channel transistor, the P region directly under the gate is inverted to N^- region, thus creating a path for majority carriers (electrons) flow. This flow forward biases the P^+/N^- junction and allows minority carriers (holes) to be injected from the P^+ substrate into N^- region. That excess of minority and majority carriers modulates the conductivity of high resistance of bulk N^- region and dramatically lowers the on-resistance of IGBT, which for a device of identical ratings is much smaller than on-resistance of MOSFET. That allows the manufacturers to use a smaller die and obtain higher current densities in IGBTs. Die sizes of MOSFET, IGBT, and bipolar transistors rated at 500 V and 15 A are compared in Figure 2-38. The current flow is shown in the left part of Figure 2-37. The correlation of transistor model containing a parasitic thyristor to silicon cross-section is shown on the right side. As the operating temperature goes up, the typical on-saturation voltage $V_{CE(sat)}$ of Figure 2-39a may increase or decrease dependent on the magnitude of collector current.

Gate threshold voltage ($V_{ge(th)}$) is defined as voltage applied between gate and emitter necessary to start the flow of collector current. It declines linearly per Figure 2-39b resulting in increased susceptibility to transient noise at elevated temperatures. Collector–emitter breakdown voltage (BV_{CES}) is determined by reverse breakdown of unterminated collector–base junction of parasitic p-n-p transistor and increases with temperature increase, Figure 2-39c.

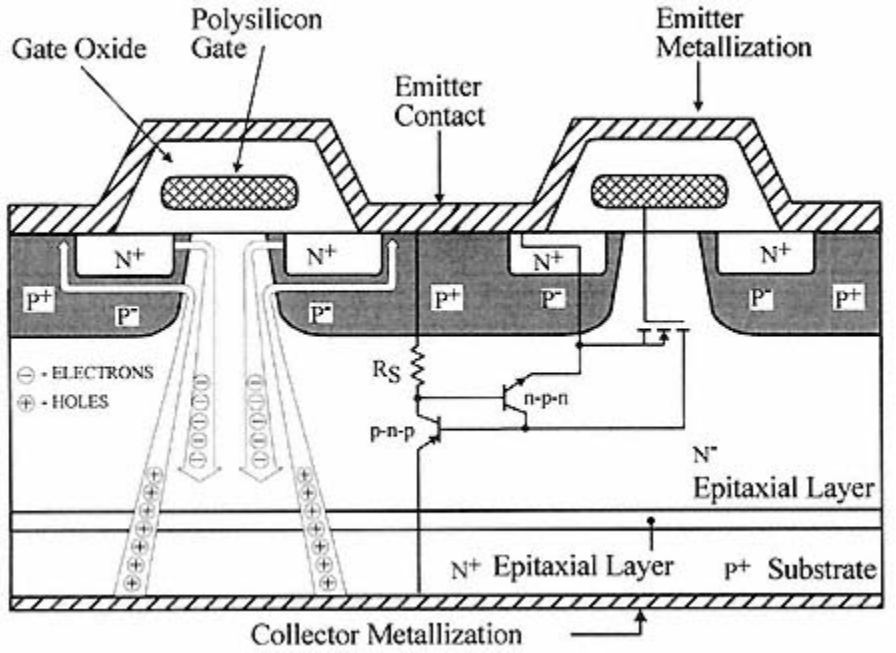


Figure 2-37
Construction of N-channel IGBT.

In contrast with MOSFETs, IGBTs do not have an intrinsic body diode. Depending on operating parameters such as switching frequency, current, and voltage levels it may be an advantage or disadvantage. When switching resistive

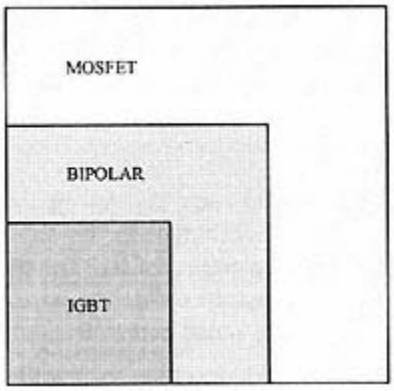


Figure 2-38
Die size comparison of similarly rated transistors, 500 V/15 A.

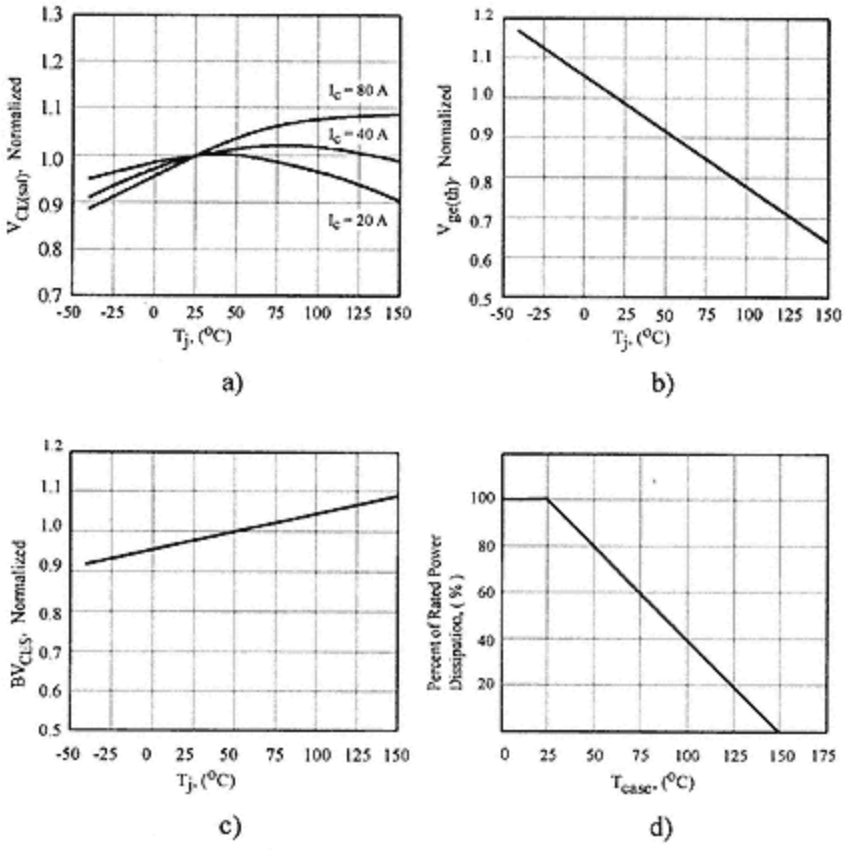


Figure 2-39
Typical performance characteristics for high power IGBT: a) on-saturation voltage $V_{CE(sat)}$ vs. junction temperature T_j, b) gate threshold voltage $V_{ge(th)}$, c) breakdown voltage BV_{CES} vs. junction temperature T_j, d) maximum rated power dissipation vs. case temperature T_{CASE}.

loads, flyback diode is not required and transistor dissipates power only during forward conduction cycle. When switching inductive loads, a flyback diode must be connected between collector and emitter of IGBT to provide current path during phase reversal. During that phase the power is dissipated in the diodes lowering the stress on IGBT. However, added components may increase the overall cost and size of power hybrid.

2.3.4— Integrated Circuit (IC)

Power hybrids offer an advantage of locating drive electronics very close to power transistor gate or base, minimizing parasitic inductance of leads and interconnecting wires. It may also prove critical to lower transient pickup and prevent false triggering, when high level currents are switched at high frequency. Power hybrids have no limitation on type or size of integrated circuits that may be used in them—analog, digital, or smart power. The main consideration should be given during system partitioning phase to circuit requirements, susceptibility to noise transients, availability of IC in die form (some ICs may be built as small hybrids utilizing several die in a package) and target hybrid cost. The majority of ICs are assembled using low power technology. The backside of die may be plain silicon or deposited gold metallization. They are mounted using epoxy and interconnected to circuit conductors with small diameter gold wires. In high volume production gold wires may be replaced by aluminum.

2.3.5— Smart Power Integrated Circuits (SPIC)

Smart power technology adds intelligence to power devices by merging them with logic, control, diagnostic and protection circuitry onto a single monolithic chip. These devices provide controlled driving power for electronic systems. Selection of packages include dual-in-line (DIP) and single-in line (SIP) in a variety of standard and custom configurations. Selection of the package depends on application and rated power dissipation. Military and space systems require devices packaged in metal or ceramic hermetic cases which are capable to withstand severe environmental screening and operation in extended temperature range. Industrial and commercial applications use ICs packaged in plastic leadless chip carriers (PLCC) or SIPs with metal tab extending beyond case outline for attachment to a heatsink.

A combination of single and mixed technologies is used in fabrication process of SPICs:

- Bipolar
- CMOS
- DMOS
- BiMOS
- HDMOS

There is a technological limit to mixed usage of these processes on the same chip. Since none of them offers an ideal solution, a trade-off is used in selection of process to address requirements of a specific application.

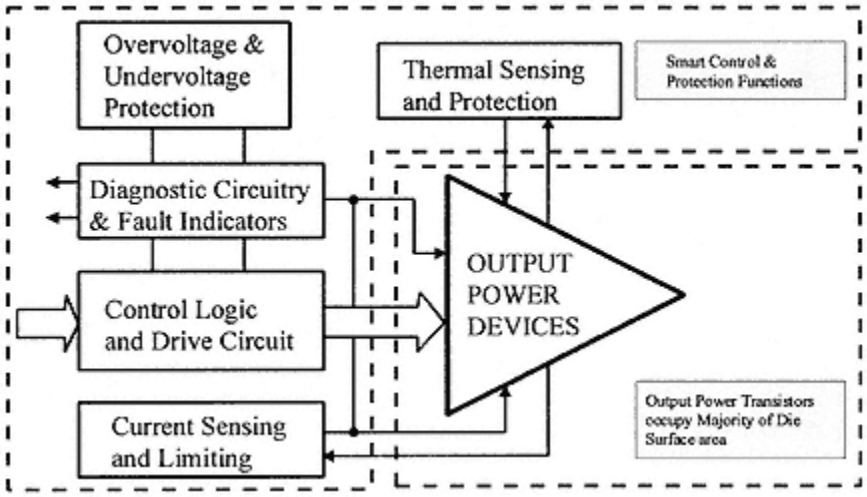


Figure 2-40
Block diagram of a typical smart power integrated circuit.

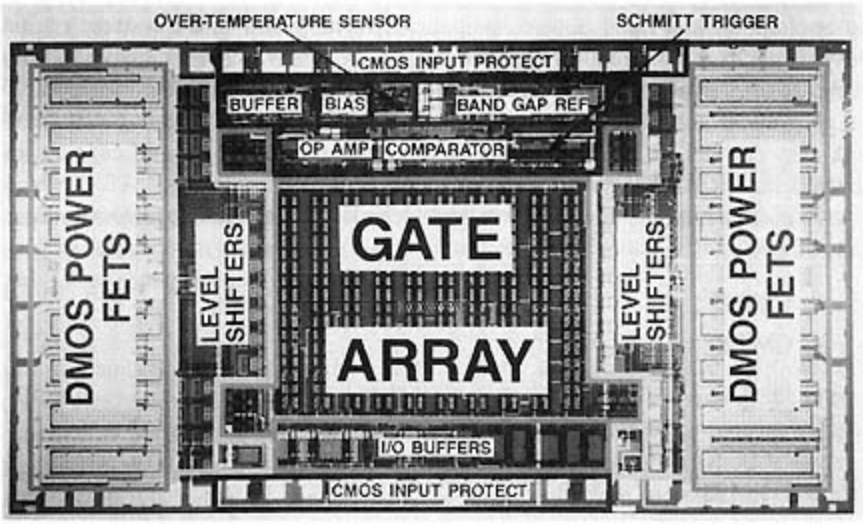


Figure 2-41
Smart power integrated circuit die – CMOS/DMOS/bipolar high voltage array. Photograph courtesy of Micrel, Inc.

Mature semiconductor technology offers devices with wide range of performance characteristics and functionality. The selection varies from a simple power transistor with drive circuitry to a very complex circuit including analog, microprocessor and power functions. Use of SPICs in system designs offers advantages of smaller size and lower cost combined with improved performance with increased reliability. However, SPICs carry more 'smarts' than power — available devices rated at voltages higher than 100 volts are limited to currents less than 1 A; devices with ratings less than 100 volts have current ratings of 10 A or less. Only some very low voltage SPICs offer current ratings higher than 10 A. Limited availability of packages and small die sizes result in relatively high junction-to-case thermal impedance ranging from 1°C/watt to 30°C/watt. The block diagram of Figure 2-40 shows typical features of SPIC.

SPIC technology gained maturity in the early 1980s, when they where introduced. Their application dominion is limited to lower range of power electronics. It is still much more costly to develop a custom SPIC, compared with hybrid or multichip module approach, however a number of standard configurations is growing. A high voltage array die is shown in Figure 2-41. The circuit combines high speed CMOS logic, CMOS analog, bipolar analog, and high voltage DMOS power devices in a single chip.

Contrary to expectations, SPICs did not eliminate the necessity for power hybrids. They enhanced the available selection of functions and increased the feasible integration density. Despite certain degree of functional programmability of SPICs, many applications require custom features, which are not available on chip. They can be implemented by integration of additional discrete circuitry around SPIC in the form of a power hybrid. This extends the advantages offered by SPIC technology into higher power application fields.

2.4— Packages

2.4.1— Introduction

Packages for power hybrid microcircuits exhibit a wide diverseness of properties and are used in commercial, industrial, military, and space applications. Two basic types of hybrid packages are typically used in the industry:

• Hermetic packages for high reliability military and space systems

• Nonhermetic packages for commercial and industrial systems

The hermetic packages are controlled by a variety of military standards and must be designed and built to pass a series of stringent qualification tests. The majority of hermetic packages have standard outlines and constructions. As a rule they are fabricated by an independent package manufacturer. The commercial level pack-

ages are designed to address a specific application and are frequently assembled by the hybrid or module manufacturers. Endless variation of specific application requirements and lack of qualifying standards inevitably lead towards a great multitude of packaging solutions — outlines, constructions, and performance.

2.4.2— Construction

The discussion in this paragraph shall focus primarily on the packages used in manufacturing of high reliability power hybrids.

The packages must provide:

• Environmental protection of the internal circuitry and interconnects

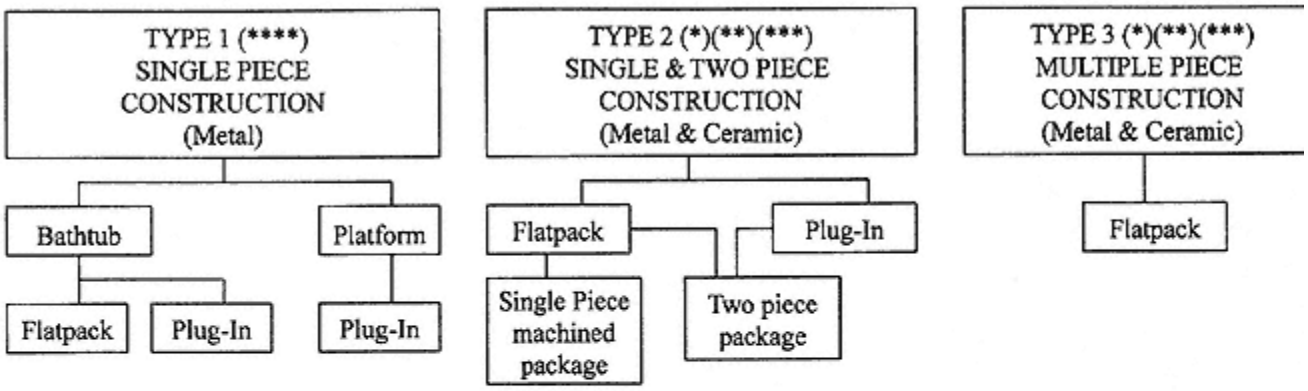
• Mechanical support

• Electrical interconnection of internal circuitry to system components

• Thermal management of internally generated heat

Power package types can be classified according to their physical outline as shown in Figure 2-42. The applications most suitable for the type are identified by the asterisks, which are defined at the bottom of the figure. Each outline type can be implemented in either of two forms: a) flatpack or b) plug-in.

Type 1, bathtub packages are formed by drawing a single sheet of metal into a bathtub shape. When the holes for leads are punched in the bottom of the bathtub, a plug-in configuration is formed. When the holes are punched in the sidewalls, a flatpack configuration is formed. The platform is fabricated from flat formed sheet of metal with holes for leads punched along the perimeter. Figure 2-43 shows Type 1 packages. A flat cover is seam welded to the bathtub case to create a hermetic seal. A dome shaped cover is used to seal the platform case either with solder or projection weld. These packages are usually fabricated from kovar and their usage is limited to hybrid circuits with low power dissipating components. Type 2 construction delineates the traditional and most popular configuration of power packages. They can be implemented in two basic forms as flatpacks or plug-ins. Use of plug-ins is typically limited to applications, where hybrid circuits must be inserted into a socket or soldered directly to the board. The efficiency of heat removal is limited by reduced contact area between the hybrid and the heatsink, which must have cutouts for the I/O leads. The flatpack configuration is designed to address effective removal of heat generated by high power dissipating components in the hybrid, and provides the maximum usable heat transfer contact area with the heatsink. Usually these packages are equipped with heavy leads for high currents. Figure 2-44 displays several popular Type 2 flatpack packages implemented in two piece construction. A single piece package is assembled using piece parts demonstrated in Figure 2-45a. The body is



APPLICATIONS:

(*) High power dissipation

(**) High current

(***) High voltage

(****) Low-to-medium power hybrids

Figure 2-42
Power packages, classification.

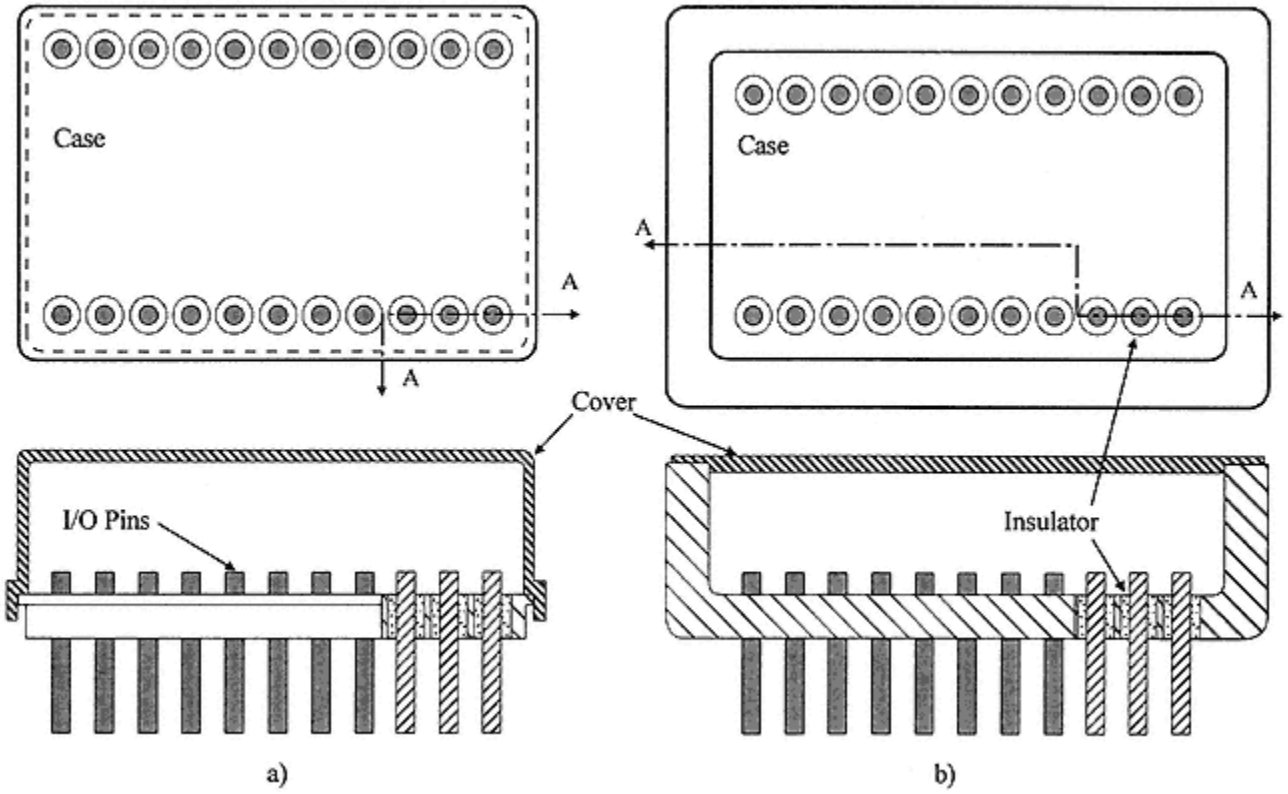


Figure 2-43
Type 1 packages: a) platform package with domed cover, b) bathtub plug-in package with flat cover.

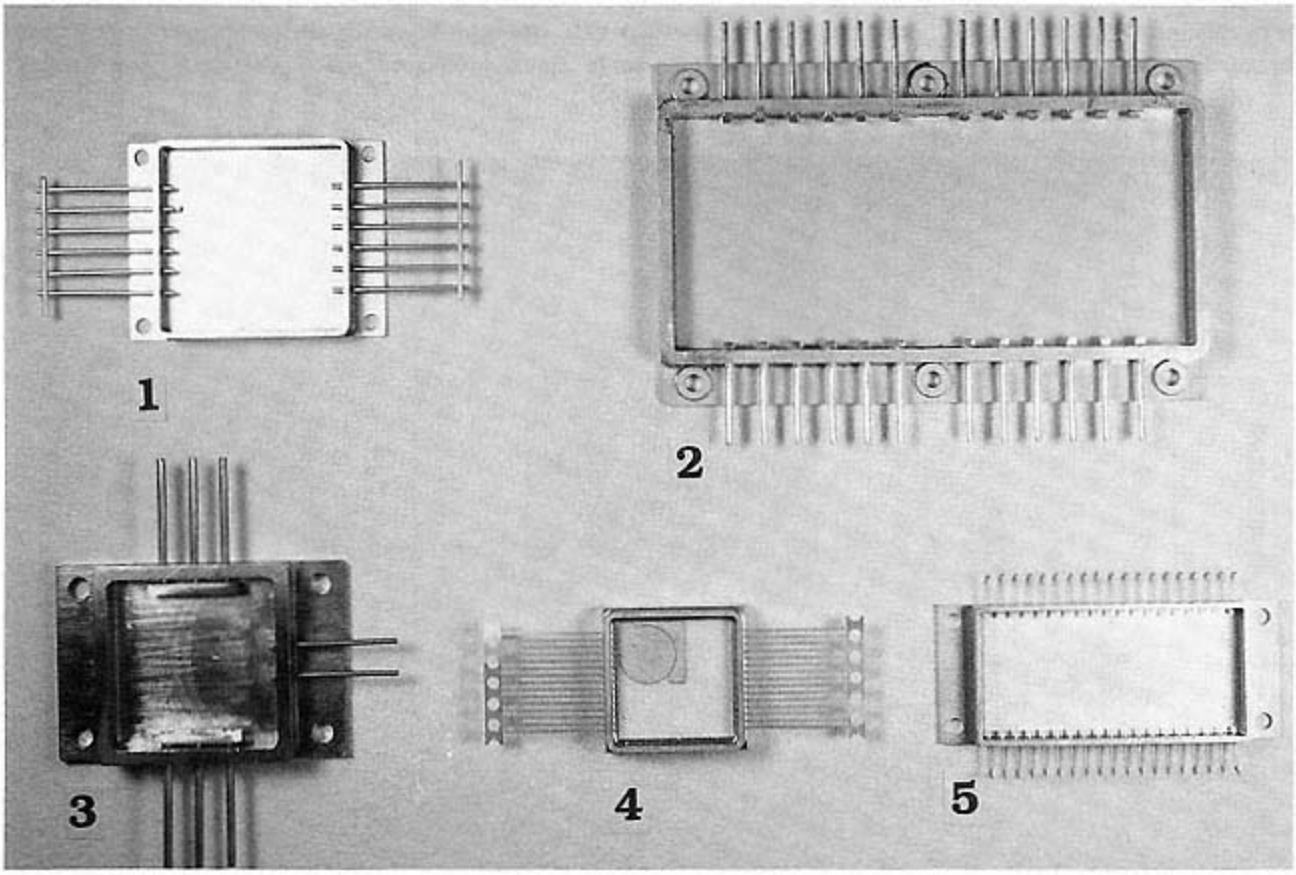


Figure 2-44
Type 2 flatpack two piece packages.

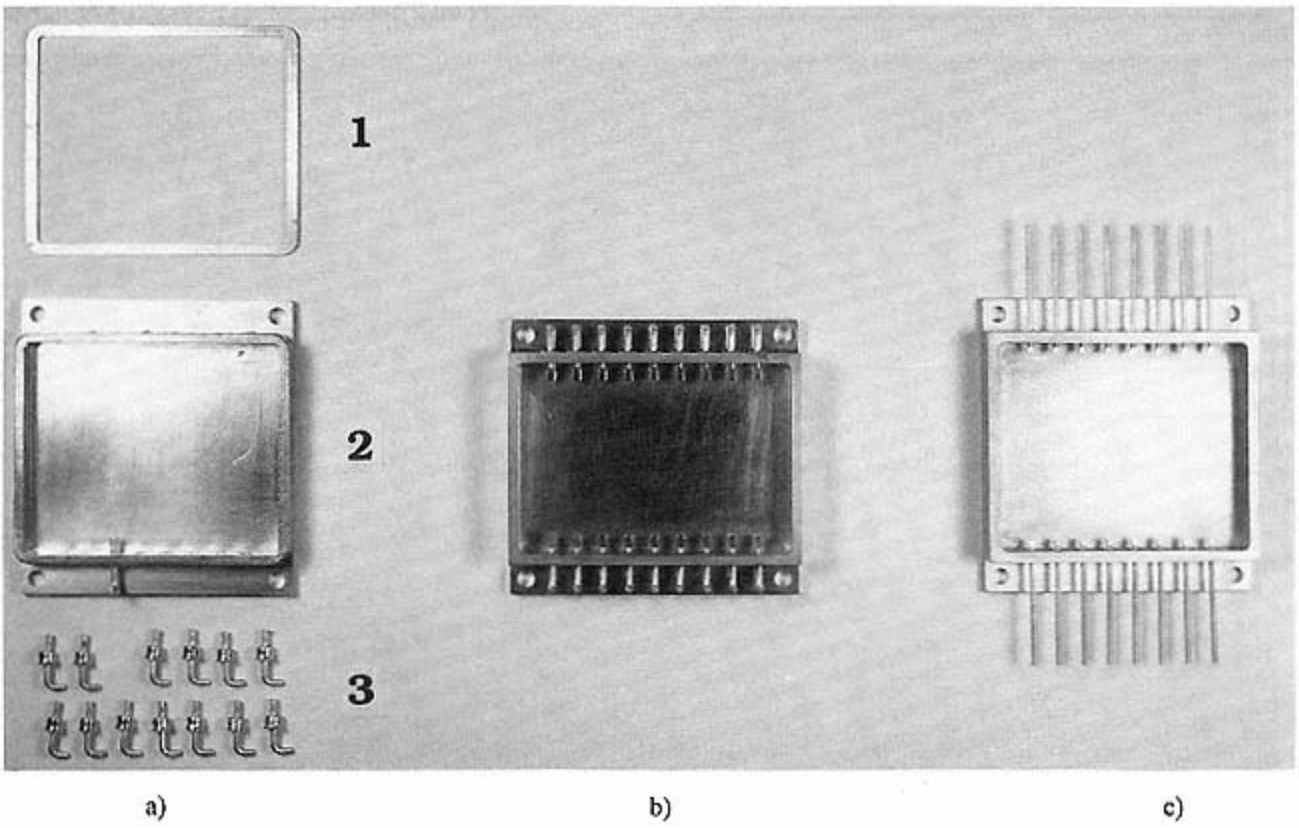


Figure 2-45
Machined copper package assembly: a) sealing ring – 1, machined body – 2, terminals with compression seal – 3, b) assembled package using terminals with compression seal, c) assembled package with terminals using ceramic insulators.

Table 2-7 Power packages, construction details

Reference	Construction	Bottom	Side walls	Insulators	Pins
Fig. 2-44 (1)	Two piece	Molybdenum	Kovar	Matched glass	Alloy #52
Fig. 2-44 (2)	Two piece	Molybdenum	Kovar	Matched glass	Copper butt welded to kovar
Fig. 2-44 (3)	Two piece	Glidcop	Stainless steel	Compression glass	Alloy #52 copper cored
Fig. 2-44 (4)	Two piece	BeO	Kovar	Matched glass	Alloy #52
Fig. 2-44 (5)	Two piece	Molybdenum	Kovar	Matched glass	Alloy #52
Fig. 2-45 (b)	Single piece	Copper	Copper	Compression glass	Alloy #52
Fig. 2-45 (c)	Single piece	Copper	Copper	Ceramic	Alloy #52 copper cored

machined from a solid piece of copper. Holes for terminals are punched in the body walls. Each terminal consists of a pin sealed with compression glass in a metallic eyelet. Each terminal is brazed to the body using a solder preform. Finally a weldable sealing ring is brazed to the upper surface of the wall. An assembled package is shown in detail b). A package with a different terminal construction is shown in detail c). Here the pin is brazed to a ceramic ferrule metallized on two cylindrical surfaces, internal and external. The assembled terminal is then brazed in the holes punched in the package walls. A brief description of construction details of packages shown in Figures 2-44 and 2-45b and c) is summarized in Table 2-7. Type 3 packages conclude the selection of hermetic enclosures for power hybrids. They offer light weight, high efficiency of heat transfer and are most suitable for high voltage applications. Such a package is shown in Figure 2-46a. The strips shown in detail b) are metallized on the sides and have

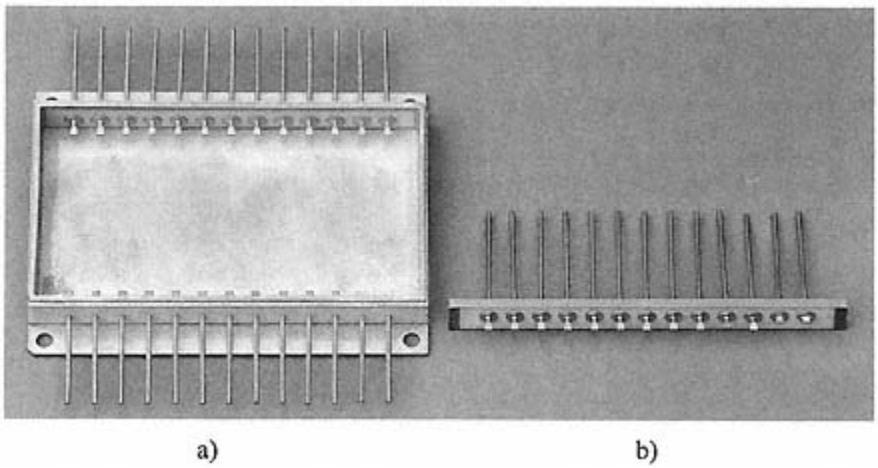


Figure 2-46
Ceramic package. Courtesy of Alberox Corporation.

pins with high electrical conductivity brazed to them. These ceramic strips are in turn brazed to the walls and the case bottom. A weldable ring is brazed to the upper perimeter of the walls to allow hermetic sealing of the package.

A large selection of materials and their combination is available to create a package to meet numerous application requirements. The summary of materials for package components and their typical combinations is shown in Figure 2-47.

2.4.3— Lead Feedthrough

The three methods of pin insulation, which were mentioned in Table 2-7 are described below.

1— Matched Glass-to-metal Seal

This method is used when the thermal coefficients of expansion of the pin, wall, and glass materials closely match. It applies mostly to kovar sidewalls with kovar pins. An oxide is intentionally grown on the surface of metal components prior to the plating. The pins are inserted into glass beads and placed into holes punched in the package body. The entire assembly is placed into a carbon boat and sent through a furnace with carefully adjusted temperature profile. When the glass melts a molecular bonding occurs between the molten glass and the oxide. After mild etching or cleaning of the surface, the package and leads are plated. To assist in plating a tie bar may be welded to the leads as shown in Figure 2-44(1). A side view of matched glass-to-metal seal is illustrated in Figure 2-48a. The weakest link in this assembly is the glass meniscus. It is very thin and brittle, and has a tendency to crack or chip-out after environmental stresses, lead forming or operator handling during manufacturing. Since the package is plated after the

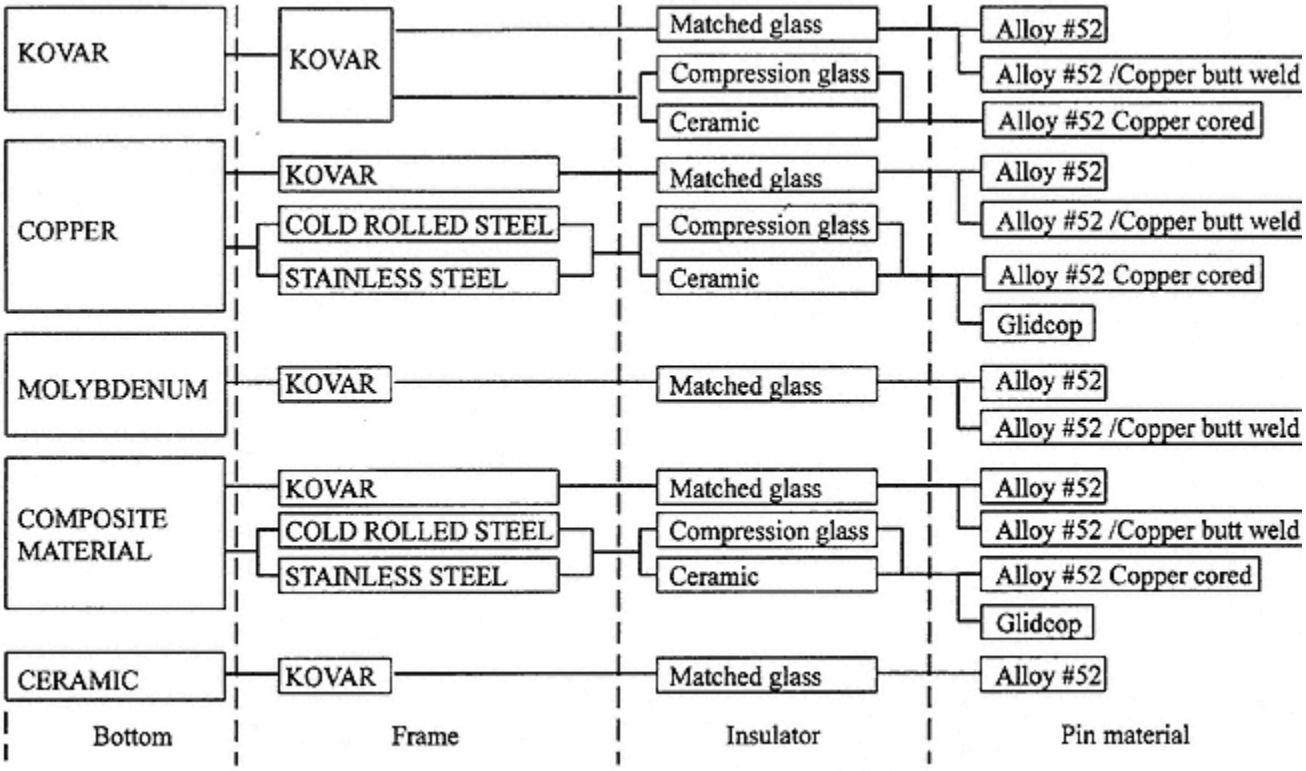


Figure 2-47
Typical combination of materials used in the composition of power packages.

glass-to-metal seal is completed, only the exposed part of the pin is plated. When a chip-out occurs, the base metal of the pin, typically alloy #52 is exposed. It is only a matter of time until this unplated portion of the pin corrodes. This occurrence led to establishment of a very detailed and stringent criteria for visual inspection of packages intended for use in high reliability applications.

2—
Compression Seal

A side view of compression glass-to-metal seal is illustrated in Figure 2-48b. This method utilizes intentional mismatch of the thermal expansion rates of materials. The outer material has the highest rate of thermal expansion, the glass has a medium rate, and the pin has the lowest rate. Prior to assembly the eyelet and the pin are plated with nickel. Then the components are assembled and fired in the furnace. During subsequent cooling the outer component shrinks onto the glass, which in turn shrinks onto the metal pin. This combination creates enormous compression forces directed inward, which result in hermetic seal without a metallurgical bonding. This configuration is also haunted by glass cracking and loss of hermeticity.

3—
Ceramic Seal

This seal is used in the Type 2 and Type 3 packages. It is accomplished in two separate ways:

• By using a ceramic feedthrough

• By using a ceramic strip

When a ceramic feedthrough is used, the both cylindrical surfaces of a ceramic doughnut are plated. Then the pin is brazed inside the feedthrough to yield a terminal shown in Figure 2-49a. During the final package assembly phase, the terminals are brazed inside the punched holes. Both brazing operations may take place at the same time, dependent on the braze materials used. This construction utilizes ceramic, which is stronger than glass and has no meniscus, therefore significantly lowering the manufacturing yield losses due to chip-outs and cracks. However, fabrication of packages with ceramic feedthroughs is much more labor intensive, which eventually raises the cost of the package.

Another design using ceramic for pin insulation is shown in Figure 2-49b. Brazed ceramic strip-to-metal seal is performed in four steps. First a high electrical conductivity pin is brazed to a kovar seal washer. Second, the ceramic substrate strip is metallized and plated with nickel around the holes and on the perimeter. Third, the pin with seal washer is brazed to the metallized ceramic. Finally the assembly is plated. The braze surface can be located on either the inside or outside of the package cavity. During final assembly, the entire strip is brazed to the package bottom and adjacent walls. Then a weldable ring is brazed

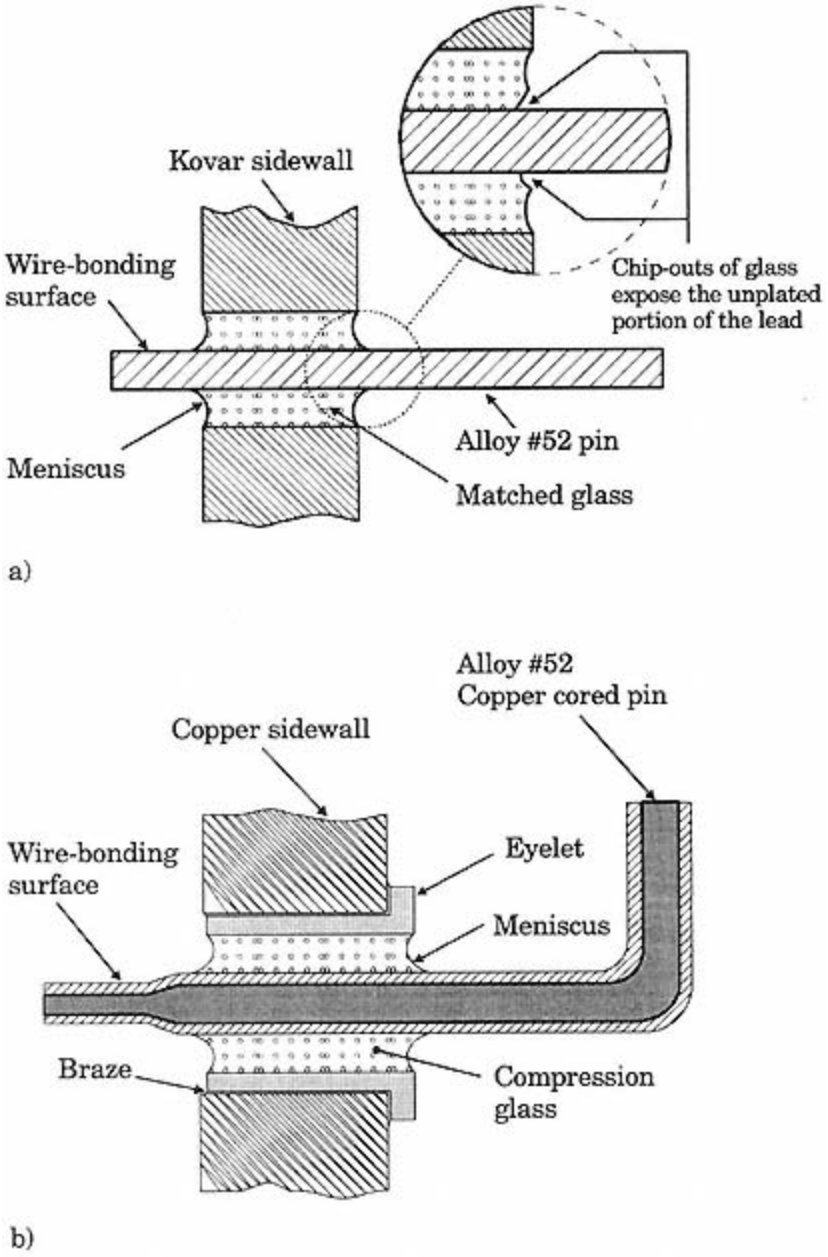


Figure 2-48
Pin sealing with glass in the sidewall: a) matched glass-to-metal seal, b) compression glass-to-metal seal terminal assembly.

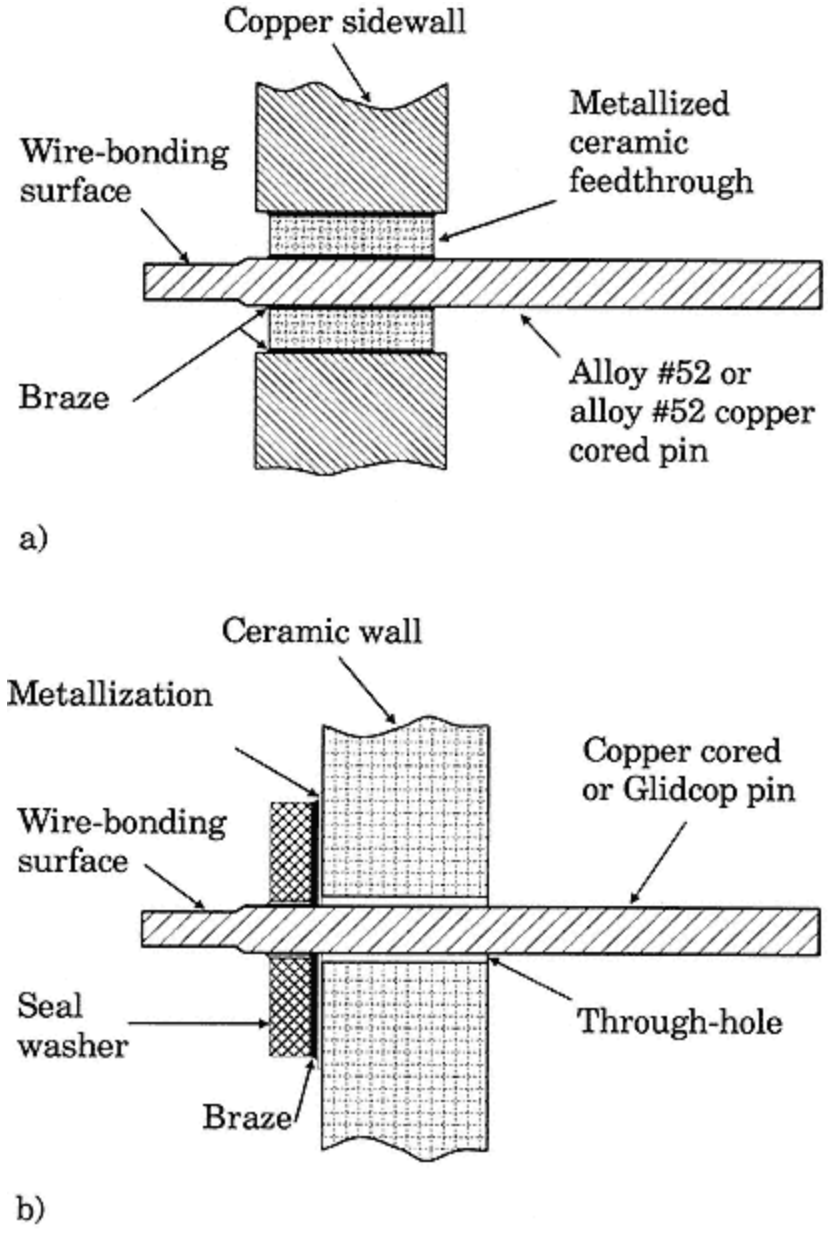


Figure 2-49
Pin sealing with ceramic in: a) ceramic feedthrough assembly,
b) pin assembly in a ceramic strip.

on the top to allow hermetic seal. This construction is particularly attractive for high current and high voltage applications, considering that it utilized hardened copper for I/O leads, which are located at a greater distance from the metal enclosure, than in the case of all metal packages.

2.4.4— Covers

The cover or lid is intended to hermetically seal the top perimeter of the package and may be fabricated in a variety of shapes, and from different materials. Typical covers are shown in Figure 2-50:

a) Flat cover. It can be welded or soldered to a bathtub or flatpack case.

b) Stepped cover is etched along the edge from a single sheet of metal. It is welded to the case by a parallel seam welder. During this operation no true

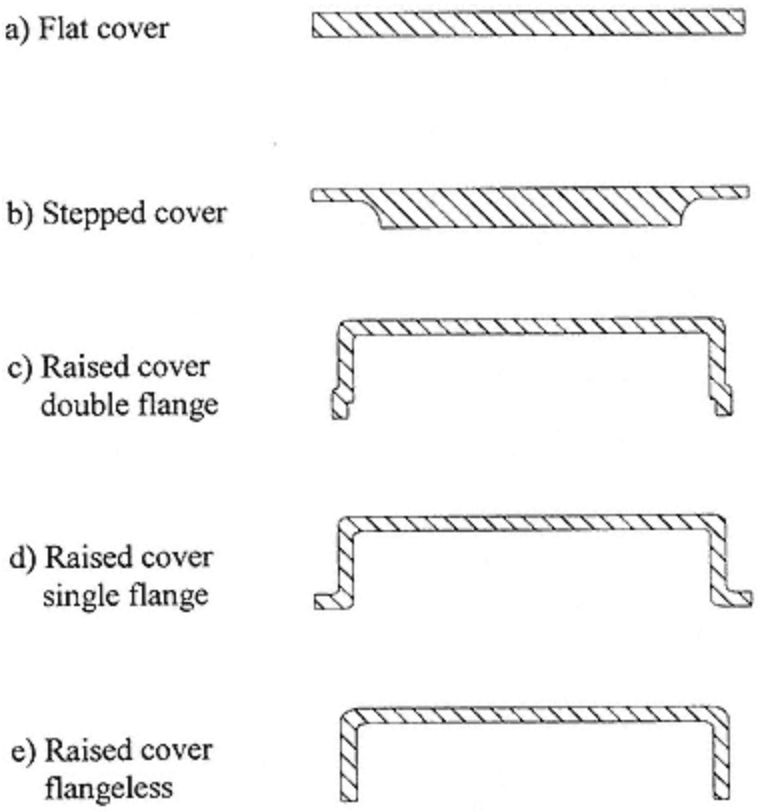


Figure 2-50
Typical covers used in hermetic sealing of hybrid packages.

welding of base materials occurs, despite what the name of this process may imply. The welding electrodes are in constant contact with the lid and move continuously, while the power is rapidly pulsed. A series of overlapping spot welds are created on opposite sides of the lid. Only melting of plating occurs and some melting is evident on the cover at the point of electrode contact, but no melting of the base is observed.

c) Raised cover double flange is used to seal platform cases using solder.

d) Raised cover single flange is used to resistance weld platform cases.

e) Raised cover flangeless can be used with solder or epoxy.

Material used for cover fabrication has to match the thermal expansion of the sealing surface of the case. The covers used to seal kovar packages and packages with kovar seal ring are made from kovar. Copper packages have a brazed-on stainless seal ring, requiring a matching stainless steel cover.

Plating of covers is necessary to prevent corrosion. Typical materials used for plating are nickel and gold which are deposited on the surface using electro-chemical reaction.

References

1. Tummala, R. R. and Rymaszewski, E. J., eds., *Microelectronics Packaging Handbook*, Van Nostrand Reinhold, New York, 1989.

2. Avallone, E. A., and Baumeister, T., III, *Marks' Standard Handbook for Mechanical Engineers*, 9th ed, McGraw-Hill, New York, 1987.

3. Harper, C. A., ed., *Handbook of Components for Electronics*, McGraw-Hill, New York, 1977.

4. *Linear Ferrite Magnetic Materials Design Manual*, Ferroxcube Division of Amperex Electronic Corp., Saugerties, New York

5. Kit Sum, K., *Switch Mode Power Conversion: Basic Theory and Design*, Marcel Dekker, New York, 1984.

6. Hnatek, E. R., *Design of Solid-State Power Supplies*, Van Nostrand Reinhold, New York, 1981 pp. 147–190.

7. Martin, W. A., "New Developments in Power Ferrites," Powertechnics Magazine, February 1990, pp. 18–21.

8. Gregory, V., "Building Magnetics With Flexible Circuits," Powertechnics Magazine, February 1989, pp. 16–22.

9. Hower, P. L. and Weaver, C. E., "Schottky Rectifiers for Low Voltage Outputs," IEEE Applied Power Electronics Conference Proceedings, April

1986, pp. 151–160.

10. Grove, A. S., *Physics and Technology of Semiconductor Devices*, Wiley, New York, 1967.

11. Ruska, W. S., *Microelectronic Processing–An Introduction to the Manufacture of Integrated Circuits*, McGraw-Hill, New York, 1987.

12. Wodarczyk, P. J. and Wojslawowicz, J. E., "Intelligent Discretes: A New Era in Power Devices," Eighteenth International Intelligent Motion Conference Proceedings, 1990, pp73–84.

13. Grant, D. and Pelly, B., "New High-Voltage Bridge Driver Simplifies PWM Inverter Design," Proceedings of Nineteenth International Power Conversion Conference, 1989, pp. 392–400.

14. Rippel, W. E., "MCT/FET Composite Switch Achieves High Silicon Utilization and High Switching Performance," Proceedings of Nineteenth International Power Conversion Conference, 1989, pp. 220–237.

15. Gauen, K., "Understanding The MOSFET's Input Characteristics," Proceedings of The Power Electronics Show and Conference, April 27, 1987, pp. 127–131.

16. Temple, V. A. K., "MCTs for High Frequency Applications," Technical Papers of Fourth International High Frequency Power Conversion Conference, 1989, pp. 62–80.

17. Kinzer, D. and Sheridan, G., "Power MOSFET Performance Continues to Improve," Electronic Products, September 1993, pp.49–63

18. Daly, T., "New Technology Makes Power MOSFETs Faster, More Efficient," PCIM, January 1988, pp. 14–18.

19. Clark, O. M., "Transient Voltage Suppressor Types and Applications," PCIM, November 1990, pp. 19–26.

20. Zommer, N., "Second Generation IGBTs," Powertechnics Magazine, September 1990, pp. 31–36.

21. Kokini, K., "Thermal Shock Testing of Glass-to Metal Seals in Microelectronics: Effect of Package Lid," IEPS proceedings, October 1984, pp. 637–651.

22. Anderson, N. C. and Weinshanker, S., "Brazing of Aluminum Nitride", The International Journal of Hybrid Microelectronics, Vol. 14, No. 4, December 1991 pp. 121–128.

23. Anderson, N. C., "Improved Technology for Construction of Hermetic

Power Hybrid Packages," Hybrid Circuit Technology, June 1991, pp. 21–23.

24. Dickinson, D. and More, D., "Hermeticity Improves Package Reliability," Electronic Packaging and Production, April 1990, pp. 61–63.

25. Sachs, R., "Considerations in the Design and Use of Hermetic Packages," Hybrid Circuit Technology, May 1988, pp. 9–13.

26. Krum, A., "Designing Power Hybrid Packages," Hybrid Circuit Technology, March 1989, pp. 17–24.

27. Severns, R., Blanchard, R., Cogan, A. and Fortier, T., "Special Features of Power MOSFETs in High-Frequency Switching Circuits," HFPC Proceedings, May 1986, pp. 133–148.

3—
Materials

3.1—
Introduction

Creation of power hybrid microcircuits involves a large variety of materials and technological processes. It is essential to clearly understand their properties and compatibility in order to use them effectively and reliably. The construction of a typical power hybrid in Figure 3-1 demonstrates relative location of components and materials assembled in a single case. It is related to the subjects discussed further and should help to understand how materials are used in the power hybrids.

3.2—
Substrates

Ceramic substrates are the most basic component of hybrid microcircuit technology. They play a multitude of very important roles in construction of power hybrids, and have to render:

• Electrical isolation between components and case. The critical characteristics — low leakage and high breakdown voltage.

• Compatibility with hybrid components, adhesives, and solders. The critical characteristic — coefficient of thermal expansion.

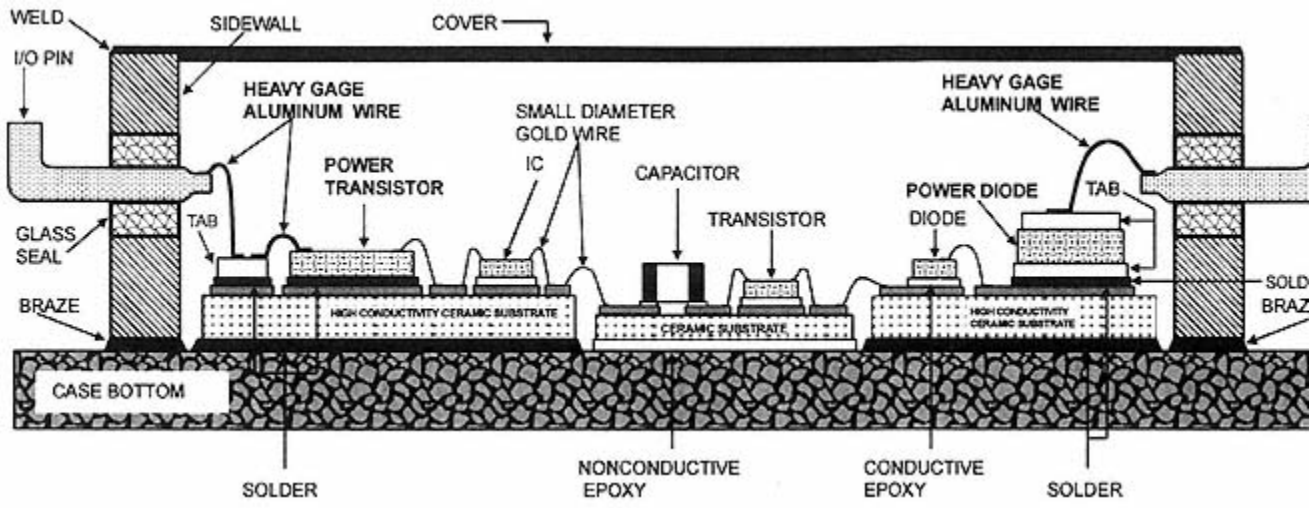


Figure 3-1
Construction of a typical power hybrid.

• High mechanical strength allowing to withstand stress and handling. The critical characteristics — tensile and compressive strength.

• Ability to withstand high temperatures of thick-film manufacturing processes without degradation and change in properties.

• Insensitivity to exposure to chemicals and solvents used in thick-film manufacturing processes.

• Surface quality and stability. Critical characteristics — camber, surface flatness and finish.

• High thermal conductivity to provide efficient heat removal from power dissipating components. Critical characteristic — thermal conductivity over operating temperature range.

Many ceramic materials are available for use in manufacturing of power hybrid circuits. They vary from commonplace to exotic, offering designers the versatility in selection of mechanical and electrical properties. Physical properties of ceramic substrate materials frequently used in power hybrids are listed in Table 3-1. None of the available substrate materials provide designers with an ideal solution. Alumina (Al_2O_3) has been a substrate of choice for use in hybrid microcircuits for decades. Most thick-film materials were developed and characterized for use on alumina substrates, making them a common material available at low cost for most general applications. However alumina has poor thermal conductivity, when compared with aluminum nitride (AIN) or beryllia (BeO), and is much less suitable for high power applications. The disadvantages of beryllia: higher cost and toxicity of its fumes and powder, are traded for availability of wide selection of compatible thick film materials and superior thermal conductivity. Aluminum nitride is a new ceramic material that offers certain advantages when compared with both Al_2O_3 and BeO. It is less costly than BeO, has a thermal conductivity much higher than alumina, and matches the thermal expansion of silicon better than both. It is nontoxic and is compatible with selected thick-film pastes. Comparison of variations of thermal conductivity and thermal expansion with temperature, shown in Figure 3-2, helps in selection of substrate material for a specific application. The shaded area defines temperature range relevant to power hybrid applications. For example, thermal conductivity of BeO in Figure 3-2b rapidly decreases approaching AlN at temperatures above 400°C. Despite that, at temperatures below 200°C BeO is an obvious choice when thermal conductivity is a primary concern. On the other hand, if close matching of thermal expansion with silicon die is more critical, then AlN is a better choice. And finally, when power dissipation level is relatively low and the cost is a driving factor, the alumina substrate becomes a prime selection. The thermal expansion and thermal conductivity characteristics of popular materials

Table 3-1 Physical properties of selected substrate materials (values at 25°C unless otherwise specified)

Property	99.5% Al_2O_3	96.0% Al_2O_3	99.5% BeO	AlN
Dielectric constant @ 1 Mhz, 25°C	9.7 – 10.5	8.9 – 10.2	6.5 – 7.0	8.0 – 9.2
Dielectric strength	15 – 36	14 – 24	10 – 43	14 – 27
Dissipation factor	0.01	0.03 – 0.1	0.02 – 0.04	0.03 – 0.1
Volume resistivity	$>10^{14}$	$>10^{14}$	$>10^{14}$	$>10^{14}$
Flexural strength	420 – 500	200 – 400	170 – 270	275 – 500
Specific gravity	3.86 – 3.92	3.70 – 3.75	2.85 – 2.92	3.25 – 3.30
Thermal coefficient of expansion (TCE) 25 – 300°C	6.6	6.4 – 7.2	7.2 – 8.0	3.8 – 4.4
Thermal conductivity	29 – 37	20 – 26	260 – 290	110 – 260
Maximum use temperature	1600	1500	1700	1800

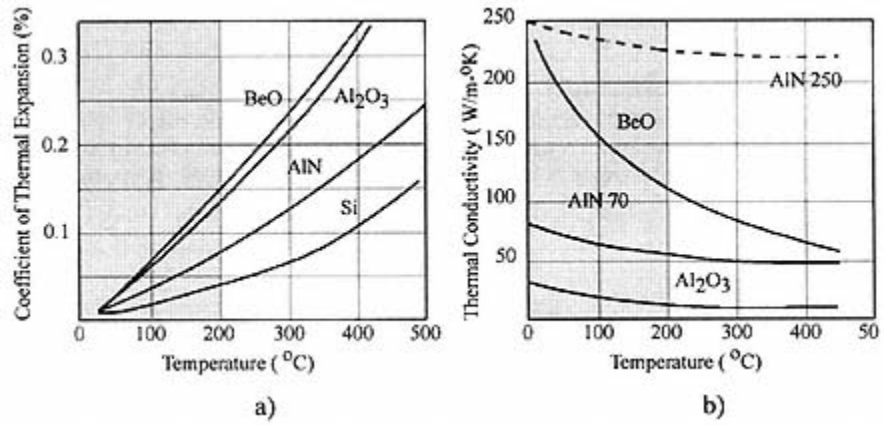


Figure 3-2
Ceramic substrate materials, performance variation with temperature:
a) CTE vs. temperature, b) thermal conductivity vs. temperature.

used in power hybrids are mapped in Figure 3-3. The shaded areas outline domains occupied by materials with similar characteristics. Several combinations of material interface can be found in power hybrid:

1. Silicon die attached to ceramic substrate.

• Selection of material is determined by power dissipation in the die. TCE of all substrates matches silicon reasonably close. If TCE is the primary concern, AlN appears to be the best choice.

2. Silicon die attached to a metal heatsink tab.

• Use of a metal heat spreader with high thermal conductivity helps to decrease thermal resistance of assembly.

3. Metal heatsink tab attached to a ceramic substrate.

• Typically attached with solder for efficient heat transfer. Molybdenum (Mo in Figure 3-3) tabs are predominantly used due to a very close match of TCE with ceramic substrate and silicon die.

4. Ceramic substrate attached to the bottom of metal case.

• If material with low TCE is used in the package construction (kovar, molybdenum, copper-tungsten composite, etc.), then the substrate mounted in the case shall be subjected to a low thermal stress.

• Careful consideration to substrate size and adhesive type must be given when material with high TCE is used in package construction (cold rolled steel, stainless steel, copper, etc.). Very tight process controls shall be required during manufacturing of the hybrid.

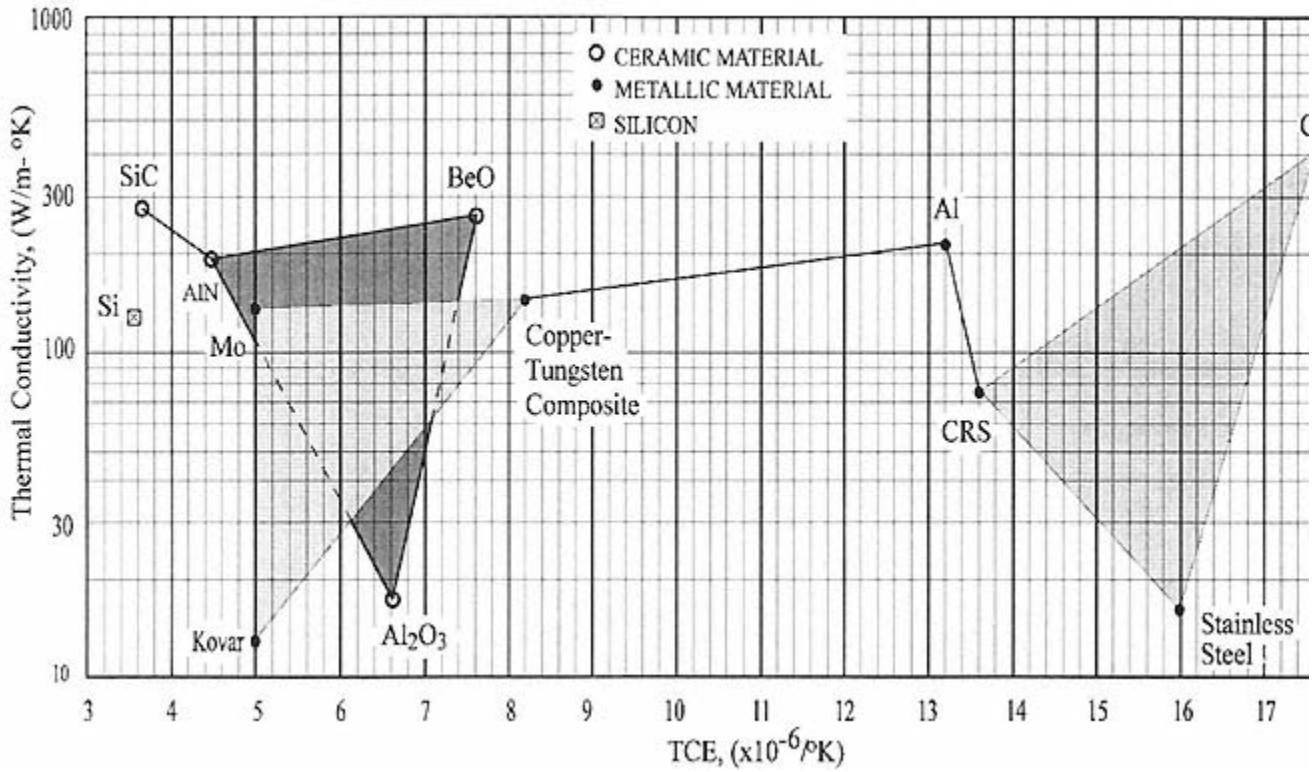


Figure 3-3
Thermal properties of materials used in power hybrids.

A large selection of thick-film materials was developed for use with alumina, beryllia, and to a lesser degree AlN ceramics. They were thoroughly characterized and are reliably used in power hybrids. Physical structure of conductors produced by the thick-film process presents serious limitation to their ability to pass continuous currents in excess of several amperes. Small cross-section and relatively high resistivity lead to large voltage drops and power loss. To prevent this solid metal tabs are used to effectively conduct the heavy currents. Tabs can be made from a variety of materials, such as:

• Copper

• Molybdenum

• Kovar

• Composites with high electrical conductivity

Tabs are usually overplated with nickel and sometimes gold flash to prevent corrosion and enhance solderability. Semiconductor chips are either soldered to the tabs or wire-bonded with large diameter aluminum wires, as shown in Figure 3-4. This technique is useful when a limited number of tabs is required.

Ceramic substrates have to provide an efficient path for heat transfer from power dissipating components to external heatsink. The electrical interconnections must be capable of conducting high currents with low loss. Use of epoxy adhesives is restricted to applications with low power dissipation. With increase of power levels, the semiconductor components and tabs are attached to the sub-

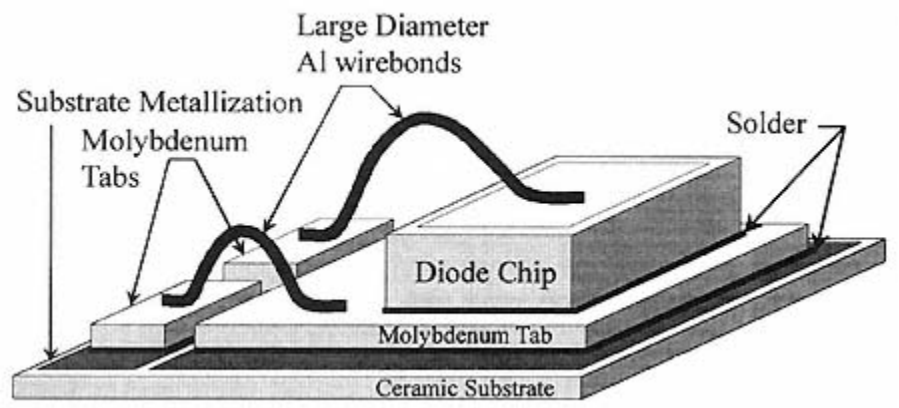


Figure 3-4
Use of molytabs for die mount and heavy current conduction.

strate with solder, and in turn, the substrate is soldered to the case bottom.

The substrate has to be metallized on one or both sides to provide a solderable interface. This can be achieved by use of either of the following technologies:

• Thick-film metallization

• Refractory metallization

• Direct bond copper metallization

• Thermal clad

Direct bond copper (DBC) metallization is unique in a sense that it is offering heat spreading and high current carrying capability at the same time. The thickness of copper foil can reach 0.020" and is very effective in reducing junction-to-case thermal resistance. Solid copper foil can be plated, wire-bonded, and soldered using a wide selection of materials. However DBC is not compatible with thick-film technology and special design techniques must be used to add resistive or multilayer patterns. One way to accomplish this is to use a thick-film subassembly attached next to DBC substrate or mounted on top of it.

Thick-film metallization is produced by screen print-dry-fire process — same as the one used to manufacture thick-film resistors, see Figure 2-1. Available materials include:

• Gold (Au) compositions — low resistivity conductors used where conductive and non-conductive epoxy or direct eutectic die bonding is required. Excellent thermocompression and thermosonic wire bonding. Solderable with gold and indium containing solders.

• Platinum/Glod (PtAu) and palladium/gold (PdAu) compositions — have high leach resistance and are used in high reliability applications, when the soldering with lead–tin containing solders is required. Exhibit high resistivity and should not be used to conduct high currents.

• Palladium/silver (PdAg) and platinum/silver (PtAg) compositions — general purpose low cost conductor materials used for soldering with lead–tin–silver containing solders. Some compositions have high resistivity.

• Copper (Cu) — low cost general purpose conductors solderable with lead–tin containing solders. Exhibit low resistivity and must be fired in a nitrogen atmosphere.

Substrate metallization may be selected using the summary of Table 3-2 as a guide. Typical characteristics of thick-film conductors are shown in Table 3-3.

To produce refractory metallization, moly-manganese, or moly-tungsten the paste is screen printed and fired at high temperature (>1000°C). Subsequently it

Table 3-2 Ceramic substrate metallization techniques

Technique/Substrate type	Thick-film	Refractory metallization	Direct bond copper	Thermal clad
Alumina (Al_2O_3)	Excellent compatibility, wide selection of materials	Excellent compatibility, good adhesion, wirebondability, solderability	Excellent compatibility, good adhesion, wirebondability, solderability	NA
Beryllia (BeO)	Excellent compatibility, wide selection of materials	Excellent compatibility, good adhesion wirebondability solderability	Excellent compatibility, good adhesion, wirebondability, solderability	NA
Aluminum nitride (AlN)	Good compatibility, limited selection	Good compatibility, fair adhesion, wirebondability, solderability	Good compatibility, fair adhesion, wirebondability, solderability	NA
Thermal clad	NA	NA	NA	Intended for low cost commercial applications. Al & Cu used as clad or base plate materials

is overplated with nickel and gold. This metallization is known for excellent adhesion to the ceramic and good bondability with gold and aluminum wires. It has a very good leach resistance to lead–tin containing solders and allows repeated rework.

Direct bond copper metallization is accomplished by eutectically attaching copper foil to the surface of a ceramic substrate. The originally developed process required presence of oxygen in the ceramic. It was necessary to produce the eutectic, which formed between copper and oxygen at 1060°C. During this proce a sheet of copper is placed onto a substrate and preheated to temperature above eutectic until a thin layer c CuO liquid is formed. After cooling the substrate and the copper foil are bonded together by the solidified eutectic phase. AlN is a nitride and not an oxide. Therefore the process of copper bonding had to be modified. It was accomplished by bonding a thin layer of aluminum oxide to the surface of AlN substrate and then repeating the original process. Typical

Table 3-3 Typical performance characteristics of the thick-film conductors

	Ag	PdAg	PtAg	Au	PtAu	Cu
Electrical resistivity (mΩ/□)	< 2	10–45	2–60	2–5	60–100	1.3–2.2
Fired thickness (mils)	0.6–0.7	0.4–0.8	0.5-0.8	0.7–0.8	0.6–0.8	0.5–0.6
Resistance to leaching	good	good	good	poor	good	very good
Bondability:						
Au wire	good	good	good	excellent	excellent	poor
Al wire	poor	fair	fair	fair	fair	good

thickness of substrates varies from 0.015" to 0.040" with copper foil 0.005" to 0.020" thick. Copper can b plated with nickel and overplated with gold to allow use of gold wire-bonding. To create a conductor patte the copper sheet must be etched, just like a printed circuit board. The copper sheet can be left overhanging the substrate boundaries to create a leadframe for connection to external components in the system, see Figure 3-5. Thermal clad material can be used as a replacement for the ceramic substrate in low cost commercial applications. A thin-film of ceramic-filled polymer (0.0027" thick) is deposited on a metal bas which can be made of aluminum, copper, and cold rolled steel. Base thickness may vary from 0.062" to 0.093". A film of solid copper (the circuit layer) 0.014" — 0.042" thick is laminated to the dielectric.

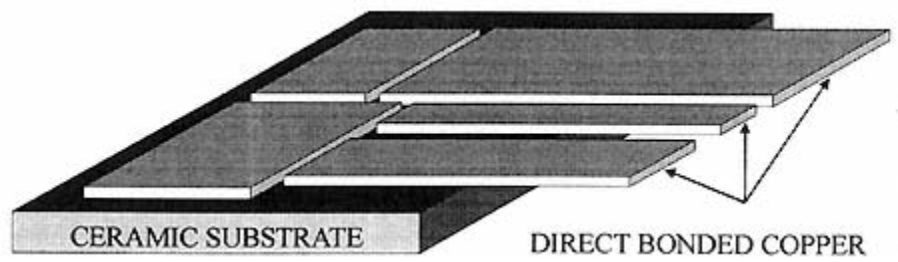


Figure 3-5
Direct bond copper metallization on a ceramic substrate.

This layer can be etched like a regular printed wiring board to create a conductor pattern. Thermal clad material may be stamped, machined, and formed to custom configurations. Overall thermal characteristics provide good heat transfer from the mounted chips to the heatsink. To allow wire-bonding to conductors the site has to be plated with nickel for Al and gold overplated for Au wires. Standard adhesives and solders are used for the component attachment to the circuit layer.

3.3—
Interconnecting Wires

Gold and aluminum wires are used in power hybrid microcircuits as jumpers and for interconnections of:

• Semiconductor chip pads to conductor pattern on the substrate

• Conductor to conductor

• Thin-film and thick-film resistors to conductors

• Miniature components (chip inductors, optocouplers, etc.) to conductors

• Package leads to conductors or tabs

Selection of the wire material and diameter depends on the type of the component, size and material of bonding pad, conductor metallization on the substrate, and current carrying requirement. Majority of all low power diodes, transistors and integrated circuits are interconnected using gold (Au 99.99%) or aluminum (Al-1% Si) bonding wires. Power devices and high current jumpers between substrates and to the package pins are bonded with large diameter aluminum (Al 99.99%) wire. When electric DC current flows in a cylindrical bonding wire it results in power dissipation P_D:

$P_D = I^2R$

Wire resistance R is equal to

$$R = \rho\frac{L}{S}$$

where

ρ = electrical resistivity of wire material
L = wire length
S = cross-sectional area of the wire equal to

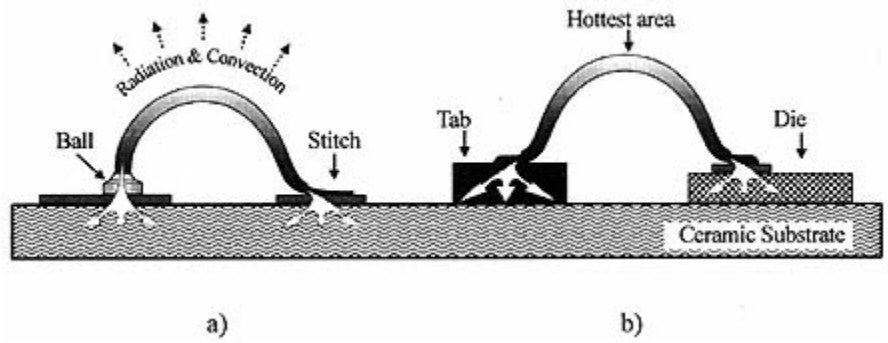


Figure 3-6
Heat removal mechanism from the bonding wires:
a) gold wire-bond, b) aluminum wire-bond.

$$S = \frac{\pi D^2}{4}$$

Substituting R and S into the first equation yields

$$P_D = \frac{4\rho L}{\pi}\left(\frac{I}{D}\right)^2$$

Power dissipated in the wire is removed in the form of heat by means of convection, radiation and conduction as shown in Figure 3-6.

Two wire-bonds are shown in the picture: a) gold wire connecting substrate metallization pads, and b) aluminum wire bonded from semiconductor chip to a metal tab. Wires used for interconnections in the power hybrids seldom exceed 0.5" in length. Incorrectly selected wire diameter and material may result in its fusing and jeopardizes the operation of the circuit. Conditions required for fusing of the wire depend on:

• Magnitude and duration of electric current

• Wire length and cross-sectional area

• Wire material

• Ambient temperature

• Thermal resistance from the bond end to the heatsink

• Thermal radiation and thermal convection parameters

Heat removed from the wire-bond by radiation and convection is insignificant when compared with heat transfer by conduction through bond ends. This is due

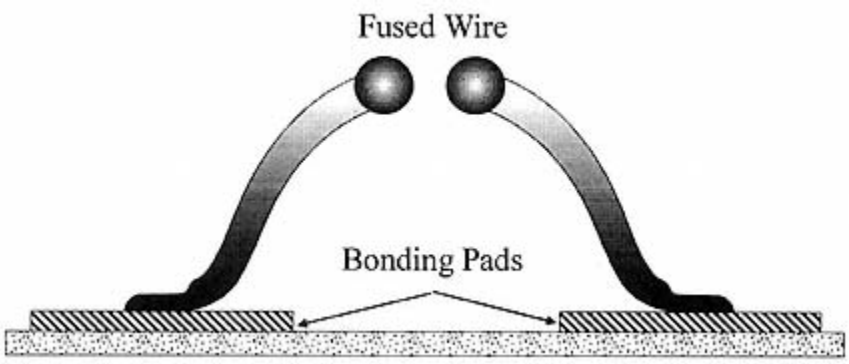


Figure 3-7
Fused wire-bond.

to a very short length of the bonding wires and diminutive heat emitting surface area. Values of fusing currents for gold and aluminum wires are listed in Table 3-4.

The efficiency of heat removal from wires by conduction depends on several parameters:

• Thermal conductivity of wire material — Al 99.99% has higher conductivity and therefore higher fusing current values than Al-1%Si.

• Quality of interface between wire and bonding pad — contamination on the bonding pad or reduced contact area result in higher temperatures and premature bond failure.

• Thermal conductivity of the material of bonding pad — higher thermal resistance results when wire is bonded to aluminum pad on silicon chip, when compared with a bond to a metal tab.

• Wire end configuration — ball has a larger contact surface than the stitch side of the bond.

The hottest spot on bond surface is located approximately in the middle of the loop, the most distant point from both ends. When the wire fuses, it looks similar to the illustration shown in Figure 3-7. Small balls of molten wire are frequently scattered across the substrate area, creating a hazard of short circuit. Design values for maximum current carrying capacity of bonding wires should not exceed ½ of the fusing current values of Table 3-4.

Table 3-4 DC fusing current values for bonding wires

Composition /	Au (99.99%)				Al (99.99%)						
Wire diameter	Wire length (mils)				Wire length (mils)						
(mils)	50	100	150	200	50	100	200	300	400	500	50
1	1.6	0.8	0.536	0.4	1.2	0.6	0.3	0.2	0.15	0.12	0.8
2	6.4	3.2	2.16	1.6	4.8	2.4	1.2	0.8	0.6	0.48	3.2
3	14.4	7.2	4.8	3.6	10.8	5.4	2.7	1.8	1.35	1.08	7.2
4					19.2	9.6	4.8	3.2	2.4	1.92	12.8
5					30	15	7.5	5.0	3.75	3.0	20
8						38.4	19.2	12.8	9.6	7.68	
10						60	30	20.0	15.0	12.0	
12						86.4	43.20	28.8	21.6	17.3	
15						135	67.5	45.0	33.8	27	
18						194.4	97.2	64.8	48.6	38.9	
20						240	120	80.0	60.0	48.0	
25						375	187.5	125.0	93.8	75.0	

3.4—
Adhesives

Since introduction in the early 1960s a large selection of adhesives became available for hybrid applications. Nonconductive and conductive adhesives are used in power hybrids to provide mechanical bond and electrical contact. Conductive adhesive is used primarily to attach low power semiconductor devices, integrated circuits, thin-film resistors with backside contact, and capacitors. Nonconductive adhesive is used to provide mechanical bond when electrical contact is not required. It is used to mount ceramic substrate in the case and attach passive components, such as inductors, ferrite cores, thick-film resistors, and optocouplers to the substrate. It is also used to reinforce large ceramic and tantalum capacitors, which require electrical contact but need additional bonding to the substrate. Implementation of Mil-Std-883C, Method 5011 established a new standard for adhesives used in high reliability military and space applications.

Most frequently used methods of application of die attach adhesives are: dispensing and screen printing. The latter has to be applied before substrate is mounted in the case. Electrical, mechanical and chemical properties of adhesives must be considered when selecting materials for application in power hybrids.

3.4.1—
Electrical Characteristics

Volume resistivity is a bulk property which is defined by the percentage of the metal filler used in the adhesive. Performance of conductive adhesives varies with temperature and aging. Resistivity of epoxy adds to forward voltage drops of diodes and saturation voltages of transistors. When these parameters are critical to circuit operation, alternate techniques should be employed. Die can be eutectically attached to a metal tab and then attached to the conductor using epoxy.

3.4.2—
Mechanical Characteristics

Thermal conductivity of adhesives is very low and varies from 0.044 W/°C-in for conductive to 0.025 W/°C-in for nonconductive adhesives. It is quite adequate for attachment of low power dissipating components, but should be used with great caution when good thermal performance is required.

Thermal expansion of adhesives is less than 65 ppm/°C below the glass transition temperature Tg. At the temperatures above Tg it rapidly increases with the upper limit of 300 ppm/°C. Glass transition temperature Tg is the softening temperature of adhesive. It varies from 80°C to 150°C and depends on the temperature and time of cure. The following factors have to be considered when selecting adhesives:

• Wirebonding temperature has to be lower than Tg, otherwise the die can move during wire bonding operation.

• Tg must be high enough to allow repeated rework in the hybrid — removal of the substrate from the case and replacement of the failed components.

3.4.3— Chemical Characteristics

Ionic contamination produces corrosive mobile ions, such as chloride, which migrate to chip surface and may cause corrosion of bond pad metallization. Potential risk of corrosion is much greater in nonhermetic assemblies where moisture contents is high compared with hermetic enclosures. Mil-Std-883C, Method 5011 sets the limits to ionic impurity levels:

• Total Ionic Content	≤ 4.5 mS/meter
• Hydrogen (pH)	4.0 ≤ 9.0
• Chloride	≤ 300 ppm
• Sodium	≤ 50 ppm
• Potassium	≤ 50 ppm
• Fluoride	≤ 50 ppm

3.5— Solders

Availability of large selection of solder compositions used in many different applications extends a comprehensive discussion of the art and science of soldering well beyond the intention of this book. This paragraph shall be limited to include only these materials and processes, which are pertinent to the applications in the power hybrids.

Soldering can be defined as a process of heating, which produces coalescence of metals by using a filler metal having a melting point below 840°F and lower than solidus of the base metals. The heat causes the solder to melt. If both parts are free of contamination and have good mechanical contact, the solder flows and wets both surfaces. The parts are joined when the solder solidifies. Some solder alloys are eutectic — compositions of metals which melt at the lowest temperature. The liquidus and solidus temperatures of these alloys are the same. Main advantages of using solder in the power hybrid assemblies include:

• Excellent heat transfer due to high thermal conductivity

• Tensile strength

• High electrical conductivity

• Corrosion resistance

• Impervious to moisture

• Metallurgical compatibility with base metals used in power hybrids

• High operating temperatures

• Thermal stability

• Repairability

Solder is available in a preform, wire, or paste form. Solder preforms are typically stamped from a thin sheet of solder alloy and have a circular, rectangular, or custom shape. The preforms can be coated with flux to enhance wetting, when used in low cost commercial applications. Flux is used to facilitate removal of oxides and other contaminants from the soldered surface and is available in five types:

• R–type flux contains pure water white rosin as an activator. This is the safest and least active of flux types, which is used only with good wettability solders on highly solderable conductors, such as gold and silver.

• RMA–type flux contains pure water white rosin with the addition of a small amount of nonionic halogenated compound, which effectively increases fluxing action. It is useful for soldering to gold, platinum-silver, palladium-silver, and silver thick-film metallizations.

• RA–type flux contains pure water white rosin or other resins with addition of small amount of ionic halogen. There is a possibility of corrosion, if flux residue is not removed.

• RSA & OA–types are highly corrosive and are not used in hybrid micro-electronics.

Solder in wire form can be solid or flux-cored. The solder paste is made by suspension of small solder particles in the flux vehicle and can be applied by screen printing or dispensed by syringe. In general no flux should be used in the soldering process, when manufacturing power hybrids for use in high reliability military or aerospace applications.

Solder alloys can be divided into several groups:

• Combination of lead (Pb) and tin (Sn) forms the largest category of solder alloys used in electronics industry. Variation in the amount of tin and lead will produce solder compositions with different melting ranges and joining characteristics. The tin components in the solder reacts with the base

metal and creates a strong but brittle joint. Addition of lead to alloy, decreases the melting temperature and increases solder strength. Compositions vary from eutectic alloy 37% lead–63% tin with melting temperature point of 183°C to 95% lead–5% tin with melting temperature range 310°C–314°C.

• Lead–tin–silver alloys are popular solders useful for soldering against pure silver or silver bearing conductors. It is believed that presence of silver in the alloy minimizes scavenging of silver from thick-film conductors and increases its strength. Eutectic alloy 62% tin–36% lead–2% silver, also known as Sn62, has a melting temperature point of 179°C. At high temperature range the eutectic alloy 97.5% lead–1.5% silver–1% tin can be used.

• Tin–silver and tin–antimony alloys provide excellent wetting and higher strength than tin–lead solders. These solders are used when high tensile strength at high temperature is required. Popular compositions include eutectic alloy 96% tin–3.5% silver with melting point at 221°C, 99% tin–1% antimony with melting point of 235°C.

• Lead–indium solders have very low scavenging and leaching of gold surfaces, and are resistant to alkaline corrosion. Lead–indium solders were proven to have superior fatigue resistance and very slow crack propagation during temperature cycling. Available alloys include: 60% indium–40% lead solidus at 174°C and liquidus at 185°C; 50% indium–50% lead solidus at 180°C and liquidus at 209°C; 19% indium–81% lead solidus at 270°C and liquidus at 280°C. The plasticity of indium helps to compensate for material mismatch in hybrid construction

• Gold containing alloys are primarily used for die attachment.

• 80% gold–20% tin with melting temperature point at 280°C. This alloy is used in specialized instances to attach the substrate to the case or in assembly of hybrid packages when high brazing temperatures are prohibitive.

• 88% gold–12% germanium with melting temperature point at 356°C is used to attach silicon, gallium-arsenide, or phosphide die. It is also used in the assembly of hybrid packages, when high brazing temperatures are prohibitive.

• 98% gold–2% silicon solidus at 370°C and liquidus at 800°C is used to attach silicon, gallium-arsenide or phosphide die.

Physical properties of solders are listed in Tables 3-5 through Table 3-9. Development of a compatible material system is essential to ensure a reliable

Table 3-5 Physical characteristics of tin (Sn) — lead (Pb) solders

Alloy composition	Temperature		E/MP	Electrical conductivity (% of copper)	Density (lb/in^3)
	Liquidus (°C/°F)	Solidus (°C/°F)			
63 Sn, 37 Pb	183/361	183/361	E	12.5	0.3032
70 Sn, 30 Pb	186/367	183/361		13.4	0.2946
60 Sn, 40 Pb	188/370	183/361		12.3	0.3068
50 Sn, 50 Pb	212/413	183/361		11.3	0.3202
95 Sn, 5 Pb	222/432	183/361			0.2679
100 Sn	232/450		MP		0.2628
40 Sn, 60 Pb	238/460	183/361		10.5	0.3350
30 Sn, 70 Pb	257/496	183/361		9.8	0.3509
10 Sn, 90 Pb	302/576	275/527		8.6	0.3881
5 Sn, 95 Pb	314/598	310/590		8.3	0.3980
100 Pb	327/620		MP		0.4090

Table 3-6 Physical characteristics of tin (Sn) — lead (Pb) — silver (Ag) solders

Alloy composition	Temperature		E/MP	Electrical conductivity (% of copper)	Density (lb/in^3)
	Liquidus (°C/°F)	Solidus (°C/°F)			
62.5 Sn, 36.1 Pb, 1.4 Ag	179/355	179/355	E	11.6	0.3036
60 Pb, 37 Sn, 3 Ag	232/450	179/355			0.3390
88 Pb, 10 Sn, 2 Ag	299//570	268/514			0.3887
92.5 Pb, 5 Sn, 2.5 Ag	296/565	287/549			0.3978
90 Pb, 5 Sn, 5 Ag	292/558		MP		0.3971
95.5 Pb, 2 Sn, 2.5 Ag	304/580	299/570			0.4043
97.5 Pb, 1 Sn, 1.5 Ag	309/588	309/588	E		0.4072

Table 3-7 Physical characteristics of tin (Sn) – silver (Ag) and tin (Sn) – antimony (Sb) solders

Alloy composition	Temperature		E/MP	Electrical	
	liquidus (°C/°F)	solidus (°C/°F)		conductivity (% of copper)	Density (lb/in^3)
96.5 Sn, 3.5 Ag	221/430	221/430	E	16	0.2657
97.5 Sn, 2.5 Ag	226/438	221/430		16	0.2650
99 Sn, 1 Sb	235/456		MP		0.2624
98 Sn, 2 Sb	235/456	232/450			0.2690
97 Sn, 3 Sb	238/460	232/449			0.2621
95 Sn, 5 Ag	240/464	221/430			0.2668
95 Sn, 5 Sb	240/464	232/450			0.2617

Table 3-8 Physical characteristics of indium (In) based solders

Alloy composition	Temperature			Electrical	
	liquidus (°C/°F)	solidus (°C/°F)	E/MP	conductivity (% of copper)	Density (lb/in^3)
60 In, 40 Pb	185/365	174/345		7.0	0.3077
50 In, 50 Pb	209/408	180/356		6.0	0.3198
40 In, 60 Pb	225/437	195/383		5.2	0.3355
25 In, 75 Pb	264/508	250/482		4.6	0.3599
19 In, 81 Pb	280/536	270/518		4.5	0.3707
5 In, 92.5 Pb, 2.5 Ag	300/572		MP	5.5	0.3978
5In, 90 Pb, 5 Ag	310/590	290/554		5.6	0.3971

Table 3-9 Physical characteristics of gold (Au) based solders

Alloy composition	Temperature		E/MP	Electrical conductivity (% of copper)	Density (1b/in^3)
	liquidus (°C/°F)	solidus (°C/°F)			
80 Au, 20 Sn	280/536	280/536	E	4.8	0.5242
80 Au, 12 Ge	356/673	356/673	E	6.0	0.5301
96.4 Au, 3.6 Si	370/698	370/698	E		0.5564
98 Au, 2 Si	800/1472	370/698			0.6113
82 Au, 18 In	485/905	451/843			0.5752

operation of the power hybrid in adverse environmental conditions.

Soldering process in general is well understood and characterized. However, many problems may occur, i careful consideration is not given to requirements of the application and compatibility of selected material It is not uncommon to use solders with different melting temperatures in the same hybrid construction

Table 3-10 Applications and compatibility of solder alloys

Metallization type	Compatible solder alloys
Thick-film substrate metallization:	
a) Gold	Indium based solders, AuSn, AuGe
b) Platinum–gold	Gold based solders, lead–tin based solders
c) Silver	Lead–tin and lead–tin–silver based solders
d) Platinum or palladium–silver	Lead–tin and lead–tin–silver based solders
e) Copper	Lead–tin and lead–tin–silver based solders
Semiconductor back side metallization	
a) Gold over silicon	AuSn and AuGe
b) Titanium–nickel–silver or similar	Lead–tin, lead–tin–silver and lead–indium–silver based solders
Hybrid case plating:	
a) Gold (>50 inches) over nickel	Indium based solders, AuSn, AuGe
b) Gold (10-20 inches) over nickel	Indium based solders, AuSn, AuGe lead–tin and lead–tin–silver based solders
c) Nickel	Lead–tin and lead–tin–silver based solders

to accommodate step soldering. Usually, selection of solder is done concurrently with selection of the metallization type and is influenced by the type of the back metallization, when a semiconductor die has to be soldered. Certain rectifier die are manufactured with aluminum top contact (anode) and are not suitable for soldering to that side. Simple solder selection guidelines are listed in Table 3-10.

References

1. Powers, M.B., "Potential Beryllium Exposure While Processing Beryllia Ceramics For Electronic Applications," Brush Wellman, Inc., 1985

2. *Guide to Selecting Engineered Materials*, Advanced Materials and Processes, ASM International Publication, Special Issue 1989.

3. Suryanarayana, D., "Thermally Conductive Ceramics for Electronic Packaging," ASME Trans. J. Electron. Packag. 111:192–198, 1989.

4. McPhillips, R. B., "Advanced Ceramic Materials for High Thermal Conductivity Substrate Applications," Hybrid Circuit Technology, August 1988, pp. 21–23.

5. *Materials for High Technology Applications*, Dow Corning Product Guide, Form 10-008E-89, Dow Corning Corporation, Midland, Michigan, 1989

6. Copeland, D. W. and Powell, D. O., "Aluminum Nitride Metallized Ceramic Substrate Performance," 6th Annual IEEE Semiconductor Thermal and Temperature Measurement Symposium Proc., February 1990, pp. 104–107.

7. Dickson, J., "Direct Bond Copper Technology," Proceedings of Nineteenth International Power Conversion Conference, 1989, pp. 287–294.

8. Barnwell, P., Brakspear, S. and Cen, Y., "Thick-Film Substrates," Advanced Packaging, March/April 1994, pp. 18–23.

9. Moravec, T. J. and Partha, A., "Diamond Takes The Heat," Advanced Packaging, October 1993, pp. 8–11.

10. Greiner, S. and Krum, A., "Selecting a Substrate Technology for Power Hybrid Applications," Electronic Packaging and Production, May 1992, pp.54–57.

11. Dupin, P., "Aluminum Nitride Ceramic for Power Hybrid Substrates," Hybrid Circuit Technology, July 1990, pp.43–44.

12. O'Brien, K., "Power Hybrids Spark Substrate Challenges,", Hybrid Circuit Technology, November 1991, pp. 14–22.

13. Konsowski, S. G., Olenick, J. A., Hall, R. D. and Leahy, K. A., Evaluation

of Advanced Ceramics for High Power and MicrowaveCircuitry—Part II," International Journal for Hybrid Microelectronics, Vol. 10, No. 3, 1987.

14. Blum, J. B., "Aluminum Nitride Substrates for Hybrid Microelectronic Applications," Hybrid Circuit Technology, August 1989, pp. 7–14.

4—
Power Hybrid Design

4.1—
Introduction

Rapid rate of change in technology and the global marketplace induced vital changes upon existing business organizational forms. Companies restructured to address demand for customer oriented business practices and effective utilization of available resources. Virtually all organizations are either engineering, marketing or manufacturing driven. Conceptually, high technology companies are project-driven and are based on a multidisciplinary decision-making process. The hybrid design practices in a project-oriented company require a highly specialized and disciplined team effort of engineering, marketing, operational and manufacturing departments with considerable involvement of customer representatives as shown in Figure 4-1.

Generally the new product initiation starts with market research. Its objective is to define the market segment, analyze the development trends and project anticipated needs for new products. The effort to define the target specification for new product is often highly integrated with ongoing programs and involves key personnel from prospective users and the design organization. Customers come in various forms and sizes. Their technical requirements and schedule limitations are different and sometimes require to fit specific needs of a single customer, rather than creating demand for a standard product. The resulting consequence: two types of products, standard, and custom. Circumstances lead-

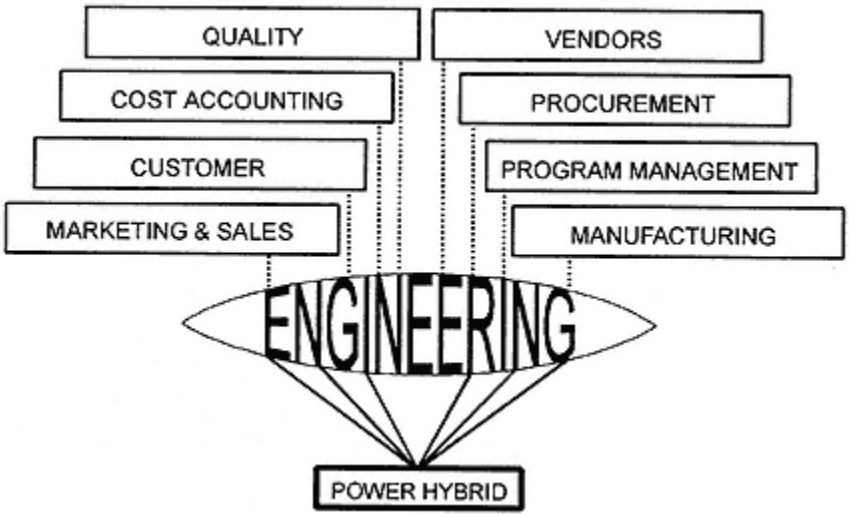


Figure 4-1
Diagram of multidisciplinary interface.

ing to development of a custom power hybrid product include:

• Highly specialized system requirements such as size, weight, outline configuration, operating environment, and electrical performance characteristics, which do not allow use of available standard products

• Build-to-print a unique circuit configuration, proprietary to a specific customer

• Unexpected system performance specification change at the last minute, when extra space for additional circuitry is not available

Advantages and disadvantages of using custom and standard power hybrids in the electronic systems are listed in Table 4-1.

Every project has certain phases of development, which are known as life-cycles. A clear understanding of these phases permits company's management to control available resources effectively and achieve the desired goals on time. The chart in Figure 4-2 shows major phases of power hybrid product life cycles. This generalized chart may not necessarily apply to every organization, because of large diversity in companies' management styles and product types.

4.2—
Functional Design Flow

Power hybrid design cycle is initiated during conceptual definition phase. At that

Table 4-1 Use of standard and custom power hybrids

Power hybrid type	Advantages	Disadvantages
Standard	Off-the-shelf availability	Limited functionality
	Low cost	Available to competition
	Multiple sources of procurement	
	Performance history	
Custom	Tailored performance	Long development time
	Use of advanced semiconductor and packaging technologies	High cost
	Fast custom modifications	
	Efficient utilization of space	
	Proprietary	

time the first bits of information are accumulated to form an outline for a new product. A project team is formed to facilitate a successful completion of the project. The project team manager is responsible for effective accomplishment of his team's goals and objectives. He must have a thorough knowledge of his business organization, provide technical expertise, assist in problem solving and have good leadership and communications skills. The project manager must act across functional and organizational lines in order to bring together team members from different departments and coordinate their work.

First phase of development cycle in Figure 4-3 is dedicated to accumulate information sufficient to initiate design of power hybrid. Information available at that phase strongly depends on circuit type: custom or standard. To initiate the design of custom power hybrid, the following information should be obtained from the customer:

1. General

• Circuit schematic

• Bill of materials

• Operating breadboard (when available)

• Quality assurance and reliability requirements

- Screening requirements (temperature cycling, burn-in, etc.)

- Qualification program and prototype approval plan

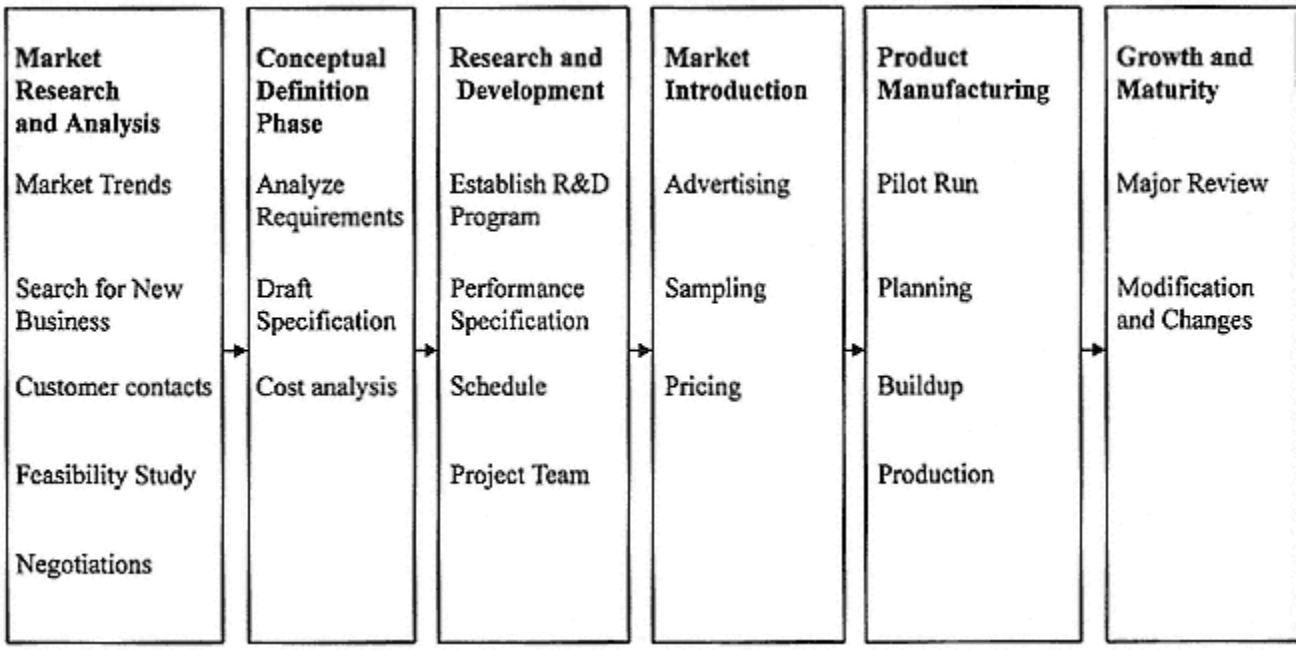


Figure 4-2
Product life cycles.

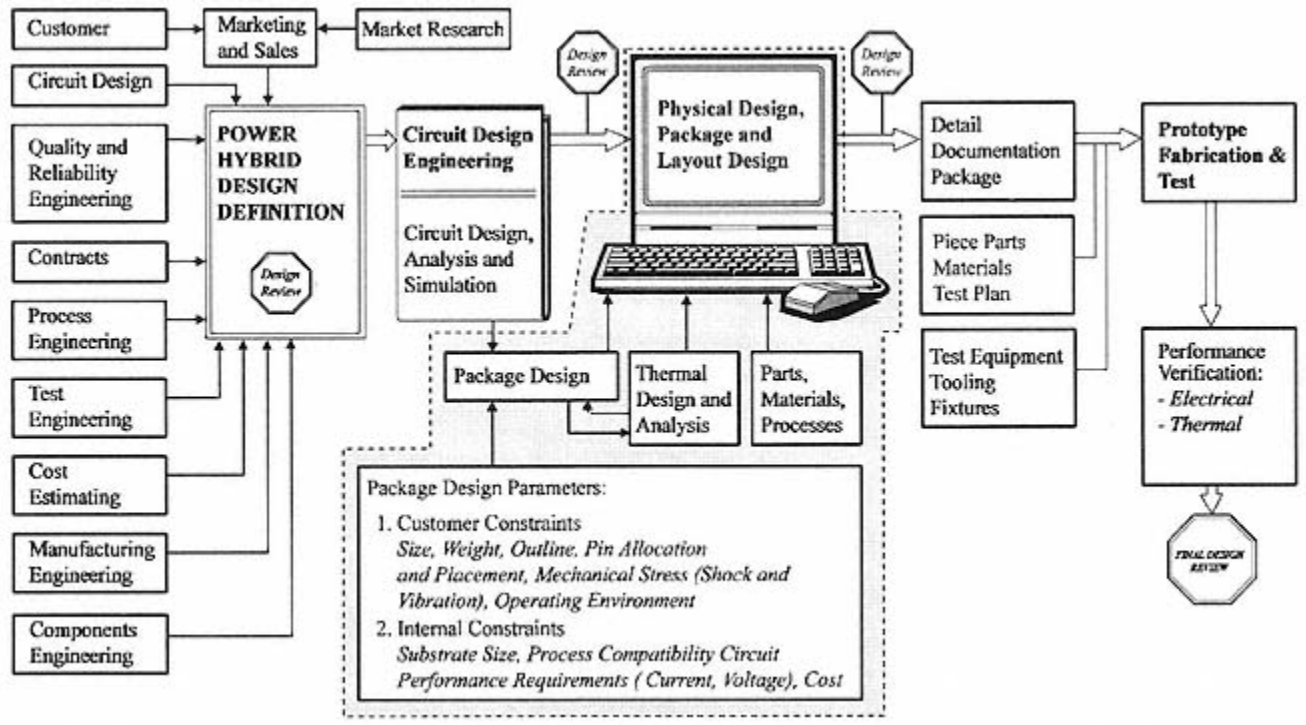


Figure 4-3
Functional power hybrid design flow.

- Air
- Vacuum
- Liquid (oil, etc.)

• Prototype delivery date

• Target cost

• Projected manufacturing rate and quantity

• Configuration control

• Definition of proprietary features

2. Performance

• Electrical

- Performance specification
- Test specification
- Breadboard test results (when available)
- Requirements for nonstandard components (matched or selected parameters, restricted procurement to a specific manufacturer, etc.)
- Tolerances on system voltages (input and power supply)
- Transient voltage conditions in the system

• Mechanical

- Size limitations (including height)
- Weight limitations
- Outline form factor (length/width)
- Type of electrical interface with the system (wires, PWB, etc.)
- Mounting surface (material, plating and flatness)
- Hybrid package lead configuration (straight or formed)
- Mechanical shock requirements (axis definition - X, Y, or Z)
- Vibration requirements (axis definition - X, Y, or Z)

- Constant acceleration requirement (axis definition - X, Y, or Z)

• Thermal

- Operating temperature range
- Storage temperature range
- Maximum temperature at power hybrid/heatsink interface

- Maximum thermal resistance (junction-to-case)

- Maximum allowable operating junction temperature

- Type of cooling (heatsink, air flow, liquid, etc.)

Information requirements for commencement of a standard power hybrid design are similar to those listed above. However, some of the data items may be not available because the definition of a standard product is based on marketing information obtained from a large number of companies with diversified field of application requirements. These data items are shown as italic and are usually defined at a later design phase. Certain critical definitions must be made at the onset even when accurate information is not available:

• Targeted Applications with Required Functionality

• Circuit Block - Diagram with I/O Functional Description

• Draft Performance Specification and Main Performance Features

• Target Package Size

• Required Thermal Performance

When the initial draft specification is defined, the electrical engineer can start the circuit design. After completion of paper design the engineer will perform the first run of circuit analysis and simulation. When the results are satisfactory, a breadboard circuit is built. Extensive testing and concurrent changes and improvements are made on the breadboard. At that time any additional available marketing requirements can be effectively implemented without causing project delays or development cost overruns. After completing all tests and successfully meeting performance specification targets, the engineer prepares for circuit design review. A detail bill of materials, circuit diagram, test results, and breadboard are presented for review by representatives of the following disciplines:

• Sales and Marketing

• Circuit Design Engineering

• Process Engineering

• Manufacturing Engineering

• Test Engineering

• Components Engineering

• Quality Assurance Engineering

• Procurement

All inputs are vital to the effective progress of the project. If changes to the

design are necessary at that time, they can be implemented with minimal impact on program cost and schedule. The list of review points includes but is not limited to:

1. Bill of materials

• Availability of components

• Component cost

• Availability of multiple sourcing

• Vendor history and approval

2. Circuit schematic, analysis and simulation results, test results

• Performance specification requirements

- Update (new inputs)

- Correlation of test data with specification requirements

- Tolerances and worst case study

- Testability

3. Schedule

• Update

4. Recommendations for layout design

4.3—
Physical Design

After all comments and changes documented during the circuit design review are implemented, the design engineer prepares for the next phase: physical design and layout. The physical design of power hybrid consists of five steps described in Figure 4-4:

A. Circuit partitioning

B. Area study

C. Package design

D. Layout design

E. Detail documentation (substrate fabrication, assembly and test)

4.3.1— Circuit Partitioning

Circuit partitioning is an act of dividing the circuit into clearly defined functions

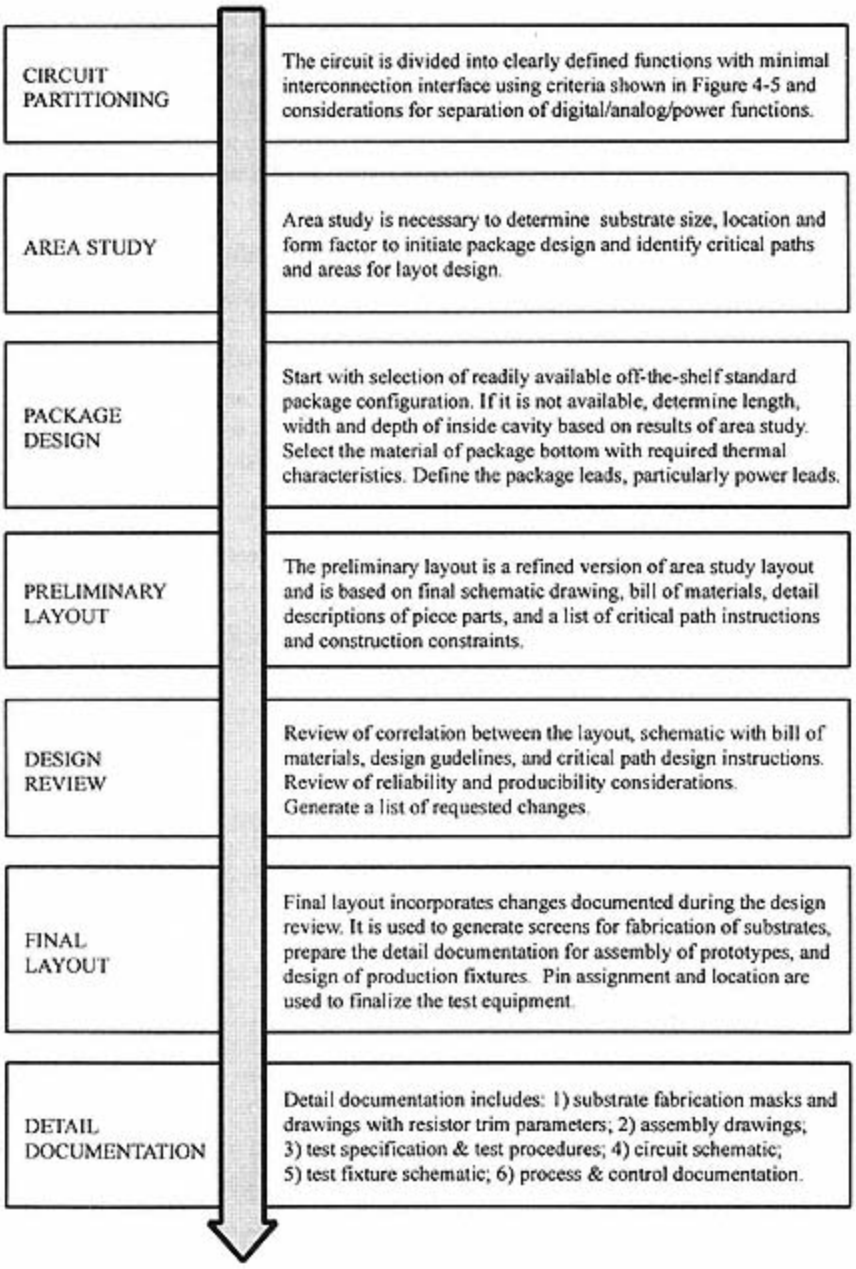


Figure 4-4
Power hybrid physical design flow.

with minimal interconnection interface. The criteria for partitioning is summarized in Figure 4-5. Partitioning of power hybrid microcircuit is different from partitioning done on the system level. This occurs primarily because of special considerations that have to be given to constructing a power hybrid using highly advanced technology with its unique materials, processes and techniques.

The main purpose of partitioning is to identify parts of the circuits that have to be isolated from each other for the following reasons:

1. Producibility. Each segment (substrate with assembled components) can be effectively manufactured using minimal different number of techniques and processes resulting high yields and low price.

2. Performance requirements. Complex power electronic circuit usually contains extensive power, analog and digital segments. It is essential to identify critical performance parameters of each of these segments and potential interaction between them to prevent detrimental cross-coupling effects.

• Considerations for separation of digital functions:

- Higher layout density of digital circuit can be achieved

- Power line decoupling for noise reduction

- Separate power and signal grounds to prevent false triggering and reduce coupling of high frequency switching transients into analog segment

- Thermal isolation from power segment

- Component placement

- Methods of construction and manufacturing technology

• Considerations for separation of analog functions:

- High gain-bandwidth product

- High sensitivity to noise

- Very low offset requirements

- Power line decoupling for noise reduction

- Separate power and signal grounds to prevent coupling of high frequency switching transients from power and analog segments

- High precision matching of semiconductor and resistor elements

- High sensitivity to electrical and thermal transients generated in power segment

- Power dissipation of selected semiconductor elements due to small size of components may require special assembly techniques (solder, eutectic to molytab, etc.) or substrate material

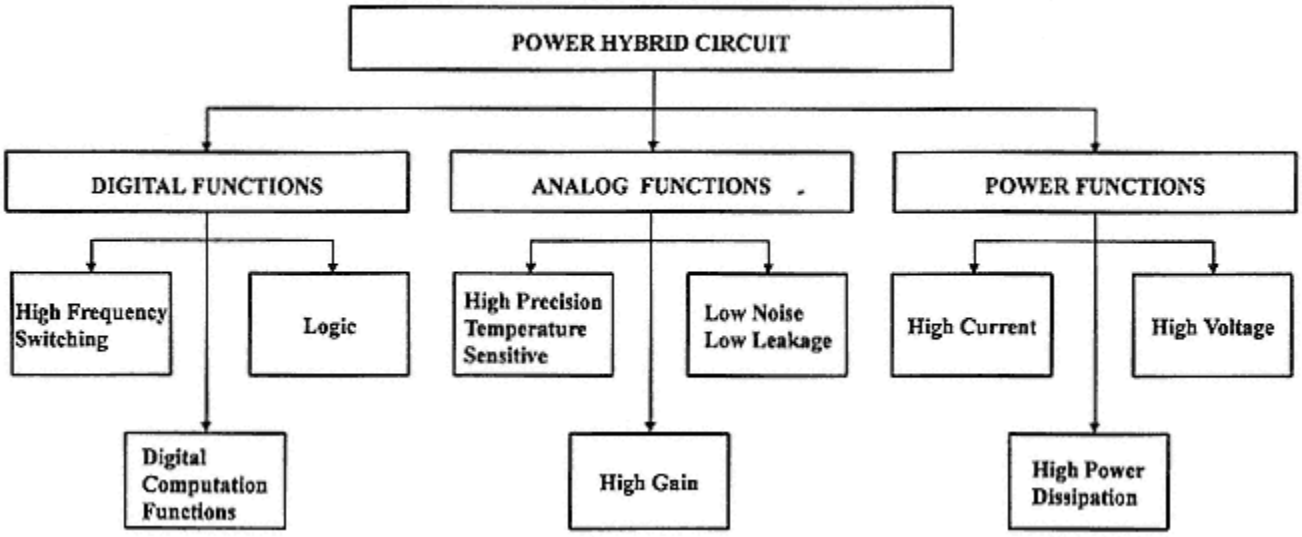


Figure 4-5
Partitioning of power hybrid microcircuit.

- Lower layout density, on account of large number of resistors, capacitors and sometimes small magnetics

• Technological considerations for separation of power functions:

- Distinctly different materials and processes are used in construction of power segment

- Large circuit elements are assembled with low component density

- Heavy bonding wires are used to interconnect components and I/O pins

- Substrate material is usually a high thermal conductivity ceramic, which has limited compatibility with thick-film processing

- Component and substrate assembly may require reduced or hydrogen atmosphere

- Assembly requires special reflow fixtures

• Electrical considerations for separation of power functions:

- Specially designed I/O leads are required to conduct large currents and provide isolation at high voltages

- Thick-film substrate metallization may not be suitable for conduction of large currents, which requires either added tabs or clad metallization

3. Cost

• Package leads connected to power segment are large in diameter and are made from high electrical conductivity materials. This considerably raises the package cost

• Substrate material is much more expensive than alumina

• Assembly of elements of power segment requires special fixturization and increased manual labor, elevating hybrid cost

• Rework of power segment may involve replacement of the entire power substrate

4.3.2— Area Study

Area study is necessary to determine the substrates' area, location, and form factor to provide sufficient information for package design. After circuit partitioning is completed, the schematic may be broken down into separate subassemblies, for example analog, digital and power as shown in Figure 4-6. Each subassembly has a separate bill of materials and component drawings. To assist in subassembly placement, a preliminary pin assignment is made at that time. When computer aided design (CAD) system is available, a "doll" of each component is drawn and

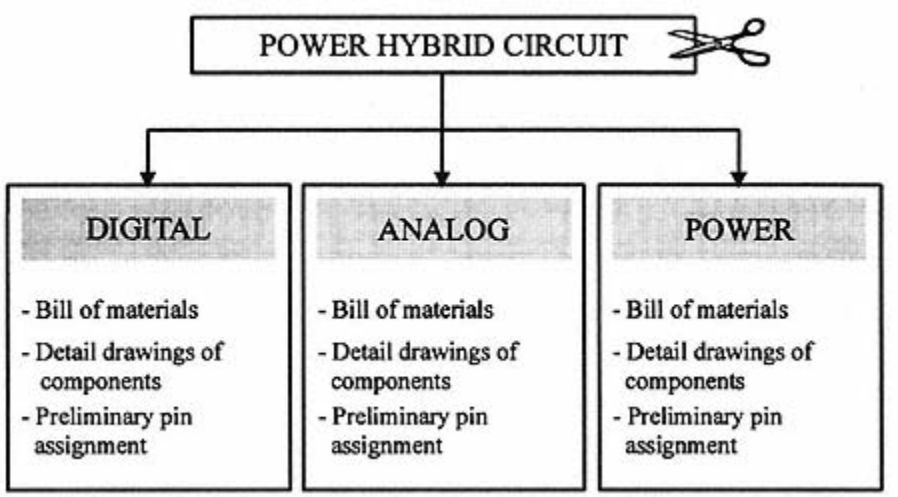


Figure 4-6
Area study design folder.

placed in an area dedicated for a specific subassembly. Components are placed at a distance from each other to allow for mounting pads, bonding pads and conductors. A schematic signal flow should be used as guidance for component placement. If CAD system is not available, each "doll" can be prepared at a scale 10:1 or larger from a heavy stock paper with reference designator marked on top and placed manually on drafting media. Mylar or vellum with grid are well suitable for that purpose. The area study layout will look similar to a hypothetical one shown in Figure 4-7, which is demonstrating the conceptual hybrid partitioning process.

The circuit schematic has been divided into three separate segments: digital, analog, and power. Each segment is built on a separate ceramic substrate effectively utilizing all advantages of hybrid technology. The digital substrate shall use alumina ceramic with multilayer thick-film metallization. That shall allow high density of component placement and interconnections.

All components shall be assembled using standard low power hybrid technology — die attach using conductive and nonconductive epoxy, and wire-bonding with small diameter gold or aluminum wires. The substrate shall be mounted in the case using nonconductive epoxy. The power dissipation of components selected for the analog substrate is low and doesn't require use of special processing or materials. Lastly, the power substrate combines all power dissipating components. Beryllia (BeO) has been selected for the substrate material due to its high thermal conductivity and compatibility with thick-film processing. Pinouts

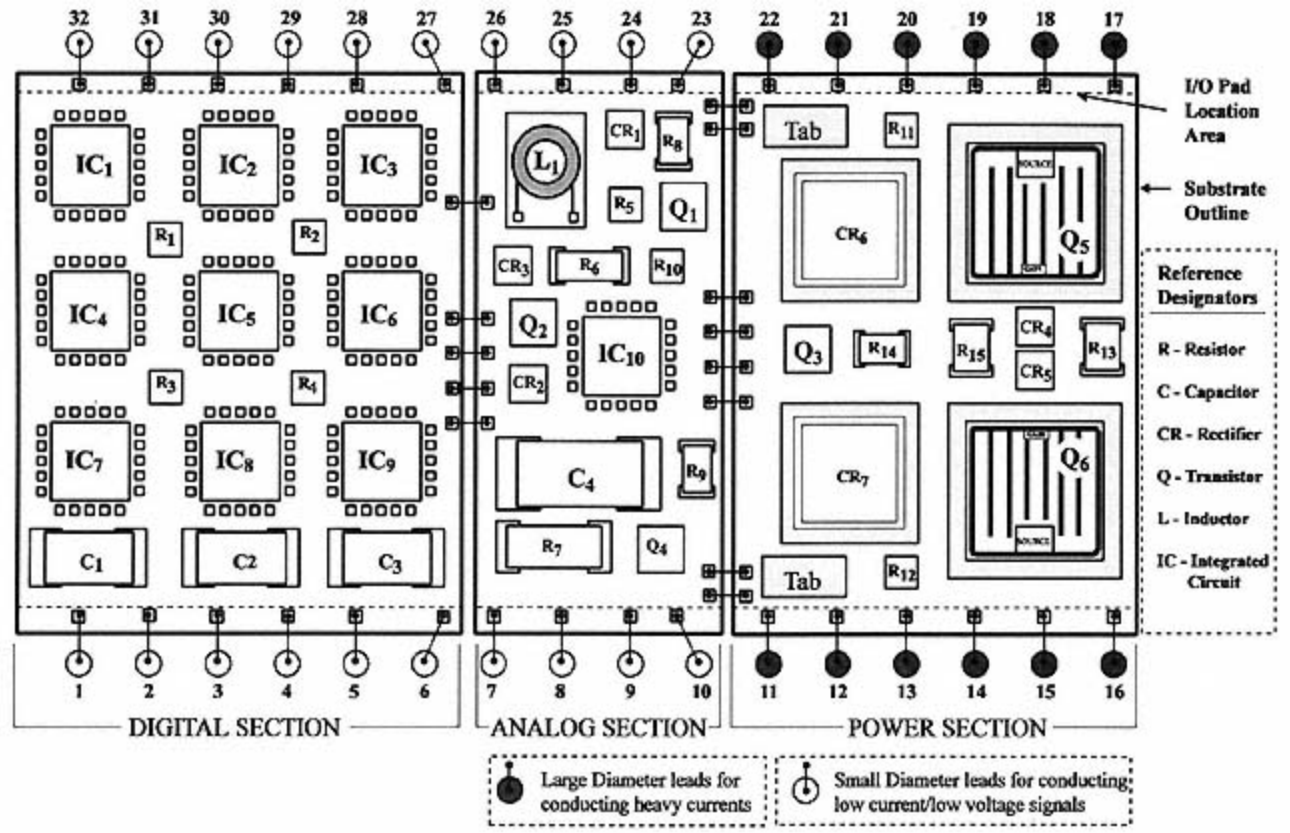


Figure 4-7
Area study component layout.

assigned to carry high currents in the vicinity of power substrate must be large in diameter and have low electrical resistance. Several additional pinouts are sometimes added to allow testing of otherwise inaccessible parts of the hybrid.

Additional benefits arise out of the partitioning process described herein. When the area study layout is done, the electrical, mechanical, and process design engineers have the first chance to review the draft hybrid proposal for layout and package design. Comments and changes made at this phase are very cost and time effective.

Other methods exist to calculate substrate area required for hybrid design. For example, the total area of all components may be calculated and thereafter multiplied by an empirical coefficient, which varies from company to company and may be between 2.5 and 4.0. This method has very limited usage in design of power hybrids, mainly due to the large size of its components and very specialized design and processing requirements.

Information obtained during area study may be summarized as follows:

• The number of individual substrates

• Individual substrate size

• Total required substrate area

• Substrate material

• Thermal performance requirements for power dissipating components

• Processing details of component and substrate assembly and mounting

• Pin location and functional assignment

4.3.3— Package Design

Package Design phase starts with a review of existing standard configurations. Selection of a standard package (better even if it exists in other products) benefits the project with lower cost (no tooling), faster procurement, better performance history, and existing test sockets and production fixtures. It pays to analyze trade-offs required to accommodate a standard package by going back and reviewing the circuit partitioning and area study. Nevertheless, it is likely that a suitable standard configuration package doesn't exist and a new one must be designed. The process of design of a new package is shown in Figure 4-8.

Paper design starts with building an outline around the substrates defined during the area study. Ideally, the substrate area perimeter should fit in the space between the package leads on two sides and the package walls on two other sides as illustrated in Figure 4-9. If the package has leads on all four sides the substrate must fit between leads on all sides. The dimension **A** in Figure 4-9 denotes the

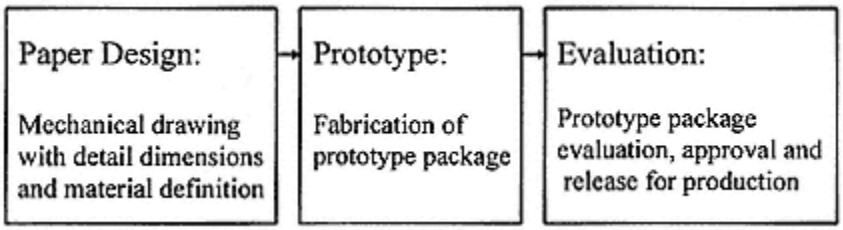


Figure 4-8
Package design phases.

minimum distance between the package wall and substrate edge and includes the corner radius, where wall meets the bottom. The distance between walls, **D**, is the minimum worst case dimension. Substrate size used in this calculation should include worst case maximum tolerances of substrate dimensions and location. The dimensions of fixtures used to locate the substrates in the package during assembly must be also taken into consideration. The dimension **B** in Figure 4-9 denotes the minimum distance from substrate edge to package pins. The distance between pins, **C**, is calculated as a minimum worst case dimension. Other dimensions that must be selected are shown in Figure 4-10:

L - overall package length is defined by:

customer constraints

substrate size

number of leads

W - overall package width is defined by:

customer constraints

substrate size

mounting flange requirements

hole size

wall thickness

inside lead length

l_1 - lead pattern depends on number of leads and their spacing

l_2 - lead spacing is the distance between centerlines of two adjacent leads

l_3 - first lead distance from package edge is defined by:

minimal required distance from the inside wall to the wire-bonding site on the pin

mounting hole diameter and location. The lead should not obstruct access to the mounting hole during screw assembly

l_4 - external lead length is defined by:

customer constraints

method of interconnection with system components socket, formed, and soldered to a PWB, formed upwards and soldered to wires, etc.)

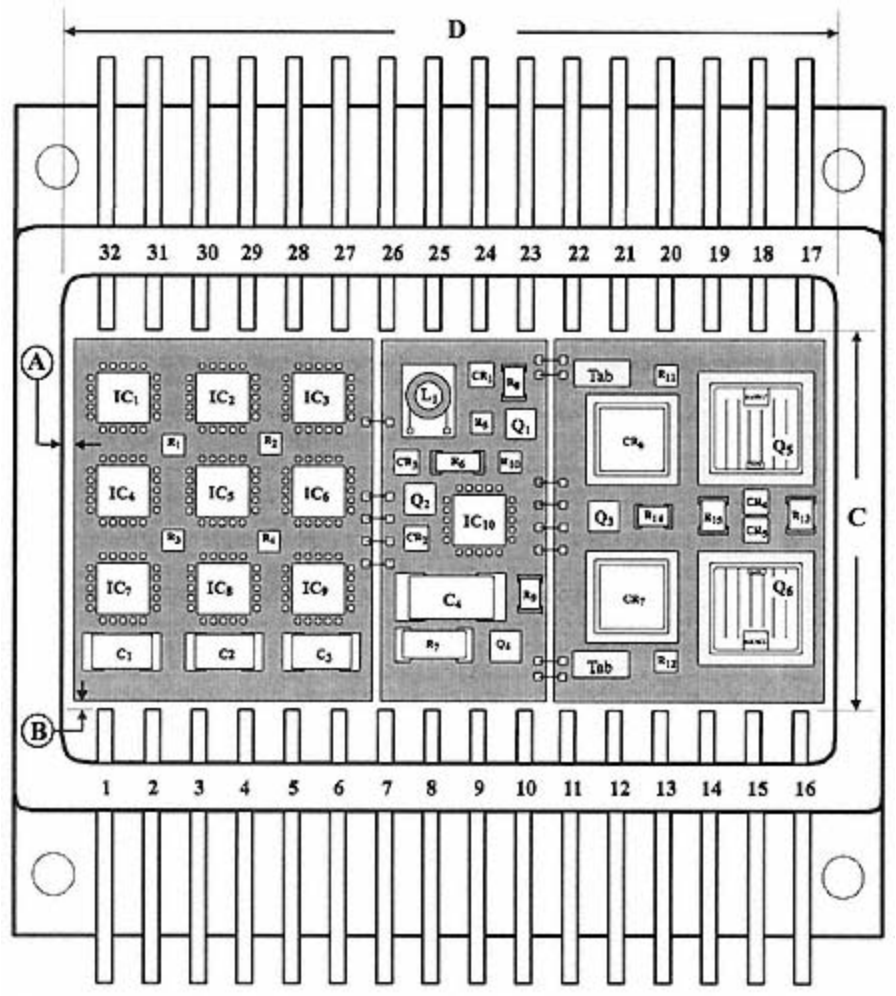


Figure 4-9
Area study layout fit in package.

final lead shape (formed or straight)

l_5 - length of flattened portion of the lead intended for wire bonding depends on pin diameter and wire diameter

l_5 - internal lead protrusion depends on lead diameter type of insulating bead and wire bonding technique (thermosonic, ultrasonic, etc.)

l_7 - lead height above the seating plane of the hybrid is defined by: lead location in the wall bottom thickness

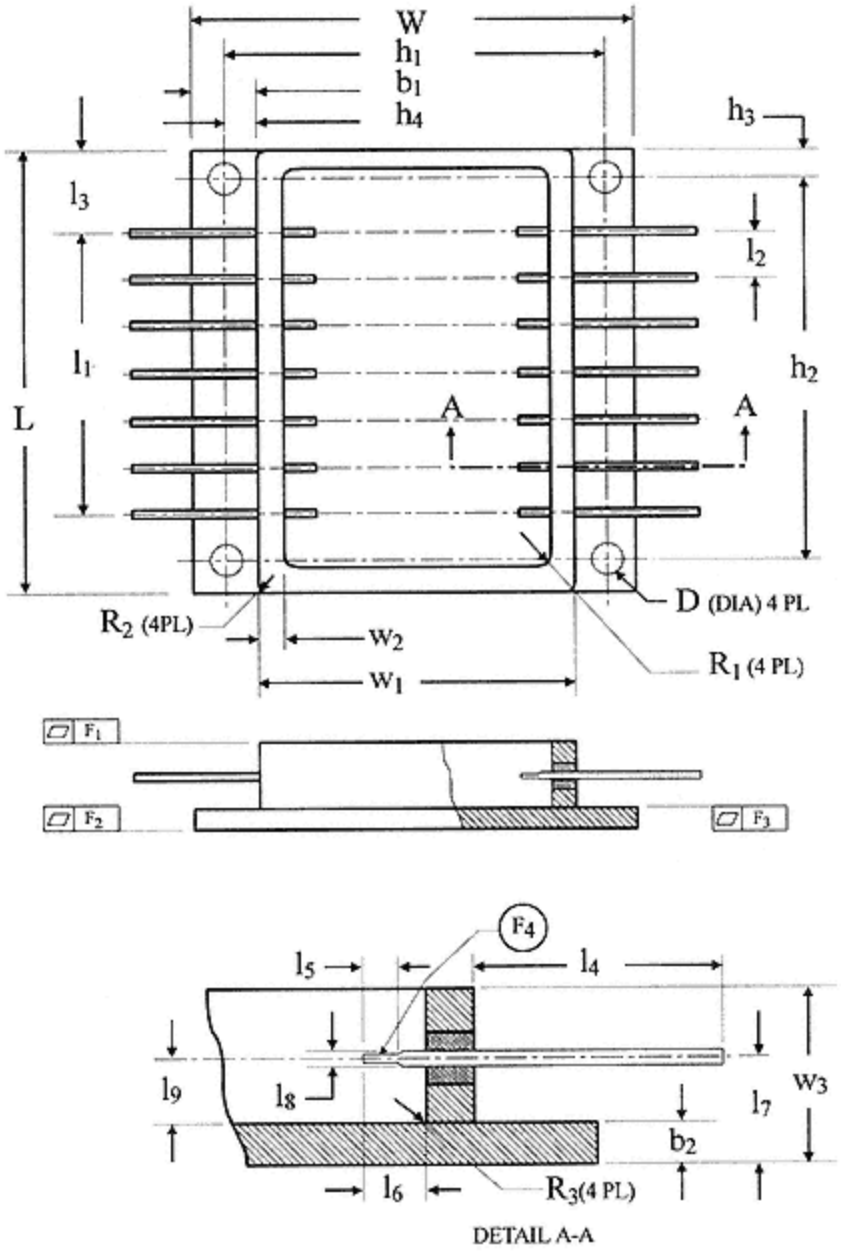


Figure 4-10
Power package — design guidelines and critical dimensions.

substrate thickness (it is desirable that pin bonding surface be located above substrate surface)

l_8 - lead diameter is defined by:
specified current carrying capability
required ability to be formed (heavy leads must be preformed prior to assembly into the package)
wire bonding method
wire-bond diameter

l_9 - lead height above the inside surface of the package is defined by:
the diameter of insulating bead
substrate thickness
distance of the bead mounting hole from wall edges

W_1 - external dimension of package wall is determined by substrate size, wall thickness and the inside pin length

W_2 - wall thickness must be thick enough to reliably support the lead assembly and depends on the diameter of insulating bead

W_3 - overall package height is defined by:
customer constraints
inside clearance requirement to accommodate large components
lead assembly dimensions
cover thickness
base thickness

b_1 - mounting flange width must provide sufficient room to accommodate mounting screws (use screw head dimensions)

b_2 - base thickness is defined by:
thermal performance requirements
mechanical properties of base material
package construction limitations
maximum allowable package size

h_1 - distance between centerlines of mounting holes on opposite flanges

h_2 - distance between centerlines of mounting holes on one side

h_3 - distance from package edge to centerline of mounting hole

h_4 - distance from outside wall to centerline of mounting hole

D - mounting hole diameter depends on mounting screw specifications

R_1 - inside wall radius

R_2 - outside wall radius

R_3 - inside radius at junction of wall and package base

F_1 - flatness of sealing surface

F_2 - flatness of outside base surface

F_3 - flatness of inside base surface

F_4 - minimum dimensions and flatness requirements for bond area depends on pin and wire-bond diameter.

The final design configuration is drawn on a detail drawing and includes the following information for review and approval by package manufacturer:

1. Complete set of dimensions with tolerances

2. Detailed description of package materials: base, walls, pins, and insulation beads. Braze material must be compatible with maximum operating and hybrid processing temperatures

3. Plating requirements

4. Solderability of base and pins

5. Environmental requirements, such as vibration, temperature cycling and thermal shock

6. Electrical performance requirements, such as maximum lead resistance and maximum leakage current between lead and case at the specified voltage

Early evaluation and approval of the design and required performance of the package by the manufacturer is vital to prevent unexpected problems at a later development phase. After approval, prototype units are manufactured. The availability of a small number of packages enables both — the hybrid design engineering and package manufacturer, to verify the validity of the design, and identify problem areas in package performance.

The prototype packages are subjected to extensive testing of:

• Mechanical dimensions and tolerances

• Case surface conditions

• Plating quality and thickness

• Physical appearance of glass insulators, leads, and braze joints

• Solderability of inside base surface

• Flatness of sealing surface

• Flatness of both base surfaces

• Solderability of leads

• Bondability of the inside lead surface

• Lead integrity

• Lead electrical resistivity

• Insulation resistance

• Hermeticity after lid seal and environmental screening

• Ability to withstand constant acceleration or mechanical shock test

Additional tests are performed after prototype power hybrid circuit is assembled in the case. They include mechanical, functional electrical, and thermal performance tests.

4.3.4— Layout Design

There is a considerable overlap in guidelines for design of low power and high power hybrids. This is apparent because the majority of medium and high complexity circuits are partitioned into the low power and high power sections, which are packaged in a single case. This section covers thick-film layout design guidelines which are not intended to be all inclusive. They are primarily aimed at specific areas of concern related to power hybrid microcircuits. Guidelines provided in this section address:

• Sequence of events

• Initial information for layout design

• General layout considerations

• Thick-film resistor design, dimensional constraints, and spacing

• Mounting pad dimensions, and spacing

• Thick-film conductors, dimensions, and spacing

• Wire bonding, pad dimensions, and spacing

Sequence of events for power hybrid layout design shown in Figure 4-11 starts with the preparation of the design folder. At this phase of hybrid design the following items would have been established and are included in the folder:

• Final circuit schematic

• Circuit partitioning into individual segments

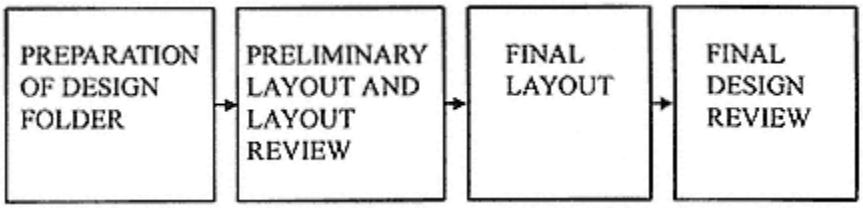


Figure 4-11
Power hybrid layout design (sequence of events).

• Parts list for each segment with detailed description of:

- component type
- value and tolerance
- component and resistor worst case power dissipation
- mechanical dimensions and tolerances for all components including alternates
- pad size and location for all semiconductor devices including alternates
- manufacturer name

• Performance specification and test data

• Thermal analysis

• Individual substrate size and material

• Detail package drawing

• Preliminary pin assignment

• Critical instruction list including:

- critical component placement and spacing
- critical paths — high current, high voltage, and low noise
- assembly instructions for power components
- TCR tracking requirements for resistors
- analog, digital and power ground separation.

4.3.4.1—
General Design Considerations

Prior to discussing thick-film resistor design, we shall review a few general layout considerations.

• Conductor and resistor pattern routing should be oriented in "X" and "Y" axes as shown in Figure 4-12. Resistors, conductors, and mounting pads should be designed with right angle corners and turns. An exception to this rule would be a case, when the mounting pad has to outline an irregular or round component to assist its location on the substrate.

• Package lead to bonding pad alignment. Placing of the exit bonding pads on the substrate strongly depends on wire diameter. Small diameter gold wires can be bonded in close proximity of the package lead. Large diameter aluminum wires require more room to develop a loop. In both cases it is a good practice to locate the bonding pads along the centerline of the pin as shown in Figure 4-13.

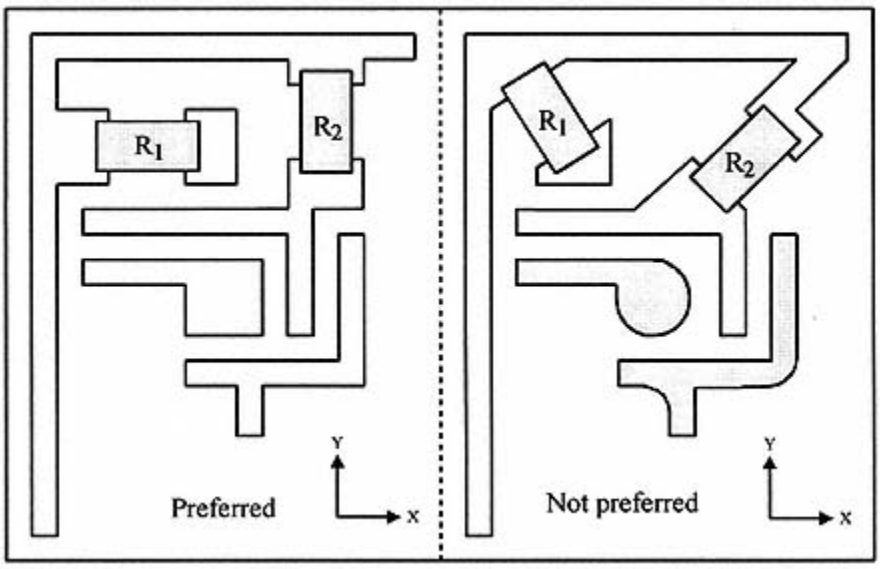


Figure 4-12
Conductor and resistor pattern orientation.

• Wire bonds on the substrate should never be made directly between pads of semiconductor components — diodes, transistors, and ICs as illustrated in Figure 4-14. This rule doesn't apply to large power diodes with top mounted metal tabs.

• Additional probe pads for troubleshooting should be placed in easily accessible locations.

• Keep conductors short and wide as possible.

• Prevent closed resistor - conductor loops as shown in Figure 4-14.

• Minimize use of conductor crossovers and wire bond jumpers.

• Do not allow bonding wires to cross.

• Limit resistor ink number to three if possible. Do not exceed 5 different inks for a single substrate.

• Avoid resistor aspect ratios $5 < A < 0.2$.

4.3.4.2—
Thick-Film Resistor Design

The process of thick-film resistor design starts with specifying the nominal val-

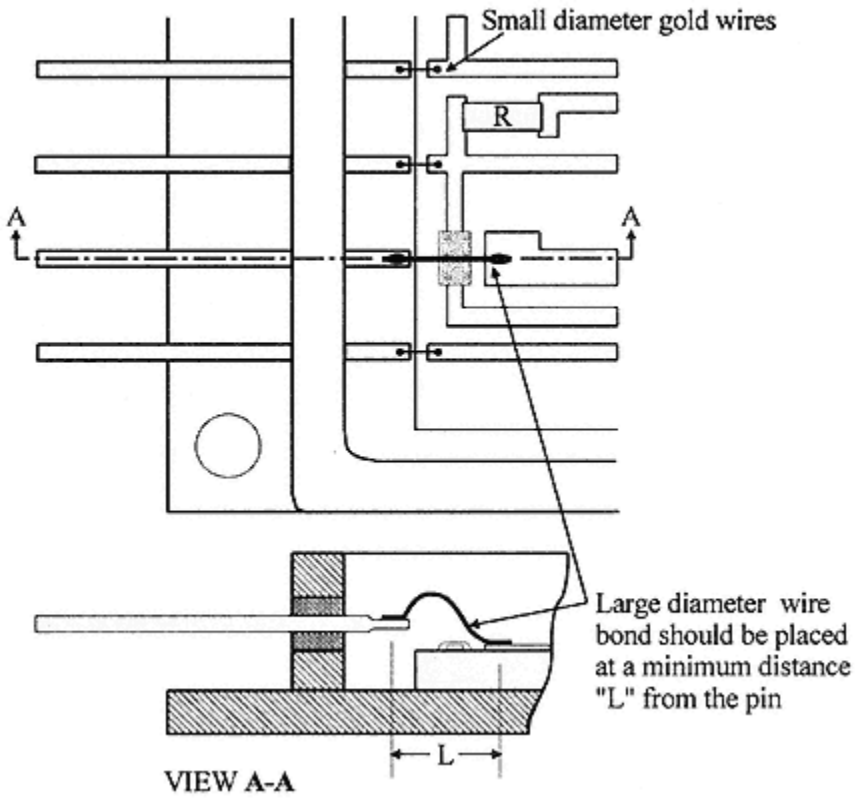


Figure 4-13
Exit bonding pad alignment.

ues, tolerances and performance requirements. This information can be obtained from the released schematic, parts list and the circuit designer. It includes:

• Nominal value

• Tolerance and tracking requirements

• Temperature coefficient of resistance

• Voltage coefficient of resistance

• Maximum continuous power dissipation

Review this information to determine the compatibility of thick-film technology with specified requirements. To assist in further calculations fill in the data in a table as shown in Table 4-2.

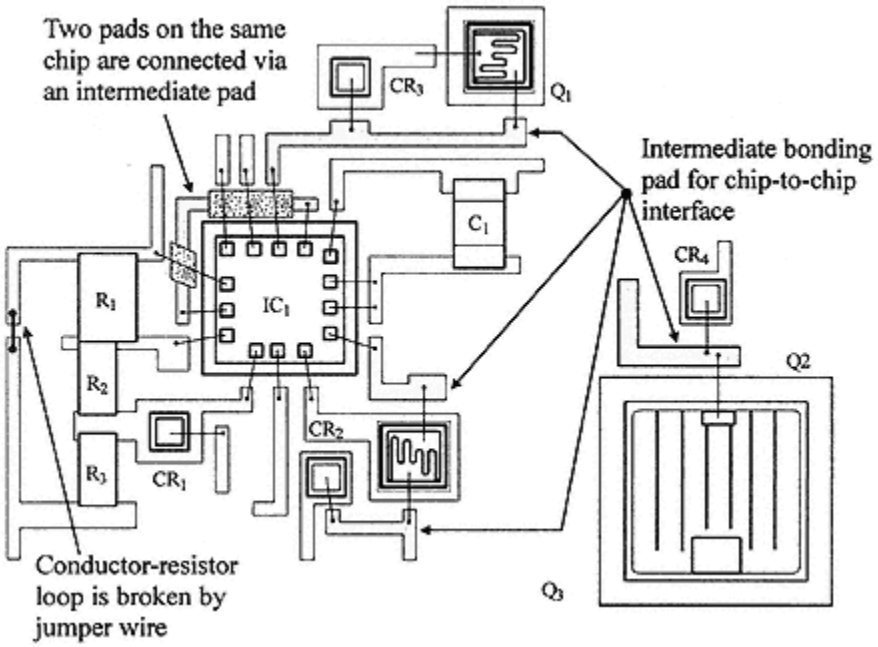


Figure 4-14
Resistor-conductor loop and intermediate bonding pads.

❶ - Resistor reference designator as shown on segment schematic after partitioning
❷ - Nominal resistor value in (Ω)
❸ - Resistor tolerance (± %)
❹ - Temperature coefficient of resistance in (ppm/°C)
❺ - Maximum applied voltage in (*volts*)
❻ - Maximum continuous power dissipation in (*mW*)
❼ - Resistor length in (*mils*)
❽ - Resistor width in (*mils*)
❾ - Sheet resistivity of resistor ink in ohms per square (Ω/□)

Table 4-2 Thick-film resistor design table

❶	❷	❸	❹	❺	❻	❼	❽	❾
✓	✓	✓	✓	✓	✓	✓	✓	✓

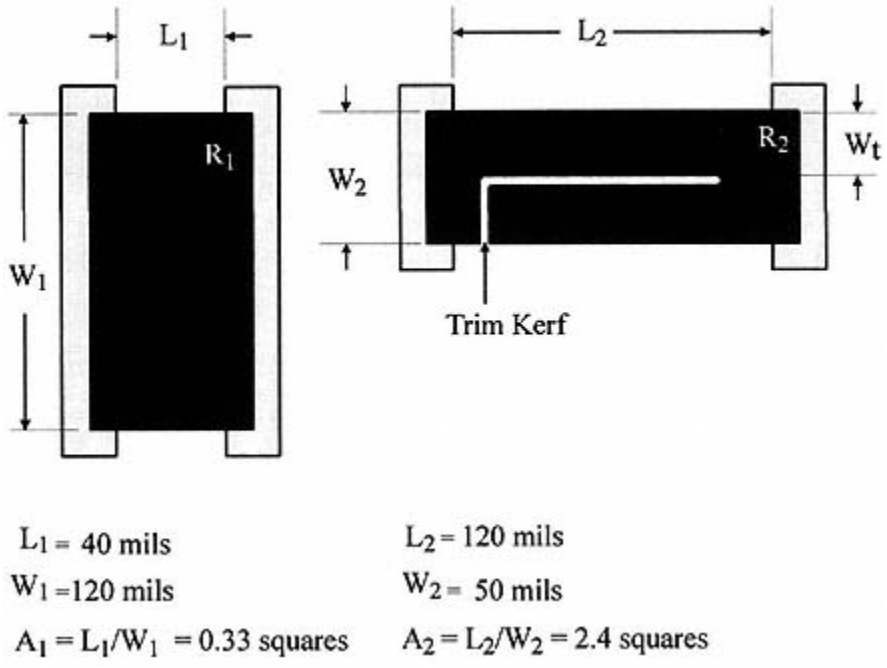


Figure 4-15
Rectangular thick-film resistors.

Items 7, 8, and 9 in Table 4-2 are filled out after resistor design is completed. To simplify the size computations, all resistors should be grouped by value. A single standard resistive ink is selected for each group to meet the following guidelines: the aspect ratio of resistor should be less than 5 and more or equal than 1/5. Design rectangular resistors with minimum width of 0.040" to achieve good stability and producibility. Resistor dimensions in Figure 4-15 define the geometry design parameters: L - resistor length and W - resistor width. The aspect ratio A = L/W allows to determine the number of squares required to yield the specified resistor value. It defines the number of total squares of width W, that can be fit in a length L. Once the resistive ink with a specified sheet resistivity has been selected, the aspect ratio can be also calculated using the formula below:

$$A = \frac{0.75\,R}{R_s}$$

where

A = resistor aspect ratio
R = nominal value of resistor (factor 0.75 is used to design the initial pre-trim value 25% below nominal to allow value increase during trim and compen-

sate for manufacturing deviation)
Rs = sheet resistivity

When the power dissipated in the resistor is negligible (less than 40 milliwatts), the dimensions can be calculated by selecting W = 40 mils for resistors with A > 1 and calculating the length L from

$$L = \frac{0.75\,RW}{R_s}$$

or when A < 1, selecting L = 40 mils and calculating W from

$$W = \frac{LR_s}{0.75\,R}$$

The specified value of working voltage (V/mm) for selected ink must be considered when selecting resistor length L. If the actual voltage across resistor terminals creates electric field larger than maximum allowed in the manufacturers data sheet, the length has to be increased.

When resistor dissipates high power, which is common in power hybrids, its geometry has to be scaled up. Surface area of resistor S = LW depends on the actual power dissipation and can be expressed as

$$S_1 = \frac{P}{P_R}$$

where

S_1 = resistor surface area after trim - area actually dissipating power (in^2)
P = resistor power dissipation in (*watts*)
P_R = rated power density in ($watts/in^2$)

Assuming that it is allowed to remove up to 50% of power resistor width during trimming, as shown in Figure 4-15 ($W_t = 0.5\ W_2$), this expression can be related to the surface area before trim as follows:

$$S = \frac{P}{0.5\,P_R}$$

It is recommended that as a safe design guideline, power rating for thick-film resistors be as follows:

• P_R = 100 w/in^2 for resistors printed on alumina (Al_2O_3) substrate and derated to 50 w/in^2 to provide 100% reliability safety factor

• P_R = 200 w/in^2 for resistors printed on beryllia (BeO) substrate and derated to 100 w/in^2 to provide 100% reliability safety factor

When the resistor value, sheet resistivity of selected ink, and power dissipation are known, the width can be calculated using

The found width value then is used to calculate power resistor length using formula

$$L = \frac{0.75\,RW}{R_s}$$

The rectangular shaped resistors are trimmed to value by narrowing the current path, thus increasing their value. The variation in resistance, that can be achieved using rectangular design may not always be sufficient, when a large resistance change is required during active trimming. During this operation one or several electrical circuit parameters are adjusted by resistance change. A significant dynamic range can be accomplished using a top-hat configuration shown in Figure 4-16.

The resistor is designed similarly to rectangular type, so that as-fired value doesn't exceed the maximum allowed by tolerance. A few constraints will simplify resistor design:

• w_1 - resistor width should be within the range of 0.020" to 0.030" to keep overall resistor size reasonably small

• W - resistor width at the top equals $2w_1$, assuming, that the width of laser cut is negligible

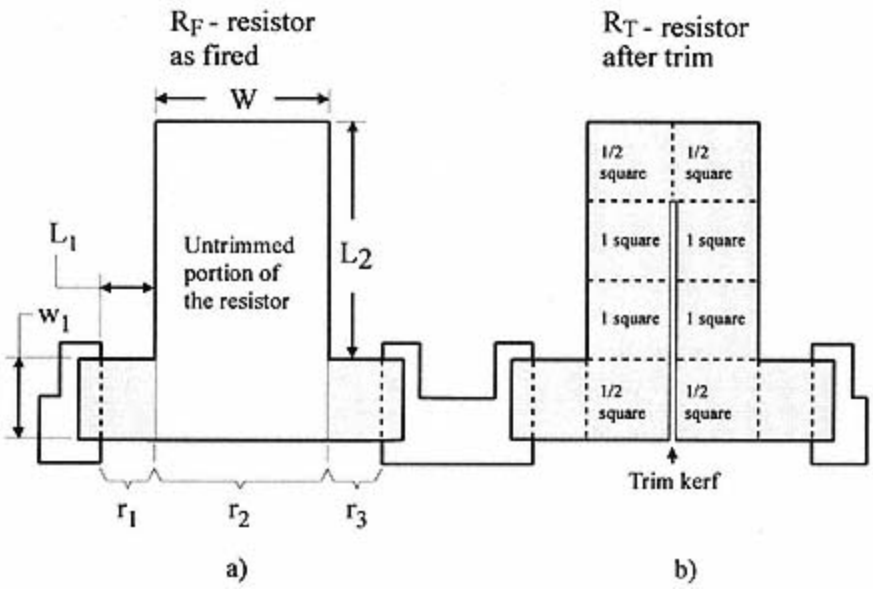


Figure 4-16
Top-hat resistors: a) before trim, b) after trim.

The top-hat resistor design involves calculation of three resistors connected in series - r_1, r_2, and r_3. Two of them - r_1 and r_3 are fixed, and designed equal by making dimensions L_1 and w_1 identical for both. Their dimensions depend on the desirable value of R_F (resistance as-fired). The dimension L_2 shall be determined by the target trimmed value (R_T). Several design parameters are selected or known at the start:

- w_1 = resistor width
- $W = 2w_1$ - width at the top
- R_T = target trim value equal to the nominal with specified tolerances
- R_F = as-fired resistor value. It is specified as a starting value R_0, when a dynamic trim in a range is performed.

Use the following formula to determine R_F, to allow for manufacturing deviation of 25%:

$$R_F = 0.75\ R_0$$

If the dynamic trim is not required, and the top-hat resistor configuration was selected to minimize the number of inks used on the substrate, then

$$R_F = 0.75\ R_T$$

Number of squares in resistor r_1

$$A_1 = \frac{L_1}{w_1}$$

Number of squares in resistor r_2 before trim is

$$A_2 \cong 1.8$$

Number of squares in resistor r_3

$$A_3 = \frac{L_1}{w_1}$$

The total number of squares in the resistor as fired

where R_s is the sheet resistivity of the selected paste.

Also

Solving for L_1 gives

$L_1 = 0.5\ w_1\ (A_F - 1.8)$

After trim to target value

$R_T = r_1 + r_2 + r_3$

where

r_2 - value of resistor r_2 after trim as shown in Figure 4-16b. Notice that each corner is equal to ½ square.

The number of squares in resistor r_2

$$A_2' = \frac{2(L_2 + w_1)}{w_1} - 2 = \frac{2L_2}{w_1}$$

Total number of squares in resistor R_T

$$A_T = A_1 + A_2' + A_3 = \frac{2(L_1 + L_2)}{w_1}$$

and also

$$A_T = \frac{R_T}{R_s}$$

Solving for L_2 gives

$$L_2 = \frac{1}{2} w_1 A_T - L_1$$

Top-hat configuration is also used to minimize number of resistive inks per substrate. It is accomplished by designing a high value thick-film resistor using material with low sheet resistivity. Considering that a large range of dynamic resistance change is not required, the laser trimming is minimized. The resistor design is to final value only. In this case resistance as fired $R_F = 0.75\ R_T$. Other configurations and trimming options are shown in Figure 4-17.

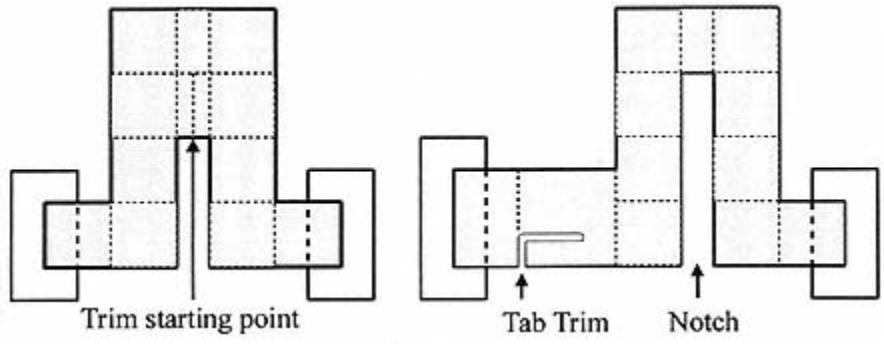


Figure 4-17
Optional geometries of top-hat resistors.

Analogous to rectangular design, the dimensions of top-hat resistors should be calculated with regards to dissipated power. Similar criteria applies to maximum power density – P_r = 50 w/in^2. Referring to Figure 4-16a, the total power dissipation in the trimmed resistor is equal to

$$P_D = P_r A_T w_1^2$$

where

P_D = total continuous power dissipation in the resistor in (*watts*)
P_r = rated power density (defined as 50 watts/in^2 for alumina substrates)
A_T = total number of squares also equal to $R_T R_S$
w_1 = resistor width
R_T = resistor value after trim
R_S = sheet resistivity of ink

Substituting for A_T and solving for w_1 gives

$$w_1 = \sqrt{\frac{P_D R_S}{P_r R_T}}$$

This formula is used to determine the resistor width based on power dissipation, resistance value, and sheet resistivity. Power dissipation in the resistor is $P_D = I^2 R_T$, where I is the resistor current. Substituting for P_D we get

$$w_1 = I\sqrt{\frac{R_S}{P_r}}$$

This formula can be rewritten to express the maximum allowable current per unit width

$$\frac{I}{w_1} = \sqrt{\frac{P_r}{R_S}}$$

Consequently, the maximum current handling capability is

$$\frac{I}{w_1} = \sqrt{\frac{50}{R_S}}$$

for alumina substrate and

for the beryllia.

Certain applications of power hybrids require use of a very low value resistors for high current sensing. Resistor values range from 0.025 Ω to 0.2 Ω. Two major specification parameters determine the technique of implementation:

- Resistor tolerance
- Thermal coefficient of resistance

Table 4-3 Physical and mechanical properties of copper-nickel alloys

Property	Typical range	Units
Chemical composition:		
Cu	27 – 55	
Ni	29 – 63	%
Other	Remainder	
Tensile strength	50 – 63	kpsi
Yield strength	20 – 35	kpsi
Elongation	32 – 50	%
Density	0.320	lb/in^3
Curie temperature	20 – 50	℃
Specific heat	380 – 427	J/kg · °C
Melting range	1170 – 1350	℃
Thermal conductivity	19.2 – 29.4	w/m · °C
Thermal coefficient of expansion, 21 – 93°C	13.7 – 14.7	µm/m · °C
Electrical resistivity	0.412 – 0.547	µΩ · m
Thermal coefficient of resistance, 25 – 150°C	30 – 36	µΩ/Ω ·°C

When resistor tolerance is larger than 1% and TCR is less than 200 ppm/°C, use of solid wire or ribbon is preferred. Table 4-3 lists typical performance specifications of copper-nickel alloys used in manufacturing of wire-wound discrete resistors. This wire can be attached to metal pads by means of welding, brazing or soldering. Large currents flowing in the wire dissipate ample amount of power, which converts to heat and must be removed for safe operation of the resistor. For example, current I = 20 amperes flowing in a resistor R = 50 mΩ shall result in power dissipation $P_D = I^2R = 20$ watts. Use of encapsulant with high thermal conductivity creates a thermal path from resistor wire through the substrate to the outside heatsink. To achieve a desired resistor value wire diame-

ter, material resistivity and length are adjusted. Wire or ribbon resistance is calculated using

$$R = \rho \frac{L}{S}$$

where

R = resistance in (Ω)
ρ = electrical resistivity in (μΩ · m)
L = wire or ribbon length
S = wire or ribbon cross-sectional area

When a lower resistance value is required, several segments of the wire or ribbon are connected in parallel. Lack of space in power hybrids leads to small dimensions of power resistor. This results in short wires with low resistivity. For example, a single wire with $\rho = 0.547\ \mu\Omega \cdot m$ which is 0.1 inches long with diameter of 0.01 inch shall exhibit resistance of R = 28 mΩ. To raise the resistor value, the wire can be wound around an electrically insulating object to increase the wire length. Tight tolerance is another difficult feature to obtain using wires. However, the resistor can be calibrated in the circuit, using 4-point measurement technique at known current.

For power resistors that do not require very low TCR, thick-film technology can be used. Resistive paste materials are available with sheet resistivities as low as 0.1 Ω/□ and TCR less than 400 ppm/°C. One of the geometrical configurations used to achieve low value thick-film power resistors is shown in Figure 4-18a. The total number of resistors connected in parallel can vary and depends on the desired value. The resulting resistance can be calculated from

$$\frac{1}{R} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \frac{1}{R_4} + \frac{1}{R_5} + \frac{1}{R_6}$$

Caution has to be exercised during trimming. If one of the resistors in the chain is overtrimmed, it will dissipate most of the power and may be destroyed. The best approach would be to trim a few resistors to a lesser extent.

Low value power resistors are frequently used to sense high current flowing in the circuit. Thick-film resistor is connected in series with conductors which exhibit TCR values 5 to 10 times that of the resistor. Two taps are used to maintain the sensing accuracy of voltage drop across the resistor, as shown in Figure 4-18b. The voltage is measured by a device with high input impedance via these taps that are connected to resistor body outside of the main current flow path. Two additional locations must be identified for application of high current during 4-point resistor trimming operation. During the trimming operation the high current is passed through the resistor to develop a stable voltage drop. This voltage is measured at the taps to determine resistor value.

Recommended dimensional constraints for thick-film resistors are listed in Table 4-4 with reference to illustrations in Figure 4-19.

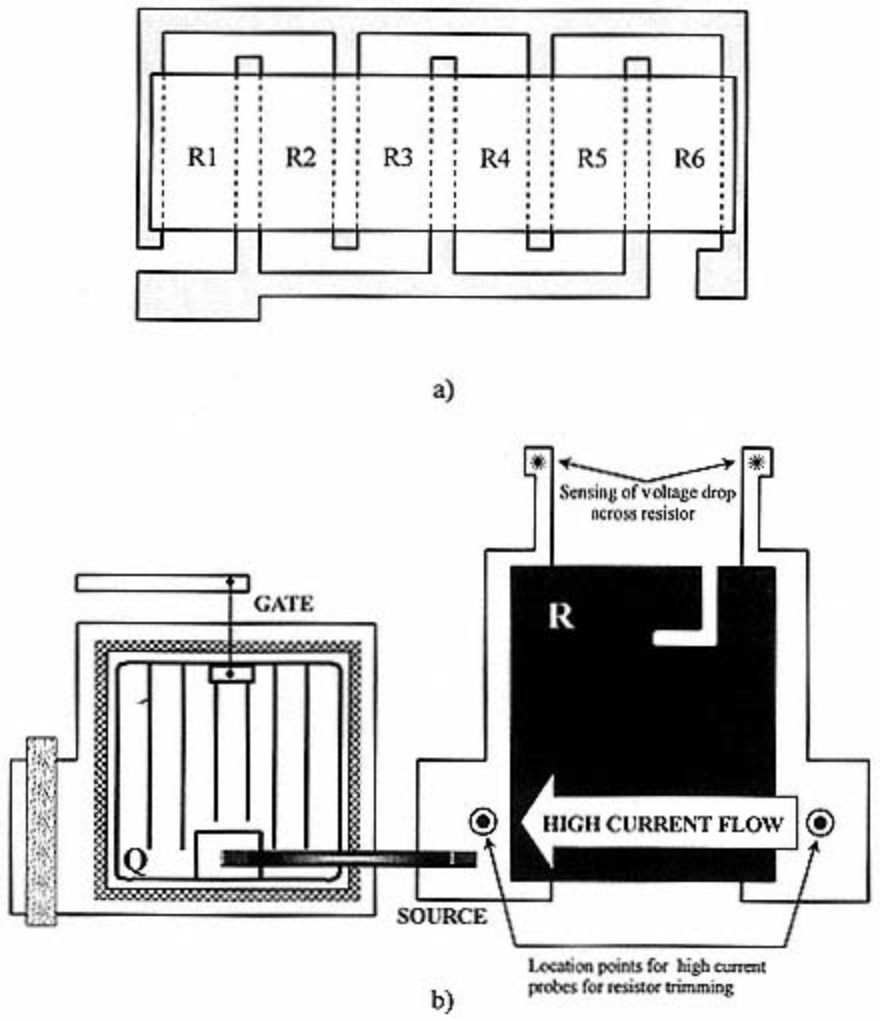


Figure 4-18
Low value thick-film power resistors: a) parallel connection of six resistors,
b) 4-point probing of low value sense resistor.

4.3.4.3— Conductors and Pads

There is more than one way to design a hybrid circuit layout. The guidelines and constraints presented in this book are based on my experience and are optimized

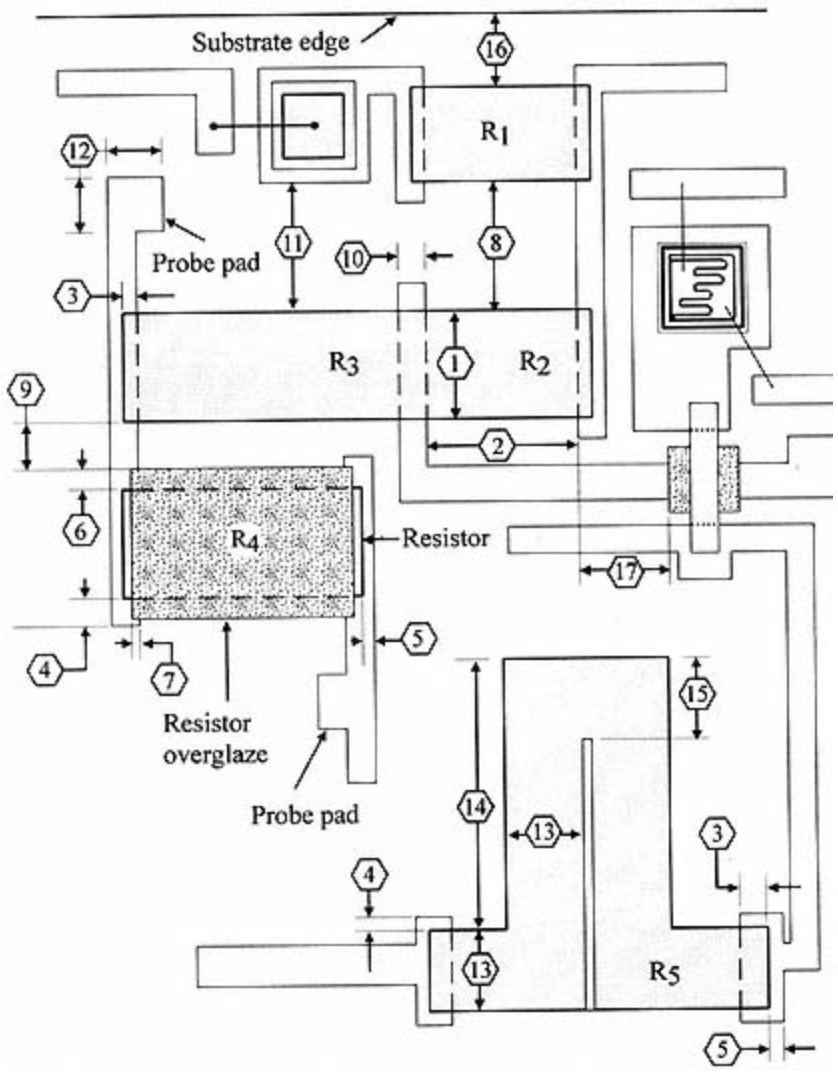


Figure 4-19
Thick-film resistor layout, dimensions and constraints.

for performance, manufacturability, and reliability of power hybrids.

This paragraph reviews guidelines for conductors and pads for component mounting or wire bonding. Epoxy attach is reviewed separately from solder attach. Individual guidelines are provided for gold ball bonding and wedge – wedge ultrasonic bonding of aluminum wires. Dimensional constraints for exit

Table 4-4 Design dimensions and constraints for laser trimmed resistors

Fig. 4-19 (Ref.)	Description	Dimensions (inch)		
		min	nom	max
1	Rectangular resistor width	0.2 < A < 5		
2	Rectangular resistor length	0.2 < A < 5		
	Resistor — conductor overlap			
3	- low power	.010	.015	
	- high power	.015	.020	
4	Resistor-to-conductor edge spacing (width)	.005	.10	
5	Resistor-to-conductor edge spacing (length)	.005	.010	
6	Resistor — overglaze overlap (width)	.005	.010	
7	Resistor — overglaze overlap (length)	.005	.010	
	Resistor-to-resistor spacing on trimmed side			
8	- low power	.020	.040	
	- high power	.040	.060	
	Resistor-to-resistor spacing on untrimmed side			
9	- low power	.010	.020	
	- high power	.040	.060	
10	Resistor center-tap	.010	.015	
11	Resistor-to-mounting pad spacing	.020	.030	
12	Resistor probe pad (length & width)	.015	.020	
13	Resistor top-hat width	.020	.030	
14	Resistor top-hat height	.050		.500

15	Resistor top-hat trim depth	.020		
16	Resistor-to-substrate edge spacing	.030	.050	
17	Resistor-to-dielectric spacing	.025	.030	

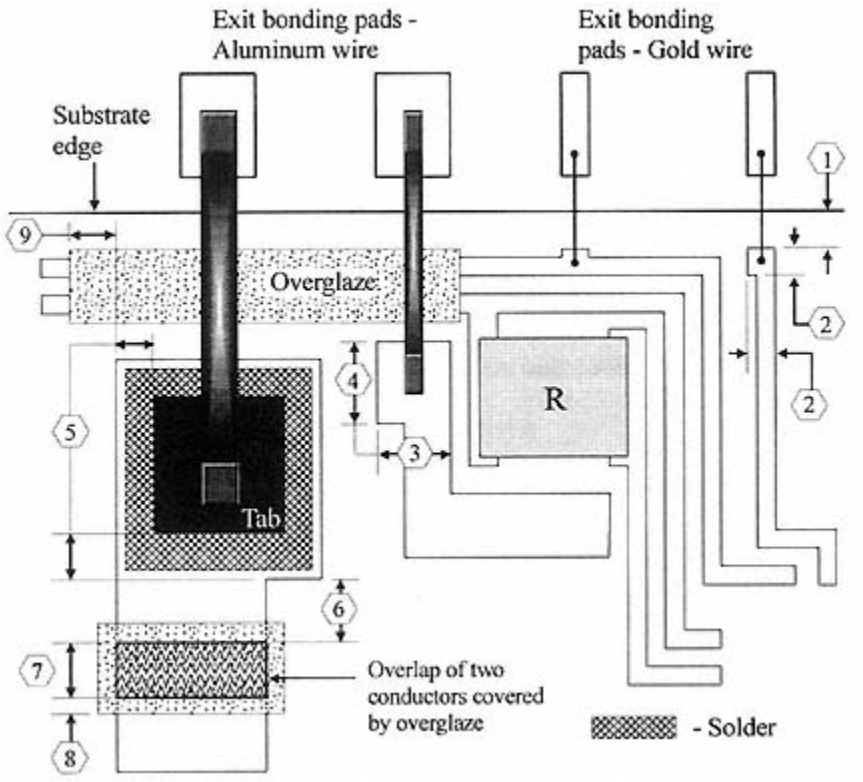


Figure 4-20
Exit bonding pads, dimensional constraints.

pads bonded with gold and aluminum wires are described in Figure 4-20 and detailed in Table 4-5. Two types of connections are used for attachments of aluminum wires. First, on the left, is bonded to a metal tab which is soldered to a conductor using paste or preform. The tab dimensions depend on wire diameter and are selected using guidelines for bonding pads in Table 4-5. The solder pad for tab mounting extends beyond tab by dimension 5 in Figure 4-20. The solderable part of the conductor may be overlapped with gold conductor as shown in the figure and covered with overglaze. Bare conductors running under wire-bonds or near solder sites are covered with glass and extend beyond solder pad by length 9 in Figure 4-20.

Power hybrids are constructed in a variety of configurations, which may require that separate partitioned segments are implemented using conventional low power technology on a separate substrate. It may be also necessary, that some of the low power circuit elements would be assembled in a close proximity to power devices to achieve better electrical or thermal coupling. In this case the

Table 4-5 Dimensions and constraints for exit bonding pads

Fig. 4-20 (Ref.)	Description	Dimensions (inch) min	nom	max
1	Bonding pad to substrate edge spacing	0.010	0.020	
2	Exit bonding pad (gold wire) length/width			
	0.001" Dia	0.010	0.015	
	0.002" Dia	0.015	0.020	
3	Thick-film conductor exit bonding pad width (aluminum wire)			
	0.008" Dia	0.015	0.025	
	0.010" Dia	0.025	0.035	
	0.012" Dia	0.030	0.050	
	0.015" Dia	0.040	0.065	
	0.018" Dia	0.045	0.075	
	0.020" Dia	0.050	0.080	
	0.025" Dia	0.065	0.100	
4	Thick-film conductor exit bonding pad length (aluminum wire)			
	.008" Dia	0.040	0.050	
	.010" Dia	0.050	0.060	
	.012" Dia	0.060	0.080	
	.015" Dia	0.075	0.100	
	.018" Dia	0.090	0.120	
	.020" Dia	0.100	0.130	
	.025" Dia	0.125	0.160	
5	Soldered tab to conductor pad spacing, length/width	0.020	0.040	
6	Solder pad to two conductor overlap spacing	0.030	0.040	
7	Two conductor overlap	0.025	0.040	
8	Overglaze beyond conductor overlap	0.005	0.010	
9	Overglaze beyond solder pad	0.020	0.040	

assembly shall be done on the same substrate. Dimensional constraints and guidelines of Table 4-6 and Figure 4-21 relate to low power subassembly where chips are attached to the substrate using conductive and nonconductive adhesives and interconnected with gold wires. Dimension 1 is necessary to facilitate chip placement and is added to the maximum chip size specified by the manufacturer.

When a wire crosses bare conductor, glass is printed over it to prevent a possibility of short circuit by sagging or pushed down wire, as for IC pad 5. Running transit conductors between terminals of chip capacitors can significantly simplify layout design. To prevent accidental shorts by adhesives between capacitor terminations and transit conductor, glass insulator is printed over it. The distance between the conductor and termination pad is shown in Figure 4-21 as dimension 10. This technique may be prohibitive when high voltage potential exists between conductor and pads or across the capacitor, and should be reviewed and approved by the circuit designer.

Figure 4-21b demonstrates the process of ball bonding. There are two ball-wedge bonding techniques — thermocompression and thermosonic. A thermocompression bond starts with ball formation by hydrogen torch or electronic flame-off which melts the wire as shown in Figure 4-21b (1,6). The surface tension of molten wire pulls the metal into spherical shape. The wire area adjacent to the ball undergoes a process of recrystallization. The recrystallized grains in the ball and adjacent wire have much lower yield stress and are easily deformed under pressure of the capillary (Fig. 4-21b (2)) when the ball bond is made. Then the capillary is positioned over the second bond pad (Fig. 4-21b (3)) and the second bond is made by the tool's wedge (Fig. 4-21b (4)). Three major parameters directly relate to the thermocompression bond kinetics – temperature of bond interface, dwell time, and degree of deformation. The temperature is controlled by preheating the work stage with the hybrid and the capillary. The typical temperatures vary from 250°C to 350°C. Dwell time is defined as the time interval from application of compression force until removal of the heat source. The degree of deformation of wire depends on the magnitude of compression force and degree of annealing of wire.

Thermosonic bonding is similar to thermocompression and is performed at lower temperatures. Bonding starts with ball bond at the first site and ends with the wedge bond (stitch). During bonding a burst of ultrasonic vibrations is applied through the capillary. Use of ultrasonic energy allows to maintain the work stage at temperatures between 125°C and 150°C.

To accommodate multiple source requirement for die procurement, the designer frequently has to deal with chips that vary in bonding pad placement and length/width dimensions. The mounting pad is designed for worst case length/width and maximum dimensions of both chips as shown in Figure 4-22. During assembly the chip is mounted approximately in the center of the pad to avoid very long wires on one or two sides.

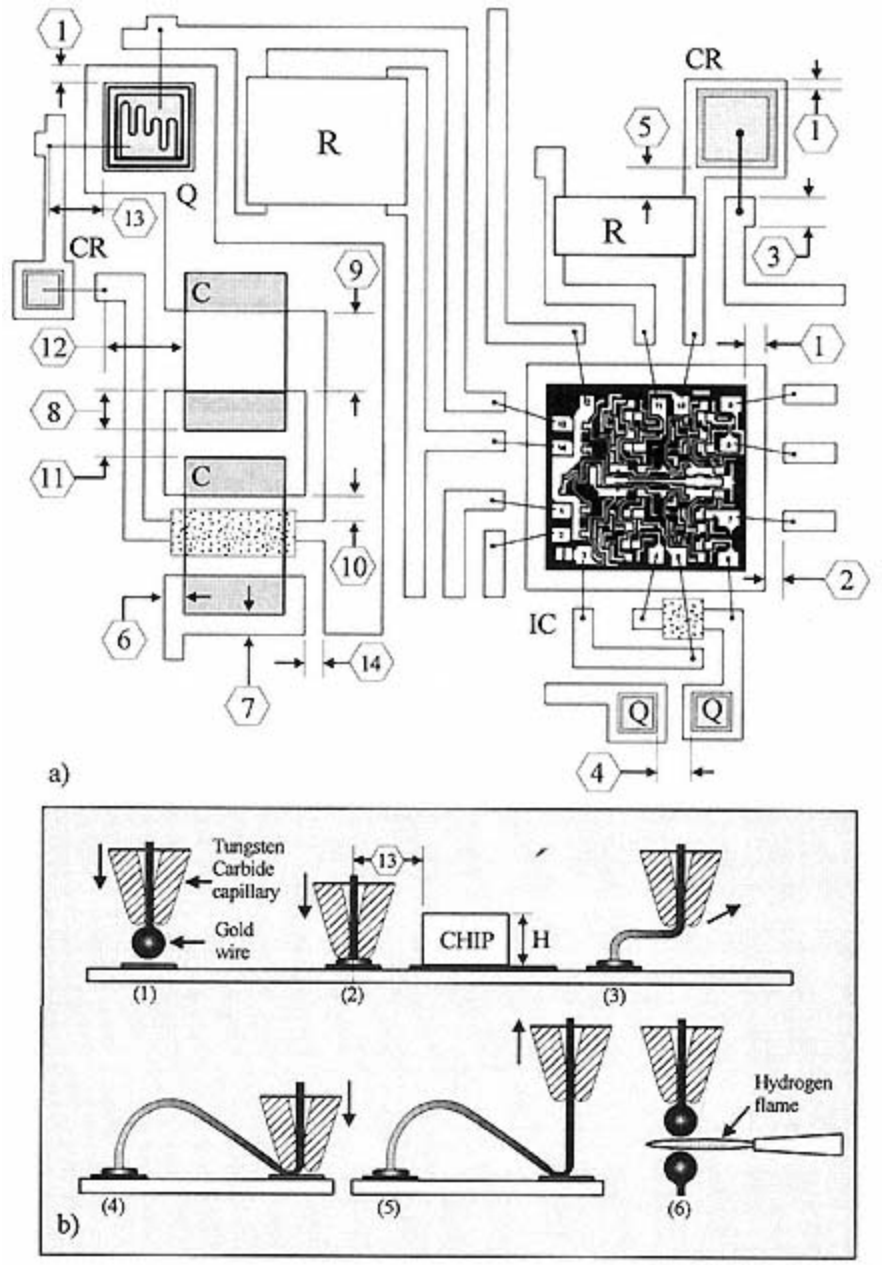


Figure 4-21
Dimensional constraints for the epoxy die attach and gold wire ball bonding.

Table 4-6 Design dimensions and constraints for epoxy attach and ball bonding of gold wire

Fig. 4-21 (Ref.)	Description	Dimensions (inch) min	nom	max
1	Mounting pad-to-die spacing (all around)	0.005	0.010	
2	Mounting pad-to-wire-bonding pad spacing	0.010		
3	Wire-bonding pad (gold wire), length/width			
	0.001" Dia	0.010	0.015	
	0.002" Dia	0.015	0.020	
4	Die-to-die spacing chip size < 0.030"	0.020		
	chip size > 0.030"	larger die size		
5	Die-to-resistor spacing	0.015	0.020	
6	Capacitor-to-conductor spacing, width	0.005	0.010	
7	Capacitor-to-conductor spacing, length	0.015	0.020	
8	Capacitor — pad overlap	0.010	0.020	
9	Capacitor mounting pad spacing	See Table 4-8		
10	Capacitor pad to conductor spacing when:			
	conductor is covered with overglaze	0.010	0.020	
	conductor is not covered with overglaze	0.025	0.040	
11	Capacitor to capacitor spacing	0.030	0.040	
12	Capacitor to wire-bond spacing	0.035	0.045	
13	Chip edge to bond site (see Fig. 4-21b)			
	Thermosonic ball bonding (the larger of)	0.020 or 2 H		
	Thermocompression (the larger of)	0.015 or 0.5 H		
14	Mounting pad to conductor spacing for ceramic capacitors:			
	smaller or equal than type 1210	0.010	0.015	
	larger than type 1210	0.015	0.020	

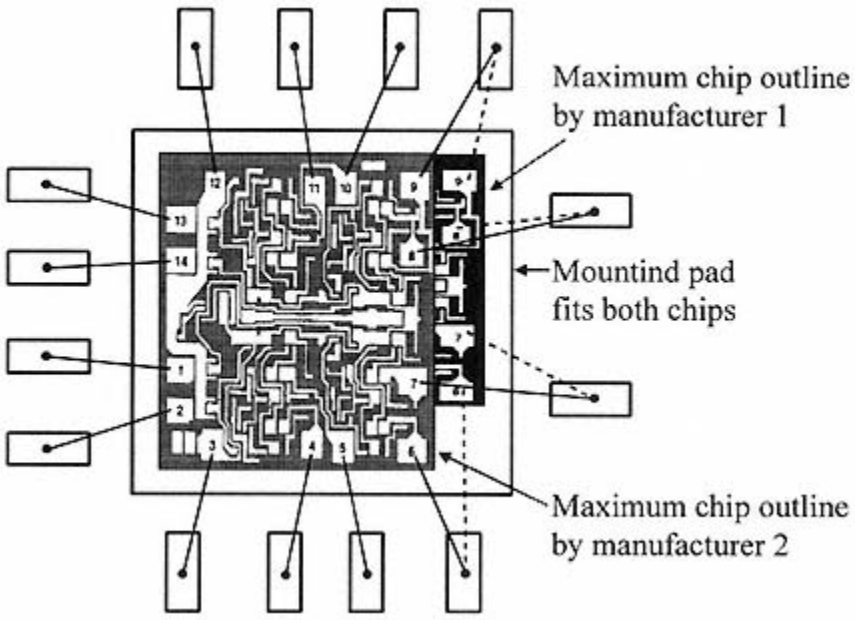


Figure 4-22
Mounting pad design for alternate chip geometries.

It is common for power subassemblies to feature solder attach of semiconductor and passive components to the substrate, where large diameter aluminum wires are used for interconnections conducting large currents. Other components, such as inductors and transformers are frequently used in hybrids designed for power conversion equipment. They have large diameter copper wire leads, which are welded or soldered to conductors or tabs. The equivalent series resistance of capacitors (ESR) can be seriously impacted by epoxy attach. It is influenced by serious conductor resistance and contact resistance. To reduce the contact resistance, capacitors are soldered to the conductors instead of using conductive adhesives. Conductors are designed wide and short, using thick-film materials exhibiting lowest resistivity. Direct bonded copper is used to achieve best performance in conducting high currents and minimizing losses.

Dimensional constraints for solder attach in power hybrids are shown in Figure 4-23 and defined in Table 4-7. Capacitor pad sizes and spacing are designed using dimensions shown in Table 4-8. It is rather difficult to attach large diameter copper wire from inductor or transformer to the pad on ceramic substrate.

Usually, the magnetic component is first mounted with nonconductive adhesive. Then the leads are positioned in place and fixed using nonconductive adhe-

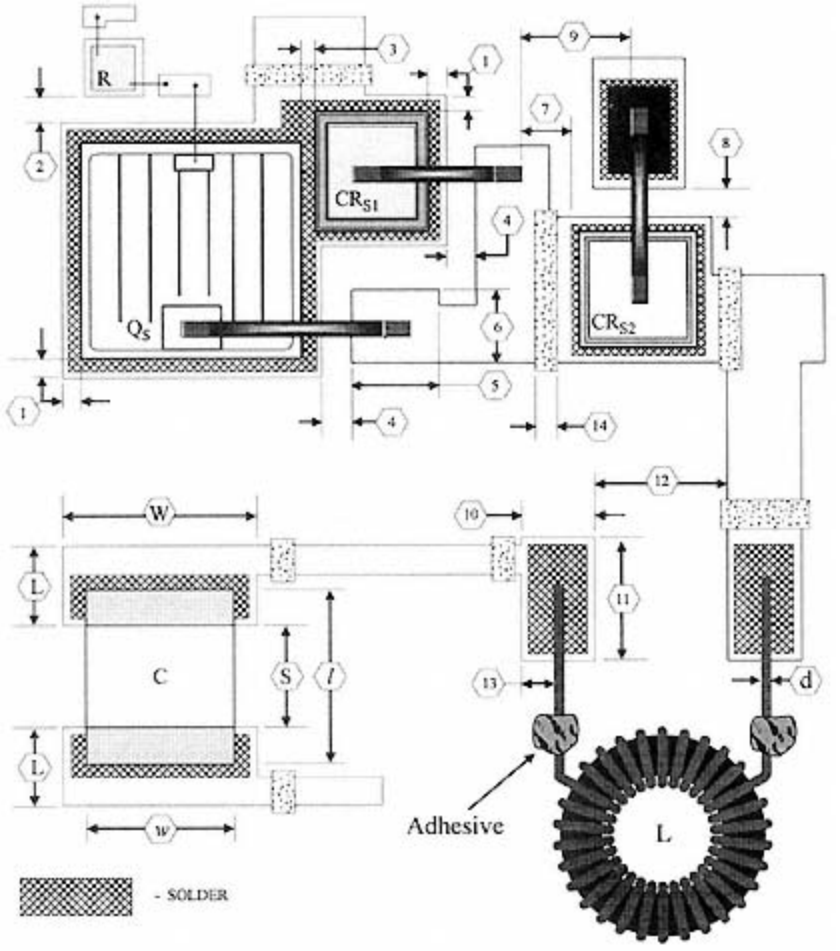


Figure 4-23
Solder attach of components, dimensional constraints.

sive also. After curing of epoxy the leads are soldered to the pads as shown in Figure 4-23. A glass dam is printed next to the solder pads to prevent solder spreading beyond the pad outline causing damage to gold conductors or contaminating bonding sites. It is recommended to increase the distance between wire-bonding and solder pads when using solder paste, rather than a solder preform. Large diameter wire-bonds are made preferably along a straight line in the direction from front-to-back. The first bond is made on the semiconductor pad and the second on the conductor. When wiring the package pins, the first bond is made

Table 4-7 Dimensions and constraints for power components attached with solder and bonded with aluminum wire

Fig. 4-23 (Ref.)	Description	Dimensions (inch) min	nom	max
1	Die-to-conductor pad spacing	0.020	0.040	
2	Solder mount pad-to-conductor spacing	0.030	0.040	
3	Soldered chip-to-chip spacing (use thermal analysis to determine the placement of power dissipating components)	0.040		
4	Solder pad-to-wire-bond spacing	0.030	0.040	
5	Wire-bond pad (aluminum wire), length	See Table 4-4		
6	Wire-bond pad (aluminum wire), width	See Table 4-4		
7	Wire-bond-to-solder spacing, same pad	0.040	0.060	
8	Solder pad-to-solder pad spacing	0.030	0.040	
9	Wire-bond-to-wire-bond spacing	See Figure 4-24		
10	Wire solder pad width	2d	4d	
11	Wire solder pad length	4d	6d	
12	Wire solder pad spacing	0.040	0.080	
13	Solder pad-to-wire spacing	0.5d	1.5d	
14	Solder dam glass width	0.020	0.040	
	Capacitor mounting pad size and spacing. Dimensions: W, L, *w, l*, and S	See Table 4-8		

on the pin and the second on the substrate pad. Solder pad size is determined using dimension 1 in Table 4 and the maximum chip dimensions specified by the manufacturer. Selection of bonding wire diameter for MOSFET or IGBT gate terminal must consider large peak currents flowing into the gate during capacitor

Table 4-8 Dimensional constraints for solder attach of multilayer ceramic chip capacitors (MLCC). Reference illustration in Figure 4-23.

Capacitor type	Capacitor dimensions		Solder pad dimensions		
	l (inches)	*w* (inches)	L (inches)	W (inches)	S (inches)
0805	0.080 ± .015	0.050 ± .015	0.060	0.065	0.035
1206	0.126 ± .015	0.063 ± .015	0.040	0.080	0.070
1210	0.126 ± .015	0.098 ± .015	0.040	0.115	0.070
1805	0.180 ± .015	0.050 ± .015	0.050	0.065	0.120
1808	0.180 ± .015	0.080 ± .015	0.050	0.095	0.120
1812	0.180 ± .015	0.125 ± .015	0.050	0.140	0.120
1825	0.180 ± .020	0.250 ± .020	0.050	0.270	0.120
2225	0.225 ± .020	0.250 ± .020	0.050	0.270	0.170
3640	0.360 ± .020	0.400 ± .020	0.060	0.420	0.300

charging. Multiple 0.001" diameter gold wires or larger aluminum wire may be used for that purpose.

Design of power hybrid layout for ultrasonic wedge-wedge bonding of large diameter aluminum wire requires understanding of main operating parameters of equipment. The configuration of Orthodyne semiautomatic ultrasonic wire bonder Model 20 shown in Figure 4-24 is used to illustrate the bonding process. Schematically, the bonder is depicted in Figure 4-25. The bonding operation is performed in a step back motion. The wire is fed to the right groove on the bonding tool. Bursts of ultrasonic energy produced by a generator with adjustable output power and time, are transmitted to the tip of the bonding tool. The common operating frequency is 60 kHz, with bond duration adjustable between 0 ms and 500 ms, with 30 ms prebond delay. The bonding tool is pressing on the wire with force sufficient to hold it in place without moving across pad surface. The wire is ultrasonically softened by the tool's wedge motion and is flowed by the vertical load. The wire flow and deformation breaks-up surface oxides and pushes contaminants sideways, exposing clean metal surfaces for metallurgical weld. Excessive vertical force may stall wedge's movements along the wire, while insufficient load will cause wedge to bounce and produce poor bond. Absorption of ultrasonic energy results in temperature rise at the bond site to values well

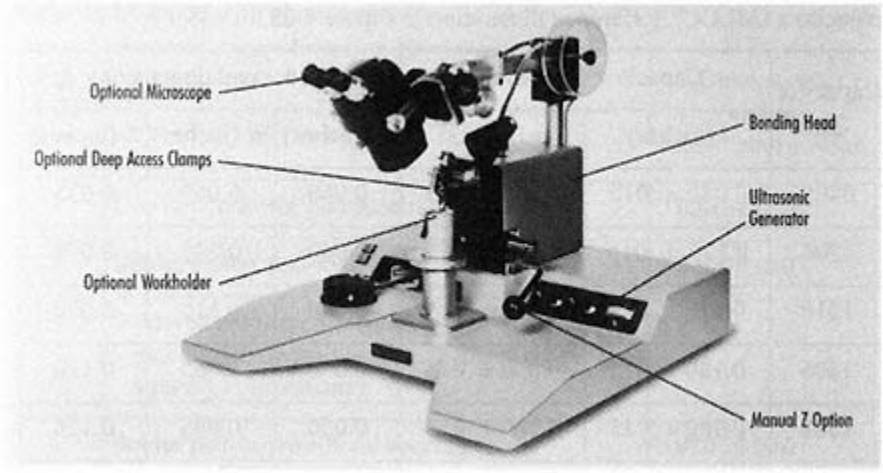


Figure 4-24
Orthodyne Model 20 ultrasonic large diameter wire bonder.
Photo courtesy of Orthodyne Electronics.

above 100°C. After formation of the first bond, the tool forms a loop to the second bond site and positions the wire in the left groove with a cutoff chisel. The wire is cut after the second bond is made. The manual bonder Model 20 has a limited access inside power hybrid package. The bonding tool access window is shown by dotted line and is limited in length to approximately 1.5" at a depth of 0.350". There is no limitation when bonding depth is 0.100".

Wire-bond sequence is always selected with the first bond on a semiconductor chip pad and the second on the substrate conductor or tab. Similarly, the package leads are also bonded firs.

Ultrasonic wire bonders can provide interconnections with wire diameter up to 0.025". High frequency and high current applications often require that a few parallel large diameter wires are connected in parallel to reduce wire temperature, conduction losses and inductance. Figure 4- 26 describes wire-bond foot-

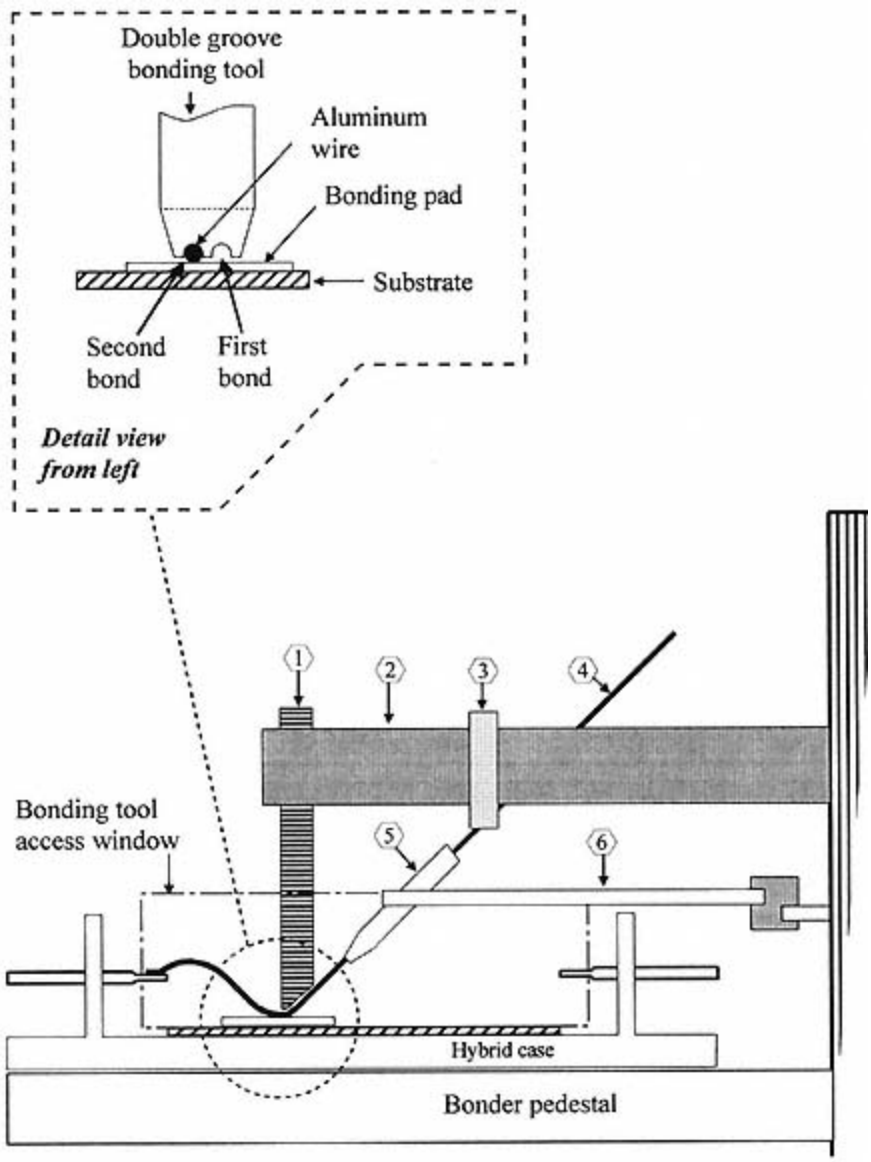


Figure 4-25
Ultrasonic wedge-wedge bonding of large diameter aluminum wire: 1–bonding tool, 2–transducer, 3–wire clamps, 4–aluminum wire, 5–wire feed capillary, and 6–wire shifter.

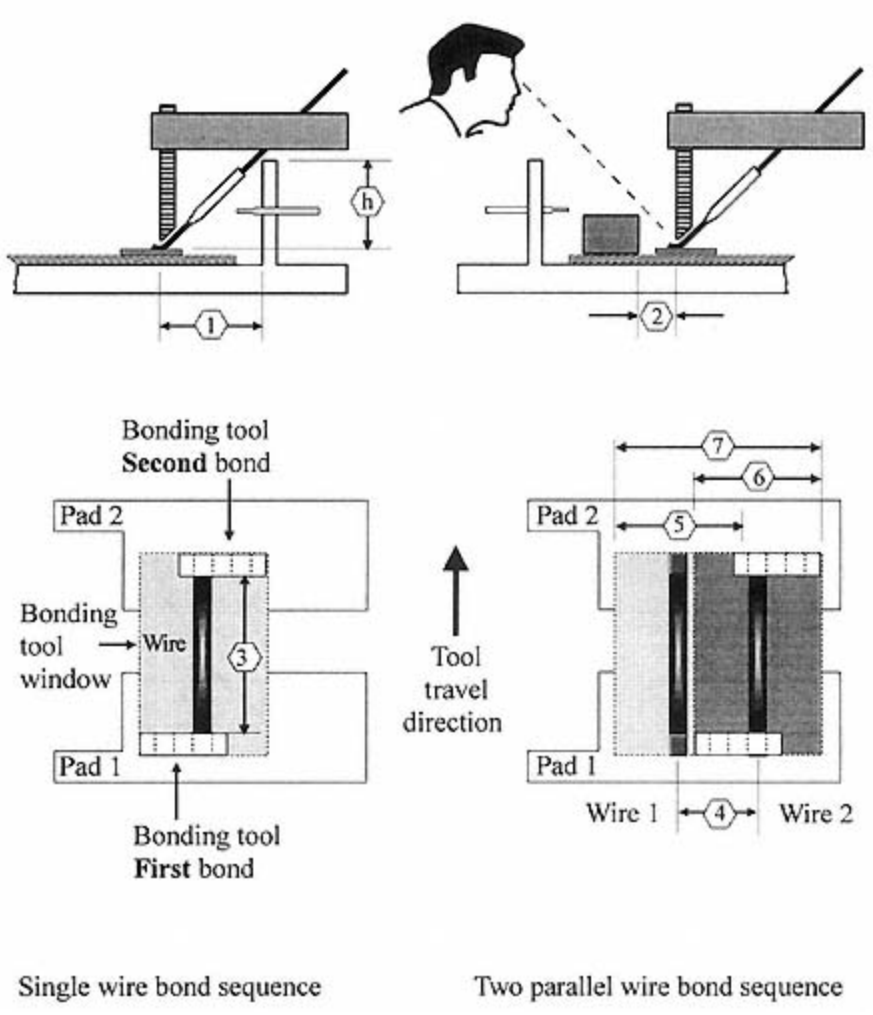


Figure 4-26
Aluminum wire footprint dimensional constraints.

print design parameters for parallel wires, which are specified in Table 4-9.

Wires can be positioned much closer than shown in the table, if bonding sites are staggered and the wire 2 is bonded first. However that will require a longer bonding pad. Use of other ultrasonic bonding machines may require a change of layout design parameters. A designer with the help of a processing engineer can develop a set of customized design parameters using manufacturers data and guidelines outlined in this chapter.

Table 4-9 Dimensional constraints for wedge-wedge wire-bond footprint

Fig. 4-26 (Ref.)	Description	Dimensions (inch) min	nom	max
1	Bonding tool to wall spacing when:			
	0.100" < h < 0.150"	0.250		
	0.150" < h < 0.200"	0.300		
	0.200" < h < 0.250"	0.350		
2	Bonding tool to component spacing (front)	0.020		
3	Wire-bond length for wire diameter:			
	0.004" to 0.008"	0.050	0.075	
	0.010" to 0.015"	0.100	0.150	
	0.018" to 0.020"	0.150	0.200	
	0.025"	0.200	0.300	
4	Spacing of two parallel identical wire-bonds			
	0.008"	0.040		
	0.010"	0.045		
	0.012"	0.050		
	0.015"	0.060		
	0.018"	0.070		
	0.020"	0.080		
	0.025"	0.095		
5, 6	Single wire bonding tool window width (all wires)	0.160		
7	Two identical parallel wire bonding tool window width			
	0.008"	0.195		
	0.010"	0.200		
	0.012"	0.205		
	0.015"	0.215		
	0.018"	0.225		
	0.020"	0.235		

	0.025"	0.250		

4.3.5— Detail Documentation

Manufacturing and procurement documentation can be generated manually or using computer aided design software. The layout drawing is created by transforming a symbolic electrical schematic into component placement and interconnections in accordance with the guidelines outlined in the previous chapter and summarized in Table 4-1 through Table 4-9. After completion of preliminary layout it is reviewed and modified if necessary.

4.3.5.1— Final Layout

The final layout depicts the power hybrid microcircuit as it will appear after assembly of all components on ceramic substrates with screened-on thick-film resistors, and interconnected using wire-bonds. Each component and resistor is identified by a symbol with marked numerical or alphanumerical description of bonding pads as defined on the schematic drawing. The complete drawn assembly is then placed into the package and wired to the I/O leads. Placement of large components and large diameter wire-bonds is accurately shown to assist in final layout analysis. Final layout incorporates all changes documented during preliminary layout design review. It is based on final versions of the schematic drawing, package drawing, bill of materials, detail description of piece parts, thermal analysis and critical path instruction list. Final layout is used to generate screens for fabrication of substrates with conductor/resistor pattern and prepare detail documentation for assembly of hybrids. It also provides necessary information for design of assembly and reflow fixturization.

An in-depth analysis of the final layout is made during the final design review by engineering, manufacturing, test, and reliability representatives. The issues scrutinized as a minimum include the following items:

- Incorporation of previous comments
- Conformance to the circuit schematic
- Conformance to critical path list
- Compliance with design rules outlined in Tables 4-1 through 4-9
- Resistor design and closed resistor loops
- Thermal design and component coupling; correlation between thermal analysis and actual design
- Compliance with maximum allowable junction temperatures
- Ground and supply conductor design, ground loops
- High current considerations, adequate selection of conductors and wires

• High voltage considerations, conductor proximity and overglaze protection

• High frequency considerations

• Package outline and design compliance with customer requirements

• Package design compliance with assembly technology

• Design provisions for troubleshooting, rework and assembly fixturization

• Accommodations for testing of externally unaccessible parts of the circuit

• Space for circuit changes and potential growth

• Manufacturability

• Reliability

• Manufacturing cost

4.3.5.2—
Artwork Drawings

When hybrid layout design is done using CAD oriented system, the resistor, conductor and glass patterns are transferred to a magnetic media, which is used to produce an artwork master in a 1:1 scale on a stable photographic film. The patterns for each separate screening operation are individually exposed using photoplotting equipment.

For a manually designed layout, the master artwork is prepared to the same scale as the final layout. It is produced by overlay cutting and stripping of opaque rubylith material placed on layout drawing. A precision coordinatograph system is used for accurate cutting. This operation can also be performed using a knife and a straightedge, when the layout is designed to 20:1 scale. An individual master is cut for each separate screening operation - conductors, different resistor pastes, resistor overglaze, dielectric glass, etc. Each master artwork is identified and then photographically reduced to 1:1 scale working mask.

Working masks (1:1 scale) are used to expose photosensitive emulsion on the screen surface to produce opening pattern in the screen which is identical to the large scale layout drawing. Each pattern has at least three registration marks in opposite corners to assist in aligning screens on the substrate surface.

4.3.5.3—
Substrate Drawings

The substrate drawing depicts a composite of conductor/resistor/glass network on a ceramic substrate. Every individual substrate is identified by a separate drawing with identification of each resistor. Screening sequence and material description is presented along standard processing notes. A separate table lists resistor desig-

nations with nominal values and tolerances. Sometimes resistor sizes and minimum width after trim are also listed. Substrate size and tolerances are indicated to ensure consistency with final assembly requirements. It is recommended that a revision letter be screened on the substrate using conductor or resistor material to help identification during manufacturing phase.

4.3.5.4—
Assembly Drawings

The assembly drawing is used to identify the exact position and placement of components and wire-bonds with reference to conductor/resistor pattern and package leads. The drawing may include detail views of alternate chip assembly and standard notes with reference to processing documents. A separate drawing is created when it becomes necessary to provide details of an individual subassembly. In addition to details of each subassembly, the composite assembly drawing shows interconnections between substrates and substrates with package leads. All I/Os are numbered and labeled per schematic drawing.

4.3.5.5—
Marking Drawings

The marking drawing shows location and orientation of identifying hybrid information. All views of power hybrid package which carry identifying markings are shown. Any marking on the bottom of the package shall impede good heat transfer to the heatsink and should be prohibited. Marking of the package body (on the side) is important for retaining hybrid's identification in the case when the cover was removed for rework. The manufacturer's guidelines and customer specification should be reviewed for exact marking details and requirements.

4.3.5.6—
Other Documents

The following drawings complete the detail documentation package:

• Circuit schematic

• Test fixture schematic

• Test specification

• Acceptance test procedure

• Thermal analysis and calculations

• Burn-in fixture schematic (when required)

• Burn-in procedure (when required)

• Process and control documentation

• Miscellaneous manufacturing and test fixtures' drawings

• Hybrid case drawing

• Cover drawing

• Specification control documents for procurement of custom components

References

1. Phillips, W. E., ed., "Microelectronic Ultrasonic Bonding," Natl. Bur. Stand. (U.S.) Spec. Publ. 400-2, 1974.

2. Bilotta, A. J., *Connections in Electronic Assemblies*, Marcel Dekker, New York, 1985.

3. Taraseiskey, H., "Custom Power Hybrids," Solid State Technology, October 1985, pp. 111–117.

4. Osterman M. D. and Pecht, M., "Placement for Reliability, Based on Physics of Failure Concepts," NAECON 90, May 1990

5. *Reliability Prediction of Electronic Equipment*, Military Handbook MILHDBK-217E, Rome Air Development Center, New York, 1987.

6. Abuaf, N. and Kadambi, V., "Thermal Investigation of Power Chip Packages: Effect of Voids and Cracks," IEPS: 6th Annual International Electronics Packaging Conference, November 1986.

7. *Advanced Packaging and Interconnection of Electronic Components*, IPC Guidelines, IIPEC, August 1985.

8. Ham, R. E., "Prediction of Bond Wire Temperatures Using an Electronic Circuit Analogy," Hybrid Circuit Technology, April 1990, pp.53–54.

9. Shawhan, G. J. and Sutcliffe, G. R., "Plated Copper Metallization for Power Hybrid Manufacture," Hybrid Circuit Technology, April 1990, pp. 37–42.

10. Tyler, J. R., "Advanced Materials for Manufacturing of Microwave Power Hybrids," Hybrid Circuit Technology, March 1990, pp.25–29.

11. *SMD Process Applications*, Amperex Electronic Company

12. Krum, A., "The Design of Power Hybrids for Military Power Supplies," Proceedings of The Power Electronics Show and Conference, April 27, 1987, pp. 109–117.

13. Hopkins, D. C., Jovanovic, M. M., Lee, F. C., Stephenson, F. W. and Hayes, M. B., "Power Hybrid Design of a High-Frequency ZCS-QRC," Technical Papers of Fourth International High Frequency Power Conversion Conference, 1989, pp. 304–317.

5—
Thermal Management and Control

5.1—
Introduction

Thermal management of power hybrids encompasses all thermal processes, materials and technologies that must be utilized to provide effective heat removal from power dissipating components and transport to the system heatsink. Its primary objective is to ensure predictable and reliable performance of all components and materials within the safe specified limits. Flow of electric current in semiconductors, conductors, wires and passive elements in the power hybrid results in loss of energy. This energy is dissipated in the form of heat, which raises the temperature of the hybrid and its elements. An inadequate design of the heat flow path from the hybrid components to cooling media results in hot spots, thermal run away and undesirable mechanical stresses. This chapter shall review and develop guidelines and recommendations for design of thermal constituents of power hybrids, methods of measurements, process controls and design verification techniques.

5.2—
Heat Flow

5.2.1—
Thermal Resistance

As a derivative from the Second Law of Thermodynamics, the heat in form of

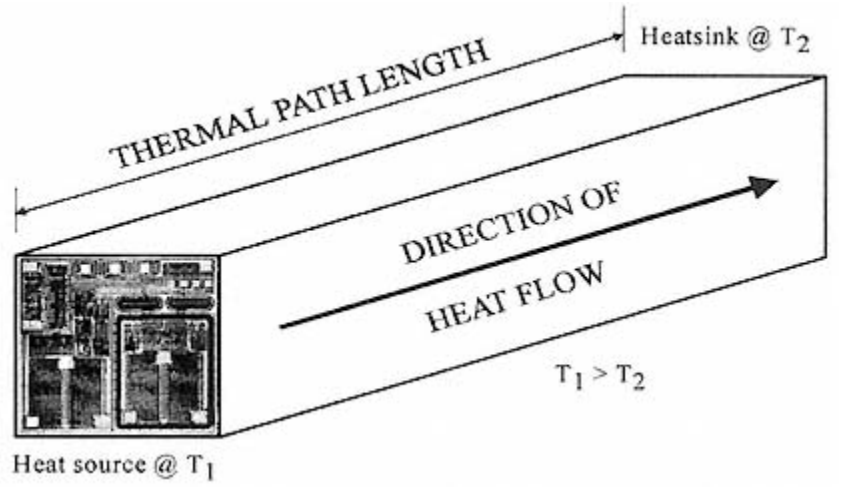


Figure 5-1
Heat flow diagram.

thermal energy flows from the high energy body to a body of low energy via a thermal path. Since body with higher energy has higher temperature, the heat transfer takes place in the direction of decreasing temperature. This is shown in Figure 5-1. The three mechanisms of heat transfer from a hybrid package are illustrated in Figure 5-2:

• Conduction, when two bodies are in physical contact, or are separated by a solid or fluid medium.

• Convection, when the bodies in contact are of different phases, i.e., solid and gas. Convection can occur naturally or be forced by moving cooling medium — air or liquid.

• Radiation, by emission of infrared energy.

Conduction is a predominant mode of heat transfer from power hybrid circuit elements to the heatsink. Cooling effect of natural convection and radiation is usually ineffective when compared with heat conduction. It proves to be negligible (roughly < 2%) and is often omitted during thermal analysis calculations. A general definition for the heat flow in a steady-state one-dimensional conduction is given by the Fourier's Law expression:

$$P = \frac{dQ}{dt} = -kA\frac{dT}{dx}$$

where

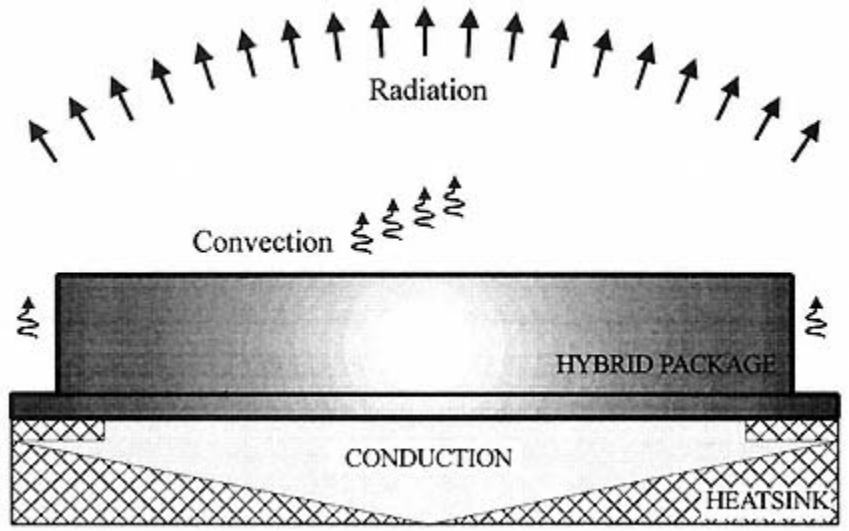


Figure 5-2
Means of heat transfer from a hybrid package.

P = heat transfer rate or power
Q = heat
k = thermal conductivity of material
A = cross-sectional area of heat flow normal to flow direction
x = length in direction normal to A
T = body temperature
t = time

It is apparent that the heat transfer rate can be increased by either of the following:

• Increasing temperature gradient dT/dx between the heat source and the heatsink

• Using materials with higher thermal conductivity k

• Increasing cross-sectional area of heat flow A

Integrating the equation

yields

$Px = kA\Delta T$

or

$$P \cdot \frac{x}{kA} = \Delta T$$

By defining the thermal resistance to heat flow as

$$R_{th} = \frac{x}{kA}$$

and substituting into the last equation, we get an expression that relates temperature gradient, dissipated power and thermal property of heat conducting medium.

$\Delta T = P \cdot R_{th}$

5.2.2— Thermal Analysis

5.2.2.1— Steady State

In the real world, heat transfer process involves an extremely complicated combination of isotherms and heat flux lines. A very large selection of database and computer software programs for analytical analysis of thermal effects in electronic systems is available today. Typical analytical methods solve multidimensional problems in complex environments and strongly depend on input variables. Most power electronics systems do not operate in a steady state mode. The power semiconductors, magnetics, resistors and other components operate under a constantly changing combination of thermal and electrical conditions, making it virtually impossible to perform an all-inclusive accurate analysis and predict the exact thermal performance at any time. It is the purpose of this paragraph to provide the reader with a proven practical and simple method to calculate the anticipated temperature of power hybrid components under specified conditions of operation. Some of the possible heat transfer paths in the power hybrid package are shown in Figure 5-3. Power is dissipated in a single transistor die Q_1. Transistor is soldered to metallization on the ceramic substrate which is soldered to the package floor. Two wire-bonds are attached to the chip — WB_1 and WB_2. WB_1 is used to conduct large electrical current and is attached to a metal tab soldered to the substrate metallization. WB2 is a smaller diameter wire

which is attached directly to the conductor. A third large diameter wire-bond WB3 is connecting the metal tab to the package I/O pin. Externally to the hybrid, an interconnecting wire is wrapped around the pin and soldered. The entire hybrid is mounted on a heatsink. The heat source is located on the chip surface and is determined by the amount of electrical energy losses. Eight possible simplified heat transfer paths are illustrated in Figure 5-3 with the assumption that the heatsink and ambient environment are at temperatures lower than the hybrid:

1. Heat source–silicon–WB1–tab–WB3–I/O pin–solder–wire

2. Heat source–silicon–WB1–tab-WB3–I/O pin–glass bead–sidewall–cover

3. Heat source–silicon–WB1–tab–WB3–I/O pin–glass bead–sidewall–braze–package base–heatsink

4. Heat source–silicon–WB1–tab–solder–conductor–ceramic substrate–solder–package base–heatsink

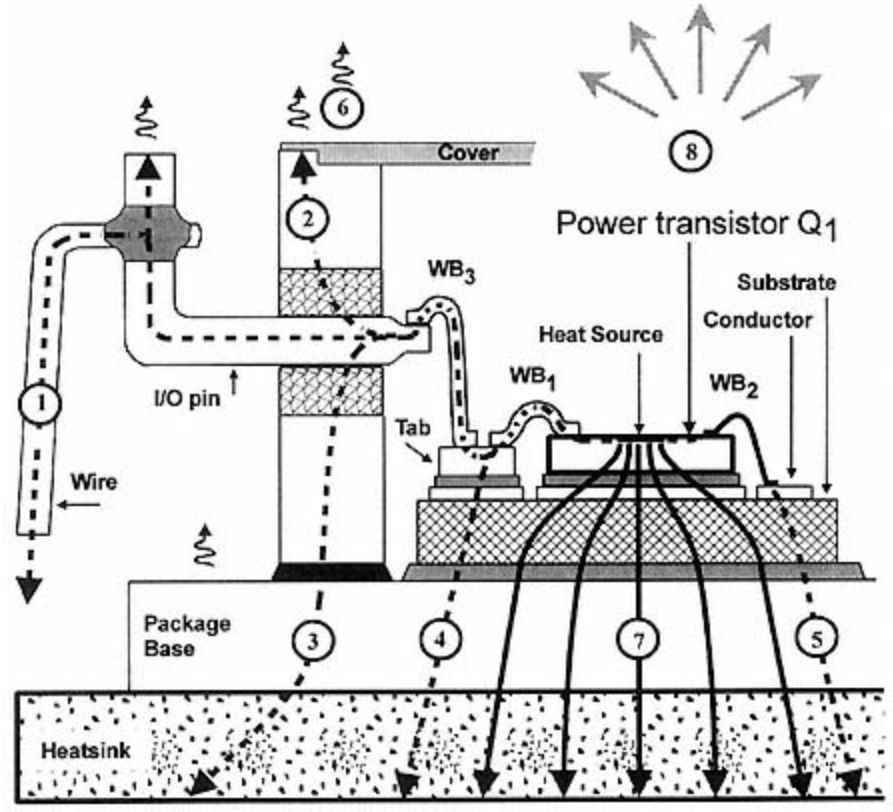


Figure 5-3
Selected heat flow paths in a power hybrid package.

5. Heat source–silicon–WB2–conductor–ceramic substrate–solder–package base–heatsink

6. Convection from external surfaces of the hybrid

7. Heat source–silicon–solder–conductor–ceramic substrate–solder–package base–heatsink

8. Radiation by components and package

The paths shown by a dashed line have high thermal resistance to heat flow and conduct a small portion of overall generated heat energy. It would be an enormous and virtually impossible task to specify all possible heat paths and their interaction in a complex power hybrid including hundreds of components, tens of I/O pins, and hundreds of wire-bonds. An oversimplified heat spreading model is frequently used by hybrid designers to estimate thermal performance characteristics of circuit elements. It provides adequate and conservative solutions. Discounting of secondary heat paths (dashed lines) and heat transfer by convection and radiation provides additional margins for reliable performance — the calculated temperature rise will be slightly higher.

The heat-spreading model takes into account the heat transfer by conduction only from the heat source to the heatsink — path 7 in Figure 5-3. A series of basic assumptions are also made:

• There is no thermal gradient at the heat source. If the heat source is a semiconductor junction, then it is assumed that the dissipated power density is uniformly distributed over the active area on the chip surface.

• Thermal properties of materials are a function of temperature and are independent of time.

• The heat flux diverges at a 45° angle from heat source to the heatsink.

• The heatsink is large enough to be considered as having an infinite capacity for absorbing heat and maintaining constant reference temperature.

• A one-dimensional heat flow occurs when the cross-sectional area remains constant. Examples are: thick-film conductors, solder or epoxy adhesives, etc.

• No heat is generated between the heat source and heatsink.

• Heat flux envelopes from different sources do not overlap.

• Dimensions are independent of temperature and time.

• All heat conducting mediums in the path of heat flow are continuous sheets; that is, no voids or patterns are present.

• All layers are of uniform thickness.

Heat spreading model is shown in Figure 5-4. The truncated shape represents the heat flux path along Z axis from a rectangular heat source. In reality the spreading angles α (along X axis) and β (along Y axis) depend on material properties, thickness, geometry and direction. A typical hybrid has a multiple layer construction, which involves a stack-up of materials with various thermal properties and physical dimensions. Such construction is treated as a set of series thermal resistances in which the heat source for each underlying layer is represented by the exit area of the previous layer's heat spreading volume. The average steady state thermal resistance for an infinitesimal rectangular heat source is given by the following expression:

$$dR_{th} = \frac{dz}{kS} = \frac{dz}{k\,(L + 2z\tan\alpha)\,(W + 2z\tan\beta)}$$

where:

R_{th} = thermal resistance
z = distance from the heat source
k = thermal conductivity of material
L = length of the heat source
W = width of the heat source
S = cross-sectional area normal to heat flow

The thermal resistance of the layer is given by:

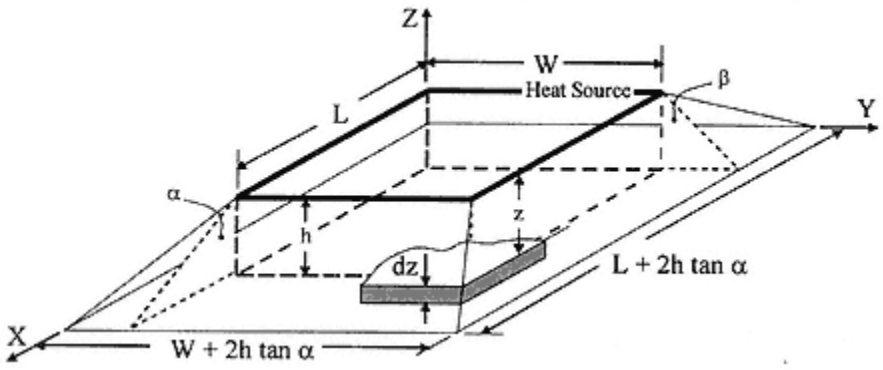


Figure 5-4
Heat spreading model for a rectangular heat source.

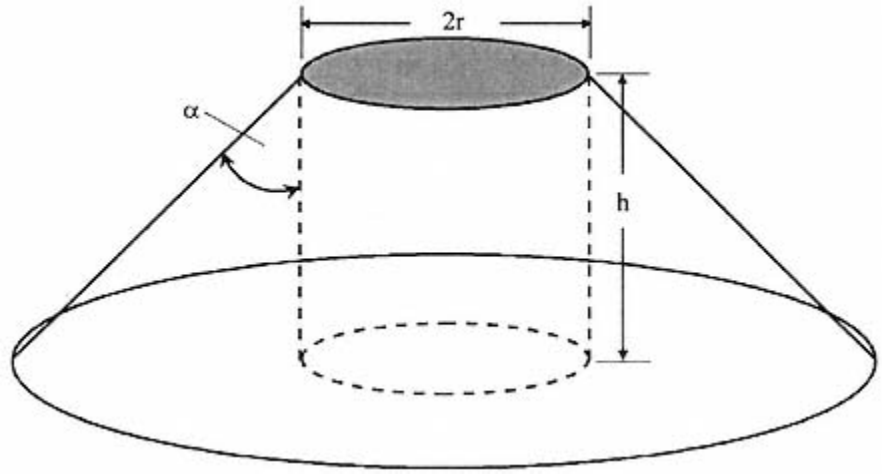


Figure 5-5
Heat spreading model for a circular heat source.

$$R_{th} = \int_0^h \frac{dz}{kS} = \int_0^h \frac{(dz)}{k\,(L + 2z\tan\alpha)\,(W + 2z\tan\beta)}$$

where h = material thickness.

Earlier we made an assumption that the heat flux diverges at a 45° angle. Therefore, for the purpose of calculations we shall set $\alpha = \beta = 45°$ and $\tan\alpha = \tan\beta = 1$. When the heat source is rectangular — $L \neq W$

$$R_{th} = \frac{1}{2k\,(L - W)} \ln\left[\frac{(W + 2h)}{(L + 2h)} \cdot \left(\frac{L}{W}\right)\right]$$

When the heat source is square — L = W = a

$$R_{th} = \frac{h}{k\,(a^2 + 2ah)}$$

In the case of a one-dimensional heat flow from square source this expression becomes

Table 5-1 Thermal resistance calculation parameters

No.	Layer description	Thermal conductivity, k (watts/°C-in) at 25°C/100°C	Thickness h (inches)	Length and width of the heat source a (inches)	Calculated therma resistance (°C/wat
1a	Silicon	3.3 / 2.4	0.020	0.060	1.01
1b	Silicon	3.3 / 2.4	0.010	0.100	0.3030
2	Solder	0.79	0.003	0.100	0.3797
3	Molybdenum tab	3.4 / 3.4	0.020	0.100	0.4202
4	Solder	0.79	0.003	0.140	0.1937
5	BeO substrate	6.3 / 5.4	0.040	0.140	0.2061
6	Solder	0.79	0.003	0.220	0.0785
7	Copper case	10.2 / 10.0	0.100	0.220	0.1061

$$R_{th} = \frac{h}{ka^2}$$

where a^2 = cross-sectional area normal to the heat flow direction.

For a circular heat source in Figure 5-5, where r = heat source radius, the expression for thermal resistance takes the following form:

$$R_{th} = \frac{1}{k\pi} \cdot \frac{h}{(r^2 + rh)}$$

Example of Calculation of Thermal Resistance and Temperature Rise

The following assembly is used to calculate junction-to-case thermal resistance and associated temperature rise. A power transistor is soldered to a spreader tab, which is soldered to a thick-film conductor on BeO substrate. The substrate in turn, is soldered to a copper case, as shown in Figure 5-6. To assist with the calculations the mechanical dimensions and values of thermal conductivity of materials are summarized in Table 5-1. The heat is uniformly generated in the

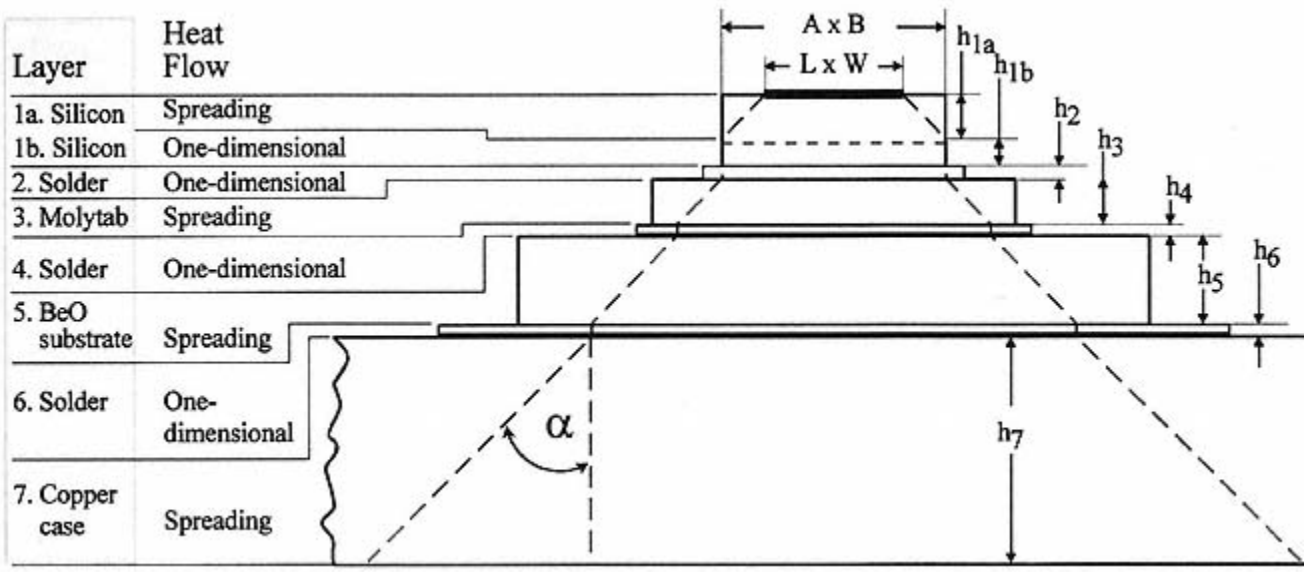


Figure 5-6
Heat spreading model.

junction area on the chip surface and spreads through the area 1a. At the border with the area 1b the heat flow encounters the sides of the transistor chip and becomes one-dimensional.

The thermal resistance of silicon chip consists of: the heat spreading portion equal to

$$R_{th}^{(1a)} = \frac{h_{1a}}{k(a^2 + 2ah_{1a})} = \frac{0.02}{3.3\,(0.0036 + 2 \cdot 0.06 \cdot 0.02)} = 1.01°C/w$$

and one-dimensional portion equal to

$$R_{th}^{(1b)} = \frac{h_{1b}}{ka^2} = \frac{0.01}{3.3 \cdot 0.009} = 0.303°C/w$$

The total thermal resistance for the transistor chip:

$$R_{th}^{chip} = R_{th}^{(1a)} + R_{th}^{(1b)} = 1.313°C/w$$

The underlying layer is solder with one-dimensional heat flow:

$$R_{th}^{(2)} = \frac{h_2}{ka^2} = \frac{0.003}{0.79 \cdot 0.009} = 0.3797°C/w$$

For the molybdenum heat spreader (molytab):

$$R_{th}^{(3)} = \frac{h_3}{k(a^2 + 2ah_3)} = \frac{0.02}{3.4\,(0.009 + 2 \cdot 0.095 \cdot 0.02)} = 0.4202°C/w$$

For solder layer between the molytab and BeO substrate:

$$R_{th}^{(4)} = \frac{h_4}{ka^2} = \frac{0.003}{0.79 \cdot 0.0182} = 0.1937°C/w$$

Assuming that the thick-film conductor material is perfectly adhered to the substrate and has a minute thermal resistance, we shall conclude that

$$R_{th}^{cond} = 0$$

The thermal resistance of BeO substrate:

$$R_{th}^{(5)} = \frac{h_5}{k\,(a^2 + 2ah_5)} = \frac{0.04}{6.3\,(0.0182 + 2 \cdot 0.135 \cdot 0.04)} = 0.2061°C/w$$

For solder layer between the BeO substrate and case bottom:

$$R_{th}^{(6)} = \frac{h_6}{ka^2} = \frac{0.003}{0.79 \cdot 0.0462} = 0.0785°C/w$$

The final material layer – copper bottom:

$$R_{th}^{(7)} = \frac{h_7}{k\,(a^2 + 2ah_7)} = \frac{0.1}{10.2\,(0.0462 + 2 \cdot 0.215 \cdot 0.1)} = 0.1061°C/w$$

The total thermal resistance from the semiconductor chip junction to hybrid case seating plane (junction-to-case) is:

$$R_{th}^{(j-c)} = R_{th}^{chip} + R_{th}^{(2)} + R_{th}^{(3)} + R_{th}^{(4)} + R_{th}^{(5)} + R_{th}^{(6)} + R_{th}^{(7)} = 2.6973°C/w$$

In order to better understand the significance of characteristics of different layers, we shall calculate the value of junction-to case thermal resistance for an identical stack-up with exception that the die size shall increase to 0.2" × 0.2" × 0.03" with the heat source 0.16" × 0.16". Repeating the calculations we get

$$R_{th}^{(j-c)} = 0.7272°C/w$$

For the same die and heat source size we shall now change the case material and thickness. New material shall be kovar with:

thermal conductivity k = 0.34 (watts/°C-in)

thickness h_7 = 0.040 inch.

The resulting thermal resistance is

$$R_{th}^{(j-c)} = 1.5873°C/w$$

Assigning to each case a power dissipation level of $P_D = 25$ watt and calculating the resulting temperature rise at the junction with reference to the case, we obtain the following values:

• Stack 1. For the chip size a = 0.1" × 0.1" × 0.03" and the copper case

$$\Delta T = P_D \cdot R_{th}^{(j-c)} = 25 \cdot 2.6973 = 67.43°C$$

• Stack 2. For the chip size a = 0.2" × 0.2" × 0.03" and the copper case

$$\Delta T = P_D \cdot R_{th}^{(j-c)} = 25 \cdot 0.7272 = 18.18°C$$

• Stack 3. For the chip size a = 0.2" × 0.2" × 0.03" and the kovar case

$$\Delta T = P_D \cdot R_{th}^{(j-c)} = 25 \cdot 1.5873 = 39.68°C$$

By doubling the length and width dimensions of the chip we accomplished a reduction of thermal resistance by a factor of 3.71. If the maximum allowable junction temperature is 150°C, and it is derated to a lower value for reliability considerations — say 125°C, then the limiting maximum operating case temperature at full power will be:

• For stack 1 — $T_{case(max)} = 57.57°C$

• For stack 2 — $T_{case(max)} = 106.82°C$

• For stack 3 — $T_{case(max)} = 85.32°C$

The advantage of increased operating temperature range at full power is clearly observed by comparison of stack 1, stack 2, and stack 3. One of the distinctive features of power hybrids used in high reliability military and space systems is their high cost. A significant contributor to the cost of raw materials used in power hybrids' manufacturing is the package. The mandate for hermeticity, high thermal conductivity and wide operating temperature range considerably limit the selection of packaging materials and their melding. One of the possible solutions is demonstrated by the transformation from stack 1 to stack 3. An expensive copper case is replaced by a much cheaper kovar case. An additional benefit of

extended operating temperature range is also gained by the increase of the die size.

The assumptions made prior to calculations were idealistic. In reality:

• The heat dissipation pattern on the chip surface is not uniform.

• The interfaces between the layers are not homogeneous and are filled with many voids.

• Thick-film conductors do not perfectly adhere to ceramic substrates and may have a thick layer of glass beneath them.

• The thermal conductivity of most materials is a function of temperature. If the thermal resistance for stack 1 is calculated at 100°C, we would get a 19.6% increase from value at 25°C.

$$R_{th}^{(j-c)} = 32.26°C/w$$

Therefore, the numbers should be considered as a reference, and be verified and correlated with the results of measurements. A set of practical adjustments may be made during calculations based on experience, materials and equipment used at a specific manufacturing facility.

The ability to accurately predict the thermal performance of the power hybrid does not end with a number, which expresses an anticipated value of the thermal resistance. It strongly depends on the circuit design, quality of construction, manufacturing processing and verification controls.

5.2.2.2—
Transient Thermal Resistance

In general, thermal and electrical characteristics of power semiconductors are interrelated. Manufacturer's data sheets specify electrical performance as a function of temperature. This information is displayed numerically and graphically. As a rule it applies to the ship regardless of packaging construction. Nevertheless, output current or power derating and steady-state or transient thermal resistance characteristics exhibit strong dependance on packaging. Data sheet parameters usually do not apply, when the power chip is used in the hybrid.

The designer is faced with the necessity to generate derating curves and specify the steady-state and transient thermal resistance for his circuit. Steady-state thermal resistance applies when the power components operates in a DC mode, in other words when power dissipation level doesn't change with time. The calculation of ΔT and R_{th} for steady-state operation was addressed in the previous paragraph.

In a majority of applications of power hybrids, the power transistors are

switching high currents at high frequency. The power dissipation in the chip depends on pulse duration, du factor and the magnitude of the losses. Figure 5-7 illustrates the stack-up construction of a semiconductor device used in the following calculations. The nature of heat flow can be compared with the flow of electri current. The electrical to thermal analogy is shown in the Table 5-2. The heat flow P_D through a thermal resistance R_{th} is proportional to the temperature differential ΔT, just like the electrical current I flowing in resistor R is proportional to the applied voltage V. Each separate layer in the stack-up is characterized by a thermal capacitance C_{th}:

$$C_{th} = \rho C_T V$$

where

C_{th} = thermal capacitance
ρ = material density
C_T = specific heat

When a pulse waveform is applied to the transistor, the power dissipation levels change with time. The junction temperature-to-case differential also becomes a function of time. As the heat flow is generated wi the first electrical pulse, the temperature differential starts increasing, as shown in Figure 5-8b. An electric analog of capacitor C charging via resistor R is shown in detail Figure 5-8a. When the pulse duration becomes very long, typically more than 10 seconds for

Table 5-2 Electrical — thermal analogy

Electrical	Thermal
Ohms Law V = IR	Fourier's Law - $\Delta T = P_D R_{th}^{j-c}$
Voltage - V	Temperature differential - ΔT
Current - I	Dissipated power - P_D
Resistance - R	Thermal resistance - R_{th}^{j-c}
Capacitance - C	Thermal capacitance - C_{th}
Conductivity - g	Thermal conductivity - K

power hybrids — the temperature gradient reaches the equilibrium level ΔT_E. The temperature differential ΔT at any given time can be expressed as

$$\Delta T = \Delta T_E\left(1 - e^{-t_1/\tau}\right)$$

where

t_1 = heating time
$\tau = R_{th}C_{th}$, a time constant of a thermal network.

As long as a single heating pulse is applied, the temperature rises as shown in Figure 5-10. With increase of the pulse width from t_{on1} to t_{on2}, the temperature gradient increases from ΔT_1 to ΔT_2. This increase is limited by the steady state equilibrium T_E, which is reached as time approaches infinity. At the end of the

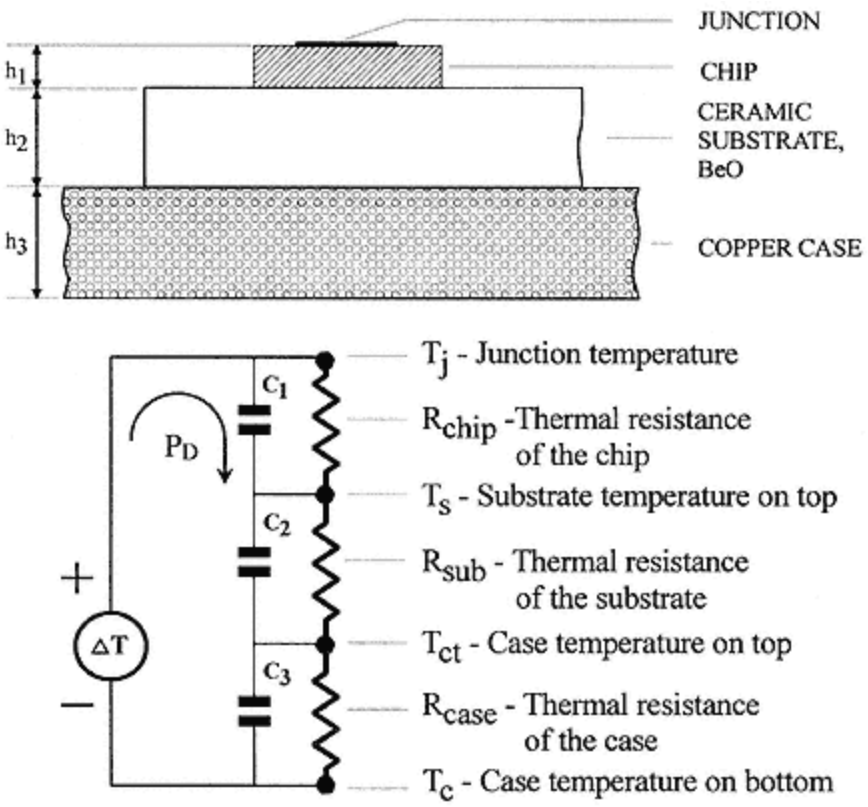


Figure 5-7
Transient thermal resistance model.

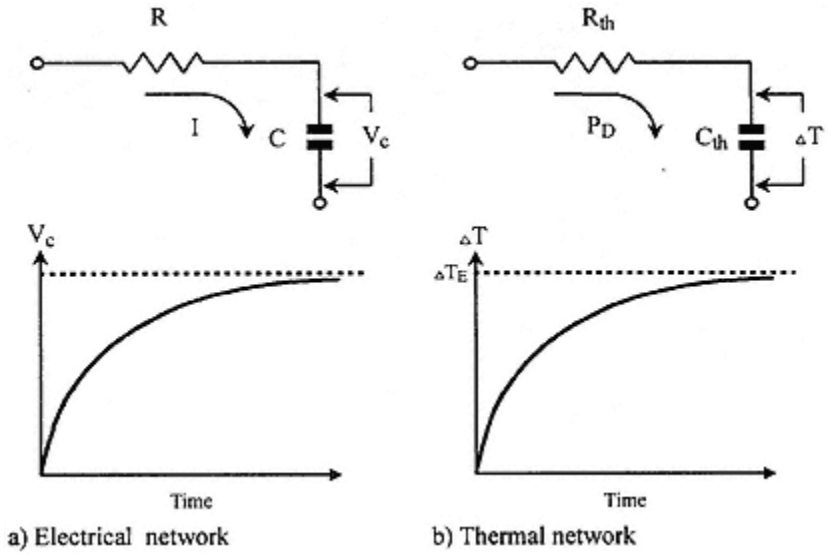


Figure 5-8
Thermal-electrical analogy of a single– pulse response.

heating pulse the temperature decreases and can be found from the expression

$$\Delta T_{off} = \Delta T_{max}\left(e^{-t_2/\tau}\right)$$

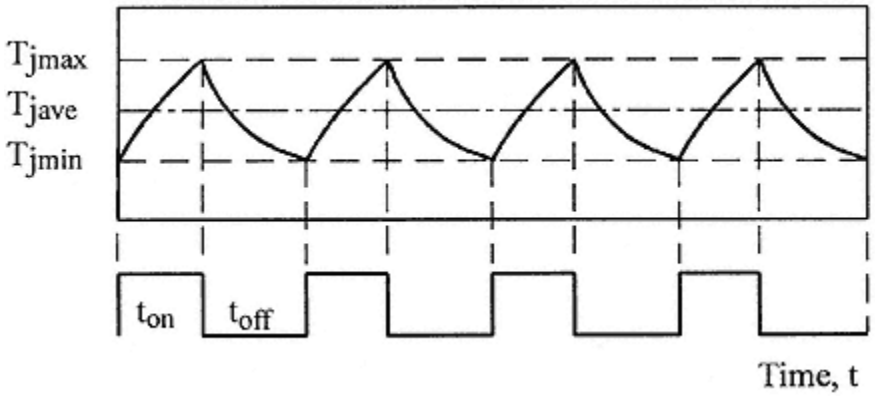


Figure 5-9
Thermal ripple. Transient response to a waveform with constant t_{on} and t_{off}.

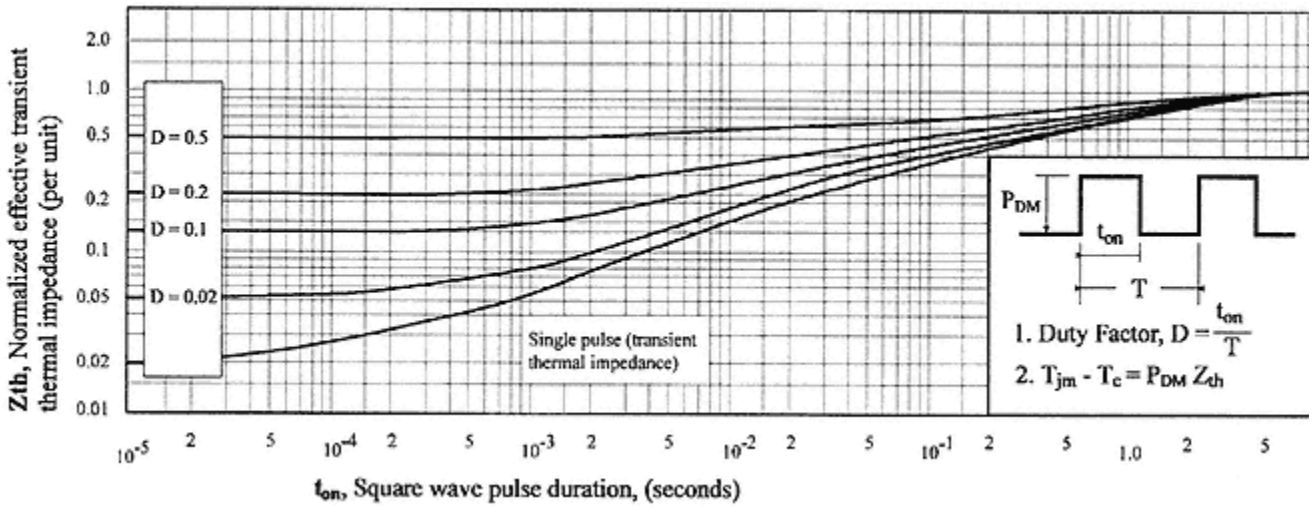


Figure 5-10
Normalized effective transient thermal impedance vs. square wave pulse duration.

Table 5-3 Transient thermal analysis for single pulse application

Layer/Characteristics	Silicon chip	BeO substrate	Copper case
Thickness (inches)	$h_1 = 0.030$	$h_2 = 0.040$	$h_3 = 0.100$
Heat source size (inches)	0.060×0.060	0.120×0.120	0.200×0.200
Density, ρ (g/in^3)	38.346	47.195	146.336
Specific heat, C_T (Cal/g-°C)	0.180	0.250	0.093
Volume, V (in^3)	0.00027	0.001088	0.01
Thermal capacitance, C_{th}(J/°C)	$C_1 = 0.0078$	$C_2 = 0.0573$	$C_3 = 0.56979$
Time constant, τ (sec)	$\tau_1 = 9.85 \times 10^{-3}$	$\tau_2 = 15.2 \times 10^{-3}$	$\tau_3 = 69.8 \times 10^{-3}$
Thermal resistance, R_{th}(°C/watt)	$R_{th1} = 1.2626$	$R_{th2} = 0.2646$	$R_{th3} = 0.1225$

where t_2 = off time.

During a typical operation of a hybrid circuit, a series of consecutive pulses are applied to the power devices. Their waveforms vary in amplitude, duration and duty cycle. They may have a constant duty cycl or be amplitude, pulse width or frequency modulated. An example of a thermal transient response to a frequency modulated waveform is shown in Figure 5-11. During the switching operation, the junction temperature of the chip fluctuates around the average value, which depends on the heating pulse configuration. Figure 5-12 illustrates the thermal ripple of the junction temperature for a case, when the t_{o} is long enough for the temperature to return to its initial value. With increase of the operating frequency, t ripple amplitude T_{jmax}—T_{jmin} decreases

By applying the formulas for R_{th}, C_{th} and τ to calculate the transient response

parameters for the model shown in Figure 5-7 we obtain the values summarized in Table 5-3.

Typically most power applications are characterized by use of a series of electrical pulses rather than a single pulse. When a square wave with a duty factor DDT_{on}/T, as shown in Figure 5-9, is applied to a single transistor, the resulting junction temperature will also depend on the pulse duration t_{on}. The shorter the pulse, the smaller the junction temperature will rise. The variation in thermal resistance with pulse duration is shown graphically in Figure 5-9. The thermal resistance is normalized so that

$$Z_{th} = \frac{R_{th(t)}}{R_{th}}$$

This family of curves allows to calculate the junction temperature if power dissipation in the chip P_{DM}, duty cycle D, and pulse duration t_{on} are known, by using the expression

$$T_{jm} = T_c + P_{DM} \cdot Z_{th}$$

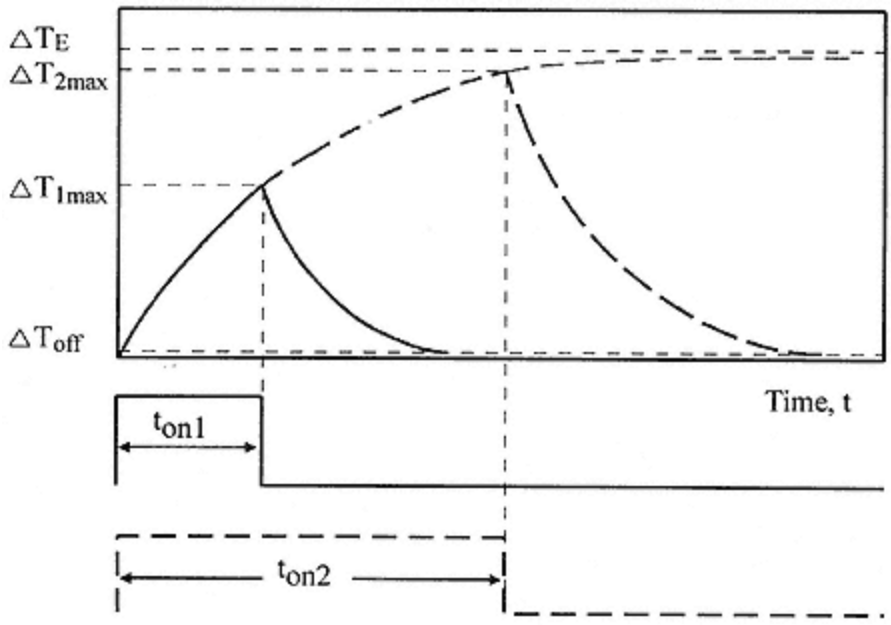


Figure 5-11
Thermal transient response dependence on single pulse duration.

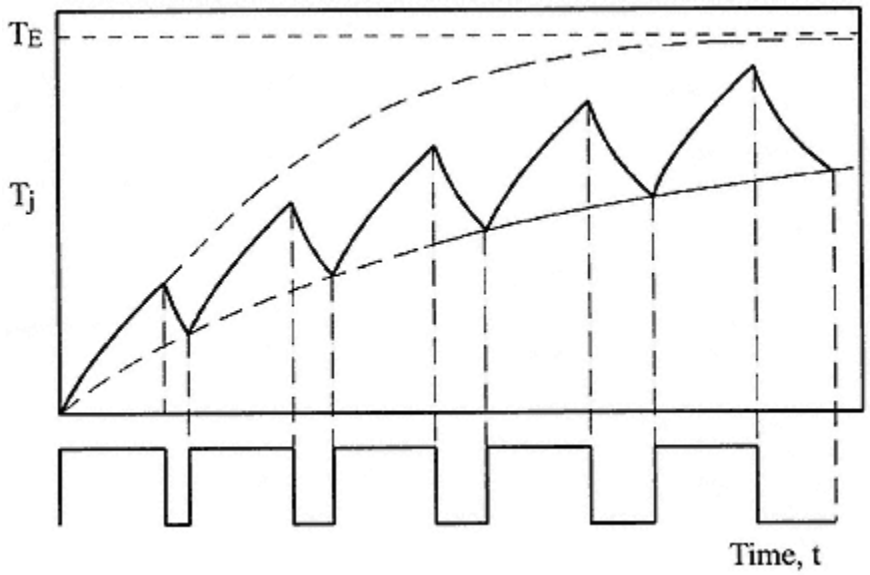


Figure 5-12
Thermal transient response to a pulse waveform with changing repetition rate.

5.3—
Thermal Partitioning

An example of a single isolated heat source was reviewed in the previous paragraph. Yet a typical power hybrid consists of a large number of power dissipating components, which are placed in close proximity of each other. When that occurs, the heat flux lines from adjacent chips interact with each other. This is demonstrated in Figure 5-13. An overlap of the spreading heat flow from adjacent components effectively increases the thermal resistance by reducing the heat flow cross-section. It is possible to evaluate the effect of overlap, when two devices are of the same size and dissipate equal amounts of heat. However, in reality the components have different sizes and form factors. They operate in a combination of continuous and switching modes. That makes the analysis very complex. There are several design techniques, that could be used to minimize this effect. First, by placing components, which operate out-off-phase, the interaction may be somewhat reduced. Another method employs reduction of material thickness. For example, reduction of package base thickness from h to h_1 in Figure 5-

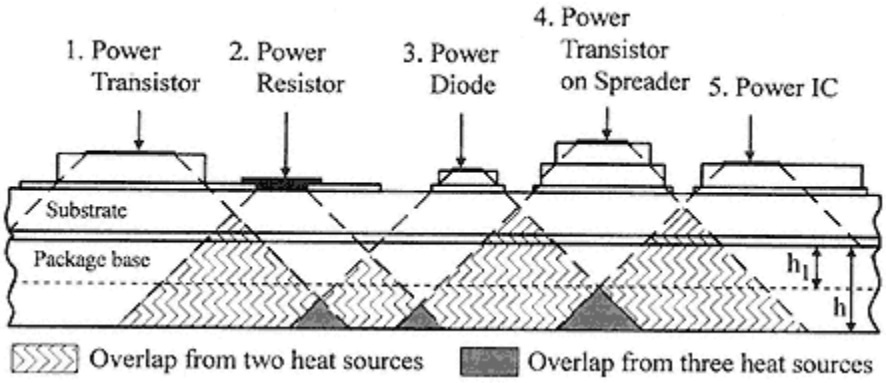


Figure 5-13
Heat flux overlap, thermal partitioning.

13 would eliminate the overlap from three heat sources and reduce the dual over laps. If the hybrid is attached to a heatsink made from a high thermal conductivity material, the internal reduction of overlap will have a definite positive effect on the overall thermal performance of the system. Otherwise, the total thermal resistance — junction–to–ambient may even increase. The overlap can also be reduced or eliminated by simply placing components far enough from each other, Figure 5-14a. The necessary distance L between the components depends on the thickness of tabs, substrate, package base and adhesives. For the illustration in Figure 5-14a, $L = H_1 + H_2$. Use of a different approach mostly helps to prevent the interaction between two adjacent heat flows. This is accomplished by mounting the chips on separate substrates, Figure 5-14b. The length of the gap G depends on the package base thickness h and is equal: $G = 2h$. Additional heat sources, such as conductors and resistors can be designed using larger dimensions to reduce the power dissipation (conductors) and lower the thermal resistance. There is no universal solution to thermal partitioning. The final design configuration will depend on circuit performance requirements, system environment and technological limitations. It is always prudent to make an extra effort to address the thermal design parameters to produce a reliable hybrid with predictable performance.

5.4—
Thermal Effects on Device Performance

Operating junction temperature of semiconductor devices has a direct impact on electrical performance, reliability, and cost of the hybrid circuit. Gain, threshold voltages, delays, leakage currents, output power levels, etc., are some of the parameters that change with temperature. Such dependence is normally taken into consideration by the circuit designer at early stages of development. After

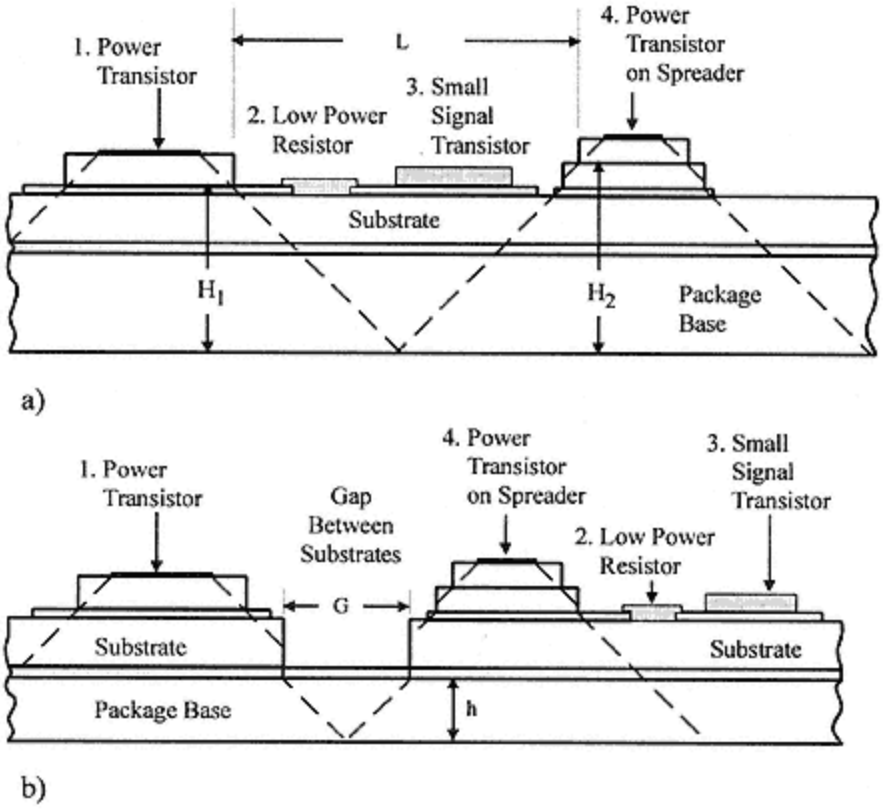


Figure 5-14
Design techniques for reduction of heat flow overlaps.

the hybrid design is finalized, the circuit design parameters are revised to accommodate the limitations unknown at the early design phase. At that point the reliability of the product is assessed. The overall reliability of hybrid circuit is the aggregate reliability of its components. Manufacturers of power hybrid circuits used in military electronic systems use MIL-HDBK-217, Reliability Prediction of Electronic Equipment published by U.S. Department of Defense. Critics of this document point out that it results in reliability predictions, which often do not compare well with field data and is frequently misused. This controversy is not covered in this book, however, it is important that the calculated Mean Time Between Failures (MTBF) of a power hybrid circuit—a single number representing a uniform failure rate throughout its lifetime is used as a reference along with good engineering and manufacturing practices.

There are many failure mechanisms in hybrids, which could be grouped as follows:

1. Internal

• Electrical overstress caused by voltage, current or power higher than maximum allowed by design

• Thermal-mechanical overstress resulting in loss of adhesion of die, tabs and substrates, and integrity of wire bonds caused by

- incompatibility of materials

- temperature cycling

- thermal shock

- excessive operating temperatures

• Chemical contamination resulting in corrosion, electrical shorts, open wire bonds caused by

- contaminated solvents

- inadequate material and process controls

2. External

• Electrostatic Discharge (ESD) caused by absence of

- conductive storage containers and antistatic bags

- conductive storage mats

- grounded wrist straps

- grounded work benches

- humidity control

- ionized air

- grounded assembly and test equipment

• Vibration

• Mechanical shock

• Electromagnetic Interference (EMI)

• Inadequate storage conditions and temperature

• Package deformation during mounting in the system caused by excessive torque or inadequate flatness of the seating plane

• Hermeticity failure due to handling of I/O leads

• Operating environmental medium – oils, salt, etc.

Many failure mechanisms associated with semiconductor devices result

from physical or chemical processes occurring on a microscopic level. Temperature accelerates these processes and allows to establish an accelerated testing program, which causes the devices to age at a faster rate without introducing new failure mechanisms. The Swedish scientist Arrhenius established a relationship between the rates of chemical reactions and temperature and expressed it by the equation:

$$R = Ae^{\left(\frac{-E_a}{kT}\right)}$$

where

R = the rate of chemical reaction
A = a constant
E_a = the activation energy for the associated failure mechanism
k = Boltzman's constant (8.62×10^{-5}eV/°K)
T = temperature in degrees Kelvin

This equation simply establishes that the chemical reactions are accelerated exponentially as the temperature increases. The activation energy Ea is an experimentally determined quantity, which defines the extent of dependance of chemical reaction rate on temperature. It is different for various failure mechanisms. The activation energy values associated with chemical reactions causing most of the failures in semiconductor devices, such as ionic contamination diffusion through oxides and silicon, metal migration and corrosion, fall in the range from 0.4 eV to 1.2 eV. Examples of standard activation energies used for typical failure mechanisms are shown below:

Failure mechanism	Activation energy
Electron trapping	1.1 eV
Gold-Aluminum intermetallics	1.0 eV
Aluminum electromigration	0.7 eV
Oxide defects	0.4 eV
Ionic contamination	1.1 eV

If the reaction rate follows the Arrhenius model, then the temperature versus lifetime relationship of a semiconductor component can be expressed as:

where

t = time to failure (lifetime)
C = temperature independent constant

Knowing the time-temperature relationship of an accelerated failure mechanism, it is possible to conduct a short duration test, that can be used to determine the reliability of the device in a matter of a few weeks, rather than many years. If a component fails at temperature T1 at time t1, and at temperature T2 at time t2, then the acceleration factor t1/t2 is expressed as:

$$\frac{t_1}{t_2} = e^{\left[\frac{E_a}{k}\left(\frac{1}{T_1}-\frac{1}{T_2}\right)\right]}, \qquad T_1 > T_2$$

The phenomena of lifetime-temperature dependence once more emphasizes the paramount importance of maintaining predictable and the lowest possible operating temperature of semiconductor devices to guarantee reliable functionality of the power hybrid circuit.

5.5—
Thermal Measurements

Calculations of the thermal resistance and reliability predictions provide theoretical reference information to the hybrid designer. These calculations are based on a series of assumptions. The actual values reflecting the hybrid performance in the test fixture or in the system depend on a large variety of parameters and conditions, which can't be defined and incorporated in modeling of heat flow process during calculations. These factors at times contribute to significant deviations from anticipated performance and may result in a catastrophic failure of the product. They can be classified as:

• Manufacturer related and consist of

- deficient hybrid circuit design
- inadequate manufacturing practices
- lack of material and process controls
- incomplete characterization of thermal and electrical performance of the device

• User related

- absence of understanding of power hybrid technology — its advantages and disadvantages
- lack of application and product performance information leading to misuse of the device in the system

The characterization of thermal performance of power hybrids is extremely important to the device manufacturer and the user. It allows the designer of the hybrid circuit to identify potential problems and incorporate larger margins in the performance specification to prevent future failures. The knowledge where the weak spots are, also helps to set up tighter process controls and perform additional testing. The user can considerably benefit from the detailed description of the thermal performance and configuration of the hybrid as demonstrated in Figure 5-15, where the hybrid package is shown from the bottom side. The dotted lines mark the outlines of the case cavity and the ceramic substrates. Low power section contains two substrates and the high power section has one substrate with four transistors Q1, Q2, Q3, Q4. During the operation of the hybrid most of the power is dissipated in the power section. Unless the user is aware of the size and location of power dissipating elements, he is unable to properly calculate the anticipated thermal performance of the hybrid in his system. For example, using the dimensions of Figure 5-15 and making following the assumptions:

• The power is dissipated continuously and uniformly across the substrate surface

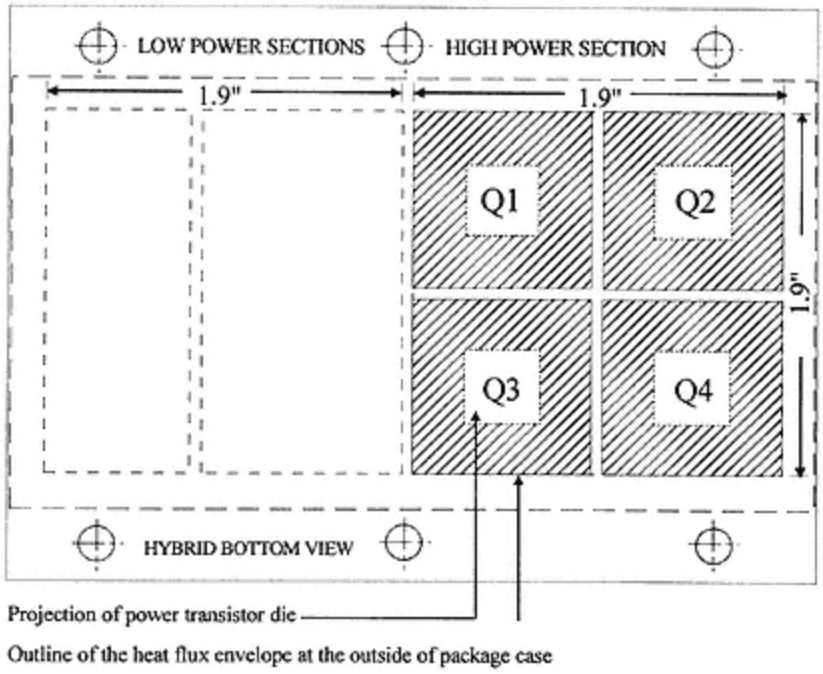


Figure 5-15
Temperature distribution on the case, bottom.

• Power dissipation in the low power section is negligible

we can calculate the case-to-ambient temperature rise values. The first

$$\Delta T_{C-A}^{p}$$

represents case-to-ambient temperature rise for the heat source produced by the high power substrate equal to 1.9" × 1.9". The second

$$\Delta T_{C-A}^{e}$$

is calculated with an erroneous assumption that the power is dissipated by the entire hybrid with area equal to 3.8" × 1.9". Using the following formulas to calculate thermal resistance values

$$R_{th}^{e} = \frac{1}{2k\,(L-W)} \ln\left[\frac{(W+2h)}{(L+2h)} \cdot \left(\frac{L}{W}\right)\right]$$

$$R_{th}^{p} = \frac{h}{k\,(a^2 + 2ah)}$$

and assuming that the power dissipation equals P_D we get

$$\Delta T_{C-A}^{p} = P_D R_{th}^{p}$$

and

$$\Delta T_{C-A}^{e} = P_D R_{th}^{e}$$

For the dimensions shown in Figure 5-15, the ratio is equal to

$$\frac{\Delta T_{C-A}^{p}}{\Delta T_{C-A}^{e}} = 1.89$$

Hybrid operation in a system where the thermal analysis was performed with a wrong assumption, that the power is dissipated by the entire case surface, may be seriously jeopardized. For the analyzed example the actual case-to-ambient temperature rise will be almost double that of anticipated value. If we postulate that the case-to-ambient thermal resistance calculated with the wrong assumption is

$$R_{th}^{c-a} = 0.68°C/w$$

and the power dissipation is $P_D = 75$ watts, we find that

$$\Delta T_{C-A}^{e} = P_D R_{th}^{c-a} = 51°C$$

The actual ambient-to-case temperature rise would be

$$\Delta T_{C-A}^{p} = 1.89 \cdot \Delta T_{C-A}^{e} = 96.39°C$$

The differential of

$\Delta T = 96.39°C - 51°C = 45.39°C$

will be added to the actual junction temperature of the semiconductor device. This unexpected temperature deviation may seriously affect hybrid electrical performance and reliability. In some cases it may cause the transistor or diode overstress and failure.

As we saw earlier, the actual thermal performance of the power hybrid circuit depends on a variety of conditions and may deviate within wide margins. Hybrid designers use several direct measurement methods to evaluate hybrid's thermal performance. Two distinctively different ways, which proved most accurate and reliable, are described in the following paragraphs.

5.5.1— Electrical

The electrical method of measuring the temperature of an operating semiconductor device uses a temperature sensitive electrical parameter (TSEP). The major advantage of this method is that it can be performed on a sealed unit accurately and fast. A TSEP is selected for each type of the tested power device — diode, bipolar transistor, MOSFET, etc. Typical TSEP parameters are:

• Diode — V_F, forward voltage drop

• Bipolar transistor — V_{BE}, base-emitter voltage at small constant current

• MOSFET — V_F, forward voltage of the intrinsic source drain diode

The device under test is calibrated prior to the measurement. The TSEP is measured at very low currents at different temperatures to establish the reference curve TSEP = f(T°C). This is accomplished by heating the device using an oven or temperature controlled hot-plate. Sufficient soaking time is necessary to ensure that the device reaches the measured temperature level. The TSEP is measured with a very low current applied. During the measurement a heating pulse is applied to the device for a predetermined duration, sufficient to raise its temperature by the dissipated power to a steady-state level. After turn off of the heating power pulse and a very short delay, the value of TSEP is measured at the current levels identical to calibration values. The average junction temperature is found by superimposing the measured value of TSEP on the calibration curve. A distinctive advantage of this method is, that by varying the duration of the heating pulse the quality of the die attach can be characterized. The pulse is made short enough, so that the generated heating energy has just enough time to propagate to the die attach material. Unlike the thermal resistance test, the die attach evaluation is transient where the temperature does not reach the steady-state level. Therefore the junction temperature shall represent the quality of the die attach — better bonded die shall have lower temperature. To characterize the thermal resistance of the entire assembly, the pulse duration is increased to allow heat flow through to the case. Use of this method is usually limited to a single semiconductor device or simple assemblies of power chips. It requires physical access to the power device terminals, which may not be available in more complex power hybrids. It is also desirable that the terminals should not be connected to other semiconductor elements, presence of which can distort the measurement. The electrical method is widely used by the manufacturers of power semiconductor devices and simple power chip assemblies. It can be used to accurately characterize thermal characteristics under steady-state or transient conditions. It is fast, accurate, and cost effective, and easy to use in the production environment.

5.5.2— Thermal Imaging

The infrared thermal imaging technique enables the designer to generate a quantified thermal map of the power hybrid circuit during operation. It allows to display temperatures of all visible elements of the hybrid — conductors, substrates, wire-bonds, wires, package leads, semiconductor devices, resistors, capacitors and magnetics. The major disadvantage of the infrared imaging method is that it requires that the tested device be unsealed (case cover removed) to allow visible

access to its components. It is time consuming and requires expensive equipment.

5.5.2.1— Fundamentals of Infrared Radiation

Infrared energy propagates through space at the speed of light as an electromagnetic wave. The location of the infrared region in the electromagnetic spectrum is shown in Figure 5-16. It covers the wavelength range from $0.75 \cdot 10^{-6}$ meters to about $1000 \cdot 10^{-6}$ meters and is located between visible light and microwaves. This range is divided into three segments — near infrared (0.75 μm to 1.5 μm), middle infrared (1.5 μm to 7 μm) and far infrared (7 μm to 1000 μm). The infrared radiation is naturally emitted by all objects because of the thermal agitation of their molecules. The intensity, frequency, and wavelength of infrared electromagnetic energy is determined by the temperature, size, and emissivity of the source. When the infrared energy emitted by the source hits another object, portions of this energy are transmitted, reflected or absorbed causing heating of that second object. When most of the transmitted infrared energy is transmitted through the object, it is considered transparent. If most of the energy is reflected, then it is considered mirrorlike. Other materials absorb most of the energy. Materials that are good transmitters or reflectors of the infrared energy are poor emitters and absorbers of such energy.

One of the most fundamental principles of infrared radiation is known as Kirchoff's Law, which is a consequence of the fact that in order to remain in equilibrium with its surroundings, the energy radiated by an object must be equal to the energy absorbed. A perfect absorber — "black body" is also the best available emitter with emissivity $\varepsilon = 1.0$. A "black body" can be closely approximated by a small aperture "a" in a large enclosure "B" whose internal walls are blackened and kept at a constant temperature as shown in Figure 5-17. Even if the absorptivity of the blackened walls is less than unity, the radiation energy entering the aperture will undergo numerous internal reflections and be completely absorbed. The concept of black body is very important, not only because it is the most efficient radiator but also because the total radiant power and the spectral distribution of this power depend only on the temperature. This property makes the black bodies very useful for calibration of equipment. The radiation of infrared energy covers a wide range of frequencies and wavelengths. The wavelength at which the radiation energy peaks is determined by the temperature of the body as shown in Figure 5-18. As the temperature increases, the peak radiation shifts to shorter wavelengths and the total amount of the radiated energy increases. The radiation characteristics shown in Figure 5-18 are described by three basic laws, which are widely used to determine the characteristics of target radiation. These laws are thoroughly reviewed in physics textbooks and are very briefly summarized below.

Stefan-Boltzmann law gives the total radiation energy emitted into a hemi-

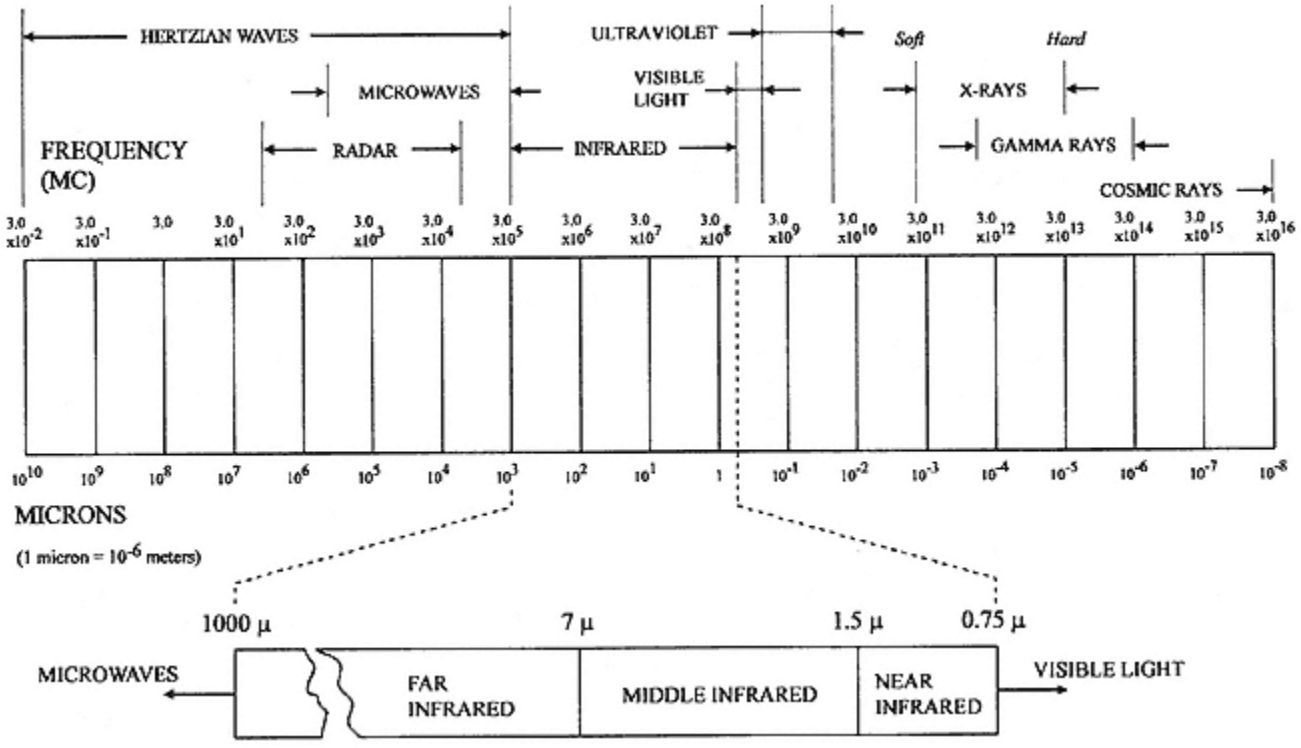


Figure 5-16
Location of infrared region in the electromagnetic spectrum.

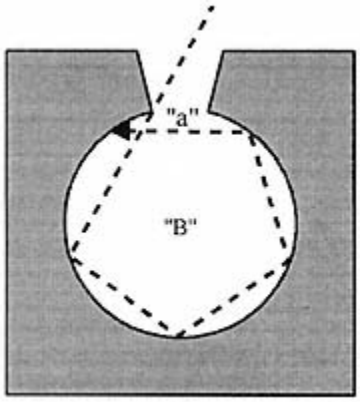


Figure 5-17
Black body is approximated by a
small aperture in a blackened cavity.

sphere from a black body of unit area at uniform temperature:

$W = \varepsilon\sigma T^4$

where

W = Radiant flux emitted per unit area, watts/cm^2
ε = Emissivity
σ = Stefan-Boltzmann constant (5.67×10^{-12} watts/cm^2 °K^4)
T = Absolute temperature of source (°K)

As the target temperature increases, the wavelength at which it emits the most energy becomes shorter. Wien's Displacement Law specifies the wavelength at which this maximum radiation is emitted for any specified temperature:

$$\lambda_m = \frac{b}{T}$$

where

λ_m = Wavelength of maximum radiation, μm
b = Wien displacement constant, 2897 μm°K
T = Absolute temperature of source, °K.

Planck's equation defines the spectral distribution of the black body radiation and permits calculation of the radiant emission in any wavelength increment:

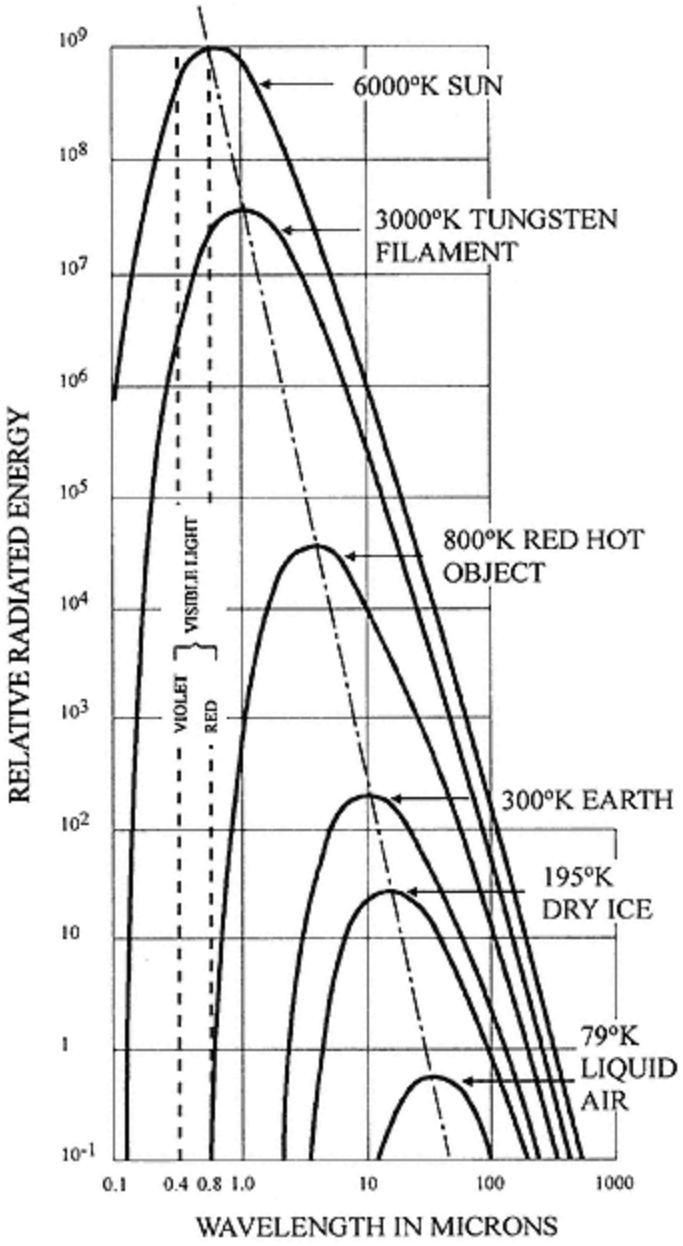


Figure 5-18
Spectral characteristics of black body radiation
from objects at different temperatures.

$$W_\lambda = \frac{C_1}{\lambda^5\left(e^{\frac{C_2}{\lambda T}} - 1\right)}$$

where

W_λ = Radiant flux emitted per unit area per unit increment of wavelength, (watts/cm^2-μm)
λ = Radiation wavelength, μm
T = Absolute temperature of source (°K)
C1 = $2\pi c^2 h = 3.74 \times 10^4$
C2 = h c/k = 1.438×10^4
e = Napierian base = 2.718

5.5.2.2—
Infrared Scanning, Principles of Operation

Infrared scanning provides a method for an accurate, nondestructive, noncontact evaluation of the thermal performance of power hybrids. Figure 5-19 shows a simplified functional diagram of the infrared scanning microscope with peripheral equipment.

The imaging system consists of three major components:

• Imaging

• Control and processing

• Input/output

The imaging section includes high resolution optics, scanning mirrors, and infrared detector. During the operation infrared energy is focused by an objective lens onto the scanning mirrors which sweep the small instantaneous field of view of the infrared detector over the analyzed area. Target scanning is accomplished by motor driven mirrors. One scans in the X direction at a rate of 60 Hz, while the other mirror scans in the Y direction at a rate of 1 to 2 Hz. This produces an image composed of a raster of 64 horizontal lines at a rate of 1 frame per second or 128 lines at a rate of 1 frame in two seconds. The optical chopper is an electromechanical device which periodically interrupts the infrared radiation beam reaching the detector. It is used to generate an alternating electrical signal with amplitude proportional to the absolute level of target radiation. The microscope has a liquid-nitrogen cooled indium antimonide (InSb) detector operating over a 2—5 μm wavelength range which displays images with spatial resolution of 15 μm with a field size of 1.6 mm and a temperature resolution of 0.1°C.

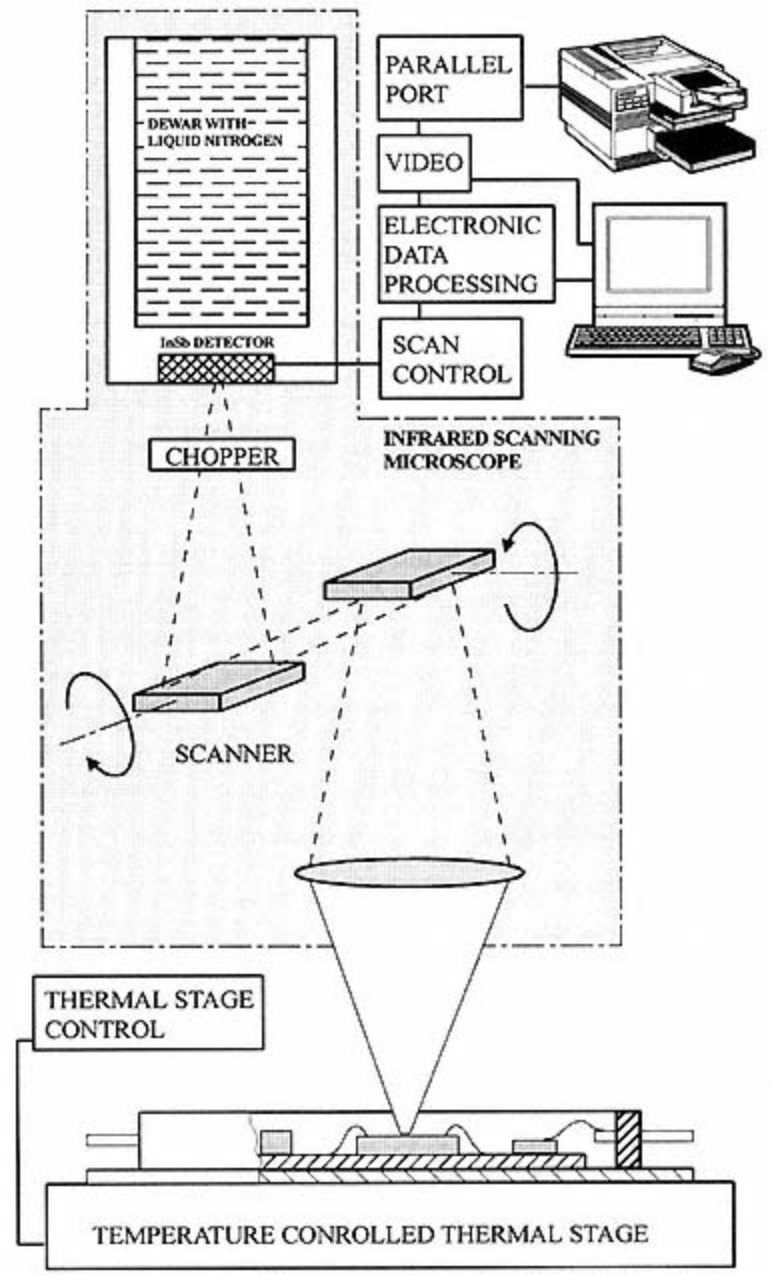


Figure 5-19
Functional diagram of an infrared scanning system.

The data processing part of the system provides necessary calculations and data manipulation to generate an image. Typical basic input/output devices available with computer-based equipment include keyboard, disc drive and monitor. The image can be displayed on the monitor, saved on a disk or printed out on a color or black and white printer. Radiance or temperature values are spread over 16-tone color display range which can be extended to 256 colors or shades of gray. The temperature intervals corresponding to each color are expressed by color bars along the right side of the image. To allow thermal mapping of the hybrid, the set-up must be first calibrated. During this procedure a sample device is placed on the temperature controlled thermal stage. The lens is focused on the unpowered tested device and scans are taken at two different temperatures — for example, 40°C and 85°C. Both radiance scans are stored and used to generate the emissivity image. Great care must be taken to assure that the hybrid temperature stabilized at the stage temperature. A specific emissivity correction value is assigned to each of the 16,384 pixels to be used later to calculate pixel temperature. The radiance measured at each pixel can be found from the following equation:

$$N_M = \varepsilon N_T + (1 - e)\, N_A$$

where

N_M = radiance measured by the instrument
N_A = ambient radiance
N_T = black body radiance corresponding to the unknown surface temperature
ε = emissivity of the sample

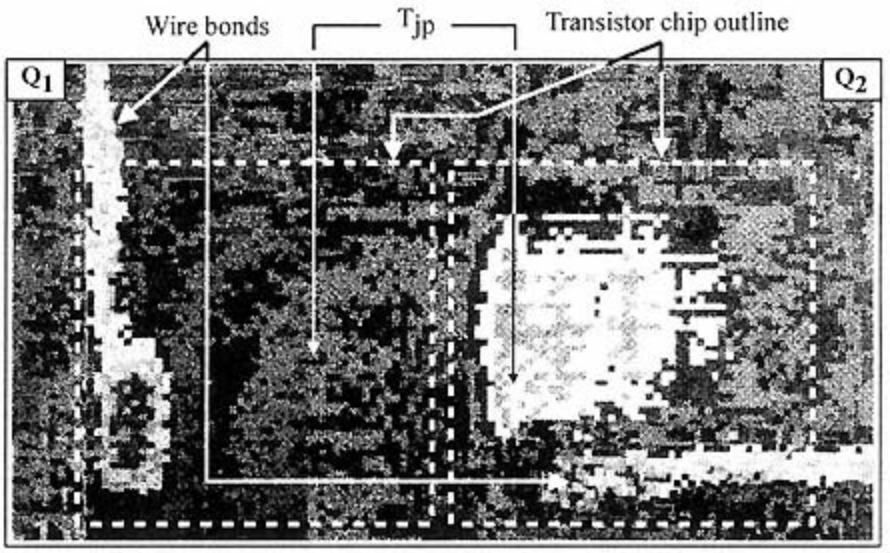
After taking scans at two temperatures T1 and T2, the emissivity can be calculated by using

$$\varepsilon = \frac{N_{M_1} - N_{M_2}}{N_{T_1} - N_{T_2}}$$

After the emissivity is calculated a third scan at a midway point T3 between T1 and T2 is taken. This allows to calculate the ambient radiance component N_A from

$$N_A = \frac{N_{M_{REF}} - \varepsilon N_{T_{REF}}}{1 - \varepsilon}$$

and N_T from



DIE	JUNCTION PEAK TEMPERATURE, T_{jp}(°C)	AVERAGE JUNCTION TEMPERATURE, $T_{j(avg)}$(°C)	AVERAGE TEMPERATURE OF WIRE BOND, $T_{wb(avg)}$(°C)
Q_1	83	67	77
Q_2	167	129	72

Figure 5-20
Typical thermal image obtained by the use of infrared thermal scanning.

$$N_T = \frac{N_M - (1-\varepsilon) N_A}{\varepsilon}$$

where

N_{MREF} = measured radiance with constant temperature reference
N_{TREF} = black body radiance at the temperature of reference scan

The stored emissivity array is later used by the computer to calculate the true temperature of each pixel of the radiance image scanned from an operating device. The resulting color coded image depicts temperature distribution on the surface of the viewed area. Figure 5-20 shows a thermal image of two power MOSFETs connected in parallel. The average temperature on the surface of tran-

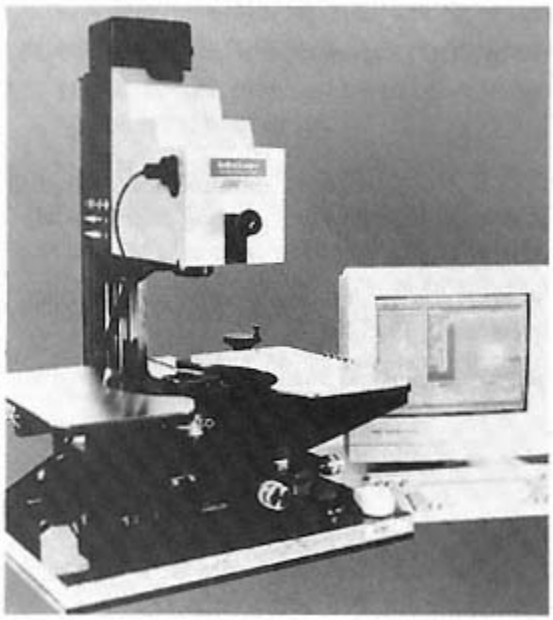


Figure 5-21
Infrared microscope model Infrascope.
(Courtesy of EDO Corporation.)

sistor Q2 is almost two times higher than the average temperature for transistor Q1. The peak junction temperature of transistor Q2 is well above allowable maximum operating temperature. After further investigation, the cause for the excessive heating of Q2 was identified. The metallized pad underneath the chip lost adhesion to the substrate and significantly lowered the cross-section of the heat path. It is important to note, that the x-ray inspection did not indicate the loss of contact. This case clearly demonstrates the usefulness of thermal imaging in evaluation of performance of power hybrids during the engineering development phase. It is also very useful in the manufacturing cycle of high reliability hybrid circuits.

The thermal imaging equipment provides a number of other options:

- Split screen for image comparison
- Temperature averaging in a selected area
- Window zoom
- Automatic calculation of emissivity
- Temperature mapping in the entire viewing area

• Analog temperature distribution along the horizontal cursor line

The Infrascope manufactured by EDO Corporation is shown in Figure 5-21.

References

1. Pecht, M., Lall, P. and Whelan, S., "Temperature Dependency of Microelectronic Device Failure," Quality and Reliability Engineering International, vol. 6, 1990.

2. Kraus, A. and Bar-Cohen, A., *Thermal Analysis and Control fo Electronic Equipment*, McGraw-Hill, New York, 1983.

3. Eckert, E. and Drake, R., *Analysis of Heat and Mass Transfer*, McGraw-Hill, New York, 1972.

4. Mahalingam, M., "Surface-Mount Plastic Packages—an Assessment of Their Thermal Performance," IEEE Trans. Components, Hybrids, Manuf. Technol. CHMT-12(4):745–752, 1989

5. Buchanan, R. and Reeber, M., "Thermal Considerations in the Design of Hybrid Microelectronic Packages," Solid State Technology, 1973.

6. Elsby, T., "Thermal Characterization of Epoxy and Alloy Attachments of Hybrid Components," 27th Electronic Components Conference, Arlingto, Va., 1977, pp. 320–323.

7. Furkay, S., Kilburn, R. and Monti, G., eds., *Thermal Management Concepts in Microelectronic Packaging*, ISHM, Silver Spring, Md., 1984.

8. Bar-Cohen, A. and Kraus, A. D., ed., *Advances in Thermal Modeling of Electronic Components and Systems*, Vol. 1, Hemisphere, New York, 1988.

9. Ellison, G., *Thermal Computations for Electronic Equipment*, Van Nostrand Reinhold, New York, 1984.

10. Elliot, T., "Infrared Measurement of Surface Temperature Now Hot Option," Power, March 1988, pp. 41–48.

11. Kallis, J., Strattan, L. and Bui, T., "Programs Help Spot Hot Spots," IEEE Spectrum 24(3): pp. 36–41, 1987.

12. Hussein, M. M., Nelson, D. J. and Elshabini – Riad, A., "Thermal Management of Hybrid Circuits: Effect of metallization Layer, Substrate Material and Thermal Environment," ISHM, Annual International Symposium on Microelectronics, 1990.

13. Thomas, E., Weil, M., Lippincott, A. and Johnson, W., "Insulated Metal

Substrates for Power Hybrids," ISHM, Annual International Symposium on Microelectronics, 1990.

14. Taraseiskey, H., "Infrared for Hot Hybrid Analysis," New Electronics, September 1989, England, pp. 17–18.

15. Fick, H. J., "SMT Substrates for High-Wattage Devices," Powertechnics Magazine, December 1990, pp. 14–19.

16. Clark, M., Langley, J., Lopuch, S., Majewski, J. and Vorhaus, J., "Thermal Design in Solid-State Microwave Power Amplifiers," Microwave Journal, December 1985, pp. 127–132.

17. Frey, R. and Kane, M., "Temperature Effects Examined for Microwave Power-Transistor Performance and Thermal-Design Considerations," MSN & CT, November 1985, pp.66–77.

18. Gillett, J. E., "Better Heat Flow Analysis on Spreadsheets," Machine Design, January 1989, pp127–132.

19. Simons, R. E., "Thermal Management of Electronic Packages," Solid State Technology, October 1983, pp. 131–137.

20. Sergent, J. and Schuyler, D. R., "Thermal Analysis Helps Keep Hybrid Microcircuits Cool," Electronic Packaging and Production, October 1982, pp. 67–75.

21. Kaye, H., "Junction Temperature Planning Boosts Product Reliability," EDN, April 1985, pp. 225–236.

22. Pound, R., "How to Manage Heat Flow in a Hybrid Package," Hybrid Circuit Technology, May 1990, pp. 54–57.

23. Designing With Beryllia, Engineering Seminar, National Beryllia Corp., 1976.

24. Antonetti, V. W. and Yovanovich, M. M., "Thermal Contact Resistance in Microelectronic Equipment," International Journal for Hybrid Microelectronics, Vol. 7, No. 3, ISHM, Silver Spring, Md., September 1984, pp. 44–50.

25. Min, Y. J., Palisoc, A. L. and Lee, C. C., "Transient Thermal Study of Semiconductor Devices," Fourth Annual IEEE Semiconductor Thermal and Temperature Measurement Symposium, Proceedings, 1988, pp. 82–87.

26. Handbook of Infrared Radiation Measurement, Barnes Engineering Company, 1983.

27. Boulton, H., "Thermography Systems for PCB Testing Applications, Elec-

Table 2-2 Typical characteristics of chip capacitors

Characteristic	Ceramic chip capacitors			Solid electrolyte tantalum capacitors
Dielectric type	NPO	X7R	Z5U	
Capacitance range	1 pF to .039 µF	100 pF to 5 µF	2700 pF to 1.5 µF	0.1 µF to 330 µF
DC rated voltage range	50 V to 5000 V	50 V to 2500 V	25 V to 50 V	2 V to 50 V
Dimensions (mils)	50 × 40 to 360 × 400	50 × 40 to 360 × 400	80 × 50 to 220 × 250	100 × 50 to 235 × 23.

characteristics and is limited only to the value and rated voltage. Listed below are important factors involv in the selection of capacitors:

- Capacitance value and tolerance
- Rated voltage - DC, AC, peak, and surge
- Physical dimensions
- Temperature limits
- Equivalent series resistance (ESR)
- Temperature coefficient of capacitance (TCC)

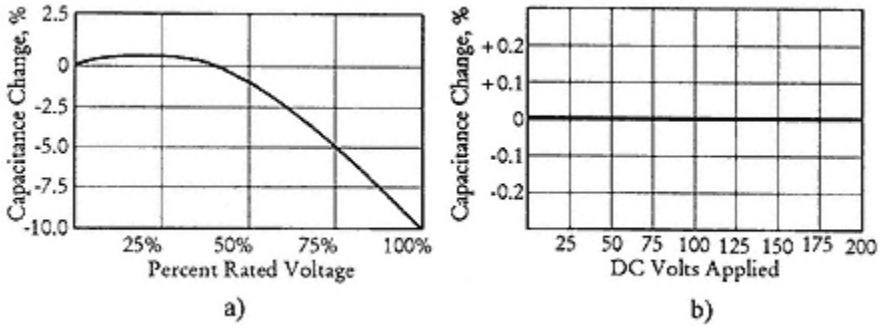


Figure 2-10
Variation of capacitance with applied DC voltage:
a) X7R dielectric, b) NPO dielectric.

tronics," April 1985, pp. 23–25.

28. Basics of Practical Infrared Radiation Measurement, Report WS 82-3, Wahl Instruments, Inc.

29. Siegal, B. S., "An Alternative Approach to Evaluating Die Attachment Quality," Hybrid Circuit Technology, January 1984, pp. 43–48.

30. Boulton, H., "Testing Hybrids Using Thermography," Hybrid Circuit Technology, July 1984, pp. 61–65.

31. Burggraaf, P., "IR Imaging: Microscopy and Thermography,", Semiconductor International, July 1986, pp. 58–65.

32. Crall, R. F., "Thermal Imaging—Reliability Analysis," PC Network, February 1990, pp10–27.

33. Blackburn, D. L., "A Review of Thermal Characterization of Power Transistors," Fourth Annual IEEE Semiconductor Thermal and Temperature Measurement Symposium, Proceedings, 1988, pp. 1–7.

6—
Manufacturing

6.1—
Introduction

Manufacturing of power hybrids can be described as a process which involves intellectual and physical labor and is intended to bring forth a product made of separable and identifiable elements by forming, combining and processing materials.

This chapter is devoted to a description of processes and their sequence in a manufacturing flow of a high reliability power hybrid. A reader interested in the description and analysis of manufacturing organizational structures and production techniques used in modern industry is referred to the considerable volume of available publications on that subject.

6.2—
Manufacturing Flow

The modern manufacturing process involves a large multifunctional team efficiently operating in a well coordinated manner. The process starts with an engineering release of the manufacturing product database and tooling to production, as illustrated in Figure 6-1. It is highly desirable that a small quantity of the final version of the product be manufactured and thoroughly tested by that time. This prevents the jeopardy of unexpected, last moment problems. The manufacturing database as a minimum consists of:

Figure 6-1
Power hybrid manufacturing organization.

- Detail documentation
  - bill of materials
  - component specifications
  - case and lid drawings
  - substrate fabrication drawings
  - assembly drawings with marking instructions
  - acceptance test procedure
  - dynamic trim procedure, when applicable
  - burn-in procedure
  - manufacturing flow card
  - pre-production test data
- Test fixturization
  - test fixtures
  - dynamic trim fixture, when applicable
  - burn-in fixtures
  - miscellaneous fixtures (thermal test, vibration and shock test, etc.)
- Tooling
  - assembly fixtures (solder reflow, holding, etc.)
  - lid sealing fixtures
  - lead forming fixtures
- Quality provisions
  - reliability requirements
  - environmental testing definition
  - qualification testing requirements and procedures
  - MTBF calculations

Each document and every piece of hardware are reviewed and signed-off by the manufacturing engineering department. Prior to commencement of production cycle the program office develops the manufacturing plan and establishes the program logistics, such as operations plan, mission scenarios and costs. With release of the purchase order the purchasing department procures materials, piece parts, tools, and fixtures necessary for production. As the material on order is delivered, it is inspected at the incoming inspection, tested and placed into kits. The kit remains in stock until release to production facility in accordance with the manufacturing plan. That initiates the power hybrid manufacturing cycle.

Table 6-1 Power hybrid component and assembly process summary

Designation	Component description	Wire bonding		Die bond	
		Au	Al	epoxy	solder
Substrate 1	Digital section	•		•	
IC_1 to IC9	Integrated circuit	•		•	
$C_{1,2,3}$	Capacitor			•	
$R_{1,2,3,4}$	Thin-film chip resistor	•		•	
Substrate 2	Analog section	•		•	
IC_{10}	Integrated circuit	•		•	
$Q_{1,2,4}$	Transistor	•		•	
$CR_{1,2,3}$	Diode	•		•	
C_4	Capacitor			•	
$R_{5,10}$	Thin-film chip resistor	•		•	
$R_{6,7,8,9}$	Thick-film resistor				
L_1	Miniature inductor	•		•	
Substrate 3	Power section	•	•	•	•
Q_3	Transistor	•		•	
$Q_{5,6}$	Power transistor		•		•
$CR_{4,5}$	Diode	•		•	
$CR_{6,7}$	Power diode		•		•
$R_{11,12}$	Thin-film chip resistors	•		•	
$R_{13,14,15}$	Thick-film resistors				
Tab	Molytab		•		•

The hybrid shown in Figure 4-7 and Figure 4-9 is used as a basis for the manufacturing flow definition. To assist in the understanding of hybrid construction, the essential information about the circuit and processes used in component assembly are summarized in Table 6-1. The hybrid includes three separate ceramic substrates mounted in a flatpack case with molybdenum bottom. It has 32 I/O pins sealed in the alloy #52 sidewall with matched glass. The sidewall is brazed to the bottom and then plated with gold. In the final hybrid configuration the leads must be formed upwards extending by 0.5 inches above the cover.

A simplified manufacturing flow chart is presented in Figure 6-2. This flowchart delineates good manufacturing practices and requirements of governing

military or other high reliability standards. It is by no means all-inclusive and should be altered to address characteristic conditions of a specific manufacturing facility.

The manufacturing operations are represented by a rectangle with a description of each step. The following list briefly explicates the operations and processes in a sequence shown in the flowchart (Figure 6-2).

(1*)—
Material Procurement

Bill of materials is used to procure all piece parts and materials necessary to produce the product. Source or specification controlled documents accompany the purchase orders. As a good practice, procurement is limited to approved vendors, who proved to be consistent and reliable in performance over time. For a large volume manufacturing, the delivery of material can be scheduled to accommodate the manufacturing plan requirements. Most high reliability programs require that the piece parts originate from a homogeneous manufacturing lot with a traceability record.

(2*)—
Incoming Inspection

All piece parts are visually inspected after delivery. The main objective includes a confirmation to the specification requirements, such as topology and mechanical dimensions. Parts are then scanned for defects, such as cracks, chipouts, etc. Materials are inspected for correct composition and age. Samples of material are also tested for performance. The base and plating materials, as well as, plating thickness is evaluated by destructive testing of cases and lids. They are also tested for corrosion resistance, wire-bondability and solderability of package leads. Visual inspection of packages includes, mechanical dimensions and plating and brazing defects.

A sample of each component is assembled and electrically tested for compliance with the specification. If required by the program, parts are burned-in and retested. Data before and after burn-in is used to calculate parameter deviations — the delta limits, which are used as accept-reject criteria.

(3*)—
Stock

The inspected and accepted material is placed into stock for storage. All components are labeled and held in cabinets with dry nitrogen atmosphere.

(4*)—
Kit Preparation

The manufacturing of power hybrids is carried out in production lots. Lot size is determined by the manufacturing plan, process flow, delivery commitments and manufacturing capacity. Kits are prepared to provide sufficient material (including anticipated yield losses) to produce one or several lots of hybrids. They are assembled based on the bill of materials of the latest revision and all outstanding and approved change notices. When the program requires traceability, all pack-

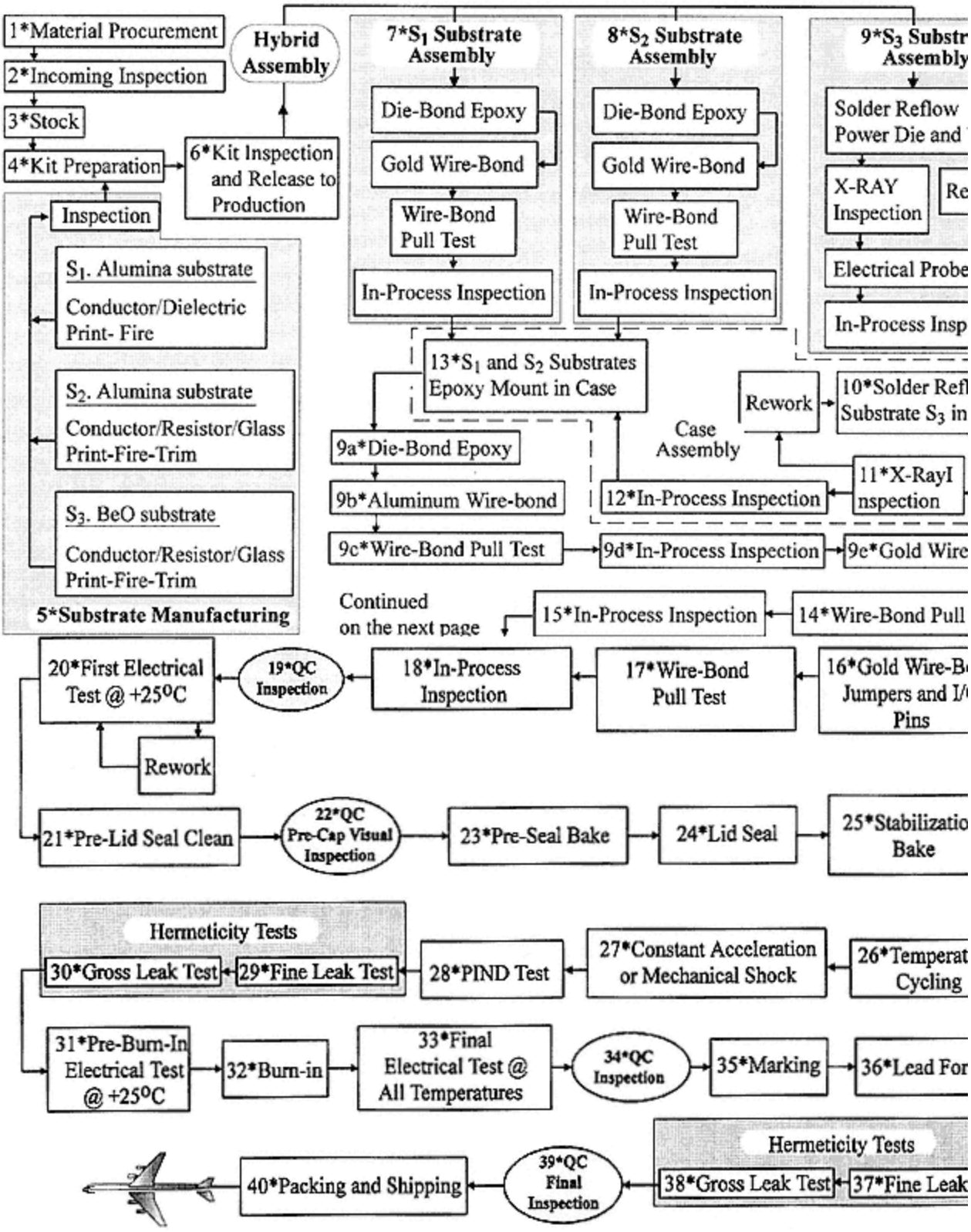


Figure 6-2
High reliability power hybrid manufacturing flowchart.

ages with components and chip carriers are clearly marked with the pertinent information, such as manufacturer's lot number, log number, etc. Homogeneous material is packaged separately so that different lots are not mixed together.

(5*)—
Substrate Manufacturing

Alumina Substrate S_1

This substrate is a thick-film multilayer printed an Al_2O_3 ceramic. The ceramic may be intended for a single or multiple substrate depositions. For a single substrate print it has to be cut to size as specified on the substrate drawing. For a multiple substrate print a large ceramic plate with laser scribe break lines is used. After deposition is completed the large ceramic plate is broken into individual substrates. The conductor and dielectric pastes are deposited, fired and fired in the furnace in a sequence shown on the substrate drawing. It typically is: conductor print-dry-fire-inspect, dielectric print-dry-fire-inspect, metal fill print-dry-fire-inspect, second conductor layer print-dry-fire-inspect, and so on. During the print the paste is deposited onto the ceramic substrate or previous layer via a mesh screen. It is dried on a belt oven and fired in a furnace profiled for the appropriate material.

Alumina Substrate S2

This is a single layer thick-film substrate with screened resistors. The deposition sequence typically is: conductor paste print-dry-fire-inspect, resistor paste print-dry-fire-inspect, glass paste print-dry-fire-inspect. An individual screen is used for resistor pastes with different sheet resistivity. The same applies when different conductor pastes are used. After completion of the deposition phase, the resistor values are brought to value by using the laser trimmer.

BeO Substrate S3

This substrate is using a different ceramic material, which exhibits high thermal conductivity and is most suitable for high power dissipating components. The deposition sequence typically is: conductor paste print-dry-fire-inspect, resistor paste print-dry-fire-inspect, glass paste print-dry-fire-inspect. An individual screen is used for resistor pastes with different sheet resistivity. The same applies when different conductor pastes are used, for example — gold and silver bearing materials. After completion of the deposition phase, the resistor values are brought to value by using the laser trimmer. Special measures must be taken to trim resistors on a BeO substrate. Dust or fumes produced during trimming operation represent a health hazard when inhaled and must be safely vacuumed from the environment and contained.

Inspection

All substrates are visually inspected after completion of deposition and resistor

trimming operations. Screened conductors are thoroughly inspected for the following defects:

• Scratches and voids in the conductor body that expose underlying substrate or dielectric layer and effectively reduce conductor width or size of a bonding pad. Especially important for conductor paths which carry large currents.

• Shorts or very close proximity of two isolated conductors. Particularly critical in high voltage applications.

• Insufficient or defective overlap of two conductors printed using dissimilar materials. A discontinuity can occur in the overlap area. It will exhibit high electrical resistance to flowing current and may fuse into open circuit.

• Correlation between the layer drawing and the screened conductor pattern.

The dielectric is inspected for the following defects:

• Cracks, voids and scratches in dielectric layer which may cause short circuit, excessive leakage or voltage breakdown between adjacent conductor layers.

• Misalignment of dielectric layer which may cause either open or short circuits.

• Correlation between the layer drawing and the screened dielectric pattern.

Resistors are scanned for the following defects:

• Voids, scratches or cracks in the resistor material exposing the substrate and effectively reducing the resistor width. Scratches and cracks in the resistor body may cause resistor latent instability after environmental screening tests. Power resistors have a specified minimum width, which may be violated by the defects.

• Resistor alignment with respect to conductors. Minimum resistor-conductor overlap must be maintained for reliable performance. Close proximity or shorts with adjacent conductors are unacceptable.

• Gross deviation from the design dimensions, which may prevent proper trimming to value.

• Overtrimming of the resistor width beyond specifications, which may cause instability in low power resistors and destruction of high power resistors by excessive heat.

• Resistor values after trim.

• Blistering or peeling of the resistor material from the substrate.

• Location and quality of the trim kerf. No detritus is allowed to remain in the kerf.

• Correlation between the layer drawing and the screened resistor pattern.

Accepted printed substrates are packaged and placed into kits with the rest of the piece parts.

(6*)—
Kit Inspection and Release to Production

Each kit is inspected prior to release to the manufacturing facility for the following:

• Complete set of accompanying documentation including the latest bill of materials, quality assurance provisions and traceability information when applicable.

• Verification that materials and components are properly counted, packaged and labeled with pertinent information.

• When required by the program, all chips are visually inspected using a high power microscope.

Kits accepted for release are signed off, stamped and forwarded to the production control. There the kits are broken down into individual lots and placed in the assembly line.

(7*)—
S_1 Substrate Assembly

Die Bond Epoxy

This operation is used to attach all active and passive components to the bonding pads on the ceramic substrate. The epoxy may be electrically conductive or non-conductive and is selected based on the component configuration. Typically, all semiconductor chips (diodes, transistors, ICs), capacitors and thin-film chip resistors are attached using conductive epoxy. Small components which do not require electrical contact with the mounting pad, still may be attached using conductive epoxy to simplify the assembly process. When a large component, such as a tantalum capacitor or a large ceramic capacitor is mounted, both types of epoxy are used. Conductive provides the electrical contact and the nonconductive, a mechanically strong bond.

The die bond process can be carried-out manually or automatically. During the manual assembly each substrate is handled individually. It is placed on a vacuum chuck, which holds it in place. Then a small amount of epoxy is dispensed onto the bonding pad via the dispenser needle tip. The amount of epoxy depends

on the component size and is controlled by the operator. Employing a vacuum pick up tube, the component is carefully picked-up from its carrier and placed onto the bonding site. A specially designed tool is used over the component surface to orient it as shown on the reference assembly drawing. Thereafter it is pressed down slightly until the epoxy fillet is formed all around the chip. One component type is bonded at a time on all substrates in the lot. Then the process is repeated with another component until all are mounted. All substrates are positioned on a tray and placed into a curing oven for a specified time duration. After curing the epoxy and cooling substrates to the room temperature, the substrates are inspected and placed into a storage container ready for the next operation.

During the automatic die bond operation the epoxy is screened onto the substrate pads using a mesh screen. Then a pick and place machine completes the die bond process. Subsequently the assembled parts are cured in an oven.

The assembled units undergo in-process inspection for the following defects:

• Wrong orientation or position of the die

• Insufficient fillet of epoxy around the chip perimeter

• Bridging of epoxy to the top surface of the die

• Bridging or unacceptable proximity of epoxy to adjacent conductor or pad

• Cracking

Gold Wire-Bonding

Gold wires are used to interconnect the die bonded components with the substrate metallization pattern and provide a path for electrical signals. A bond is formed from the components pad to the conductor bonding site. Bonding mechanism depends on equipment used for this operation. Typical types include ultrasonic, thermasonic and thermal compression wire-bonding. Equipment can be manual or automatic. One substrate is completely wire-bonded at a time. When two types of wire, varying either in composition or diameter, are used, the process is split into individual steps for each wire.

After the lot wire-bonding operation is completed, substrates are subjected to a visual inspection. The criteria varies dependent on the wire-bonding method. However in general the defects are as follows:

• Connection of the bond to a wrong pad

• Evidence of under or over bonding indicating poor setting of the equipment

• Excessive deformation of exit wire

• Evidence of intermetallic formation

• Only part of the wire-bond is overlapping the bonding pad

• Crack in the wire

• Cracking of the silicon in the bond area

• Crossing wire-bonds

• Wire-bonds too closely spaced or shorted

• Wire-bonds to materials not compatible with the process — solder, epoxy, etc.

• Scratches, cuts, nicks or sharp bends in the wire

• Missing wires

• Excessive wire loop height

Wire-Bond Pull Test

A sample or the entire wire-bonding lot is subjected to a nondestructive wire pull-test in accordance with the requirements of the program. The equipment used in this test is adjusted to a setting appropriate to the wire diameter. The setting is in grams. With the substrate secured in the holder, the hook is placed under the wire, the actuating lever is released and the wire pulled for a short duration not exceeding one second. If no failures occur at the preset values, the lot is acceptable. There are three basic modes of failure. First, when the wire breaks at the loop. Second, when the wire lifts from the bonding pad intact. Third, when the wire breaks at the ball or wedge knee. In the event of failure, the lot is rejected and the defective wire-bonds must be replaced.

In-Process Inspection

The substrates with all components, die bonded and wire-bonded, are inspected for compliance with the assembly drawings. The manufacturing card is checked for sign-off by the authorized operator or the supervisor. Units are now placed into storage bins ready for assembly in the power hybrid case.

(8*)—
S_2 Substrate Assembly

This step is identical to S_1 substrate assembly.

(9*)—
S_3 Substrate Assembly

Solder Reflow Power Die and Tabs

One of the most important characteristics that sets power hybrids in a unique class of products is the fact that some of their components dissipate large amounts of power. Heat generated during this process must be effectively removed to ensure continuous and reliable operation of the circuit. Solder material is used to attach the power chip to the substrate or heatsink. It provides a

strong mechanical bond and an excellent thermally conductive interface. The quality of this interface is of great importance to the performance of the chip. Defects in the form of voids can develop during the solder reflow operation. They are caused by poor wetting or entrapment of air and other foreign materials, creating spots with very high thermal resistance, which effectively reduce the chip's ability to dissipate power. A void in the first interface under the power device has the most significant influence on the junction temperature. As the distance from the junction grows, the voids with the same dimensions have less influence. Therefore the void acceptance criteria under the chip has to be carefully defined and enforced.

The location of solder reflow operation on the flowchart is very important. It takes place at temperatures much higher than the curing temperatures of epoxies and thereupon must be assiduously considered. There are several options of consecution to implement this operation:

1. Reflow solder power chips to the substrate outside the case using the high temperature solder. Reflow solder the substrate with power chips into the case using solder material with lower melting temperature. Proceed with the rest of the assembly process.

• Advantages of this method include:

- easy removal of the power substrate from the case for rework

- low temperature solder is used to reassemble the new substrate in case

- easy to pretest the power chips by probing

- simple reflow fixturization

- easy to perform meaningful x-ray inspection of the void content in solder

• Disadvantages:

- labor intensive, adds one extra step

- additional part handling, potential for collateral damage

2. Reflow solder the substrate into the case first using higher melting temperature solder. Reflow solder the power chips onto the mounted substrate using solder material with lower melting temperature. Proceed with the rest of the assembly process.

• Advantages:

- easy to pretest the power chips by probing

- low temperature solder is used to reassemble the new power chip on the substrate

- easy to perform meaningful x-ray inspection of the void content in solder

- simple reflow fixturization

• Disadvantages:

- the entire hybrid circuit must be exposed to high temperature if the substrate has to be removed and replaced

- labor intensive, adds one extra step

- additional part handling, potential for collateral damage

- power chip x-rays may be difficult to read

3. Place power chips with solder preforms on the substrate and the substrate with solder preform into the case. Then reflow solder at one temperature. Both the power chips and the substrate are mounted at the same time. Proceed with the rest of the assembly process.

• Advantages:

- single step operation

- hybrid is exposed to a lower temperature (when compared with the second option) if the substrate or power chip have to be removed and replaced

• Disadvantages:

- complex reflow fixtures

- x-rays may be difficult to interpret

- all solder interfaces must reflow if a rework operation has to be performed

The first method was selected for use in the flowchart due to its obvious advantages over others. A fluxless solder preform is used to attach each power chip and tab to the substrate metallization. Chips and tabs are placed in a specially designed fixture, which helps to locate the parts on the substrate and prevent them from moving during the reflow process. Each reflowed component is held in place by a weight, sufficient enough to prevent its lifting during melting and solidifying of solder. That ensures that the solder interface layer is homogeneous and thin.

Substrates assembled in fixtures are placed on the belt of reflow furnace, which has a carefully programmed temperature profile tailored to the mass, size and quantity of the parts. Best equipped facilities utilize reflow furnaces with hydrogen atmosphere. At elevated temperatures hydrogen acts as a mild flux, removing oxidation and promoting wetting. This process produces highest qual-

ity solder attach. It leaves no residue or contaminants. When hydrogen furnace is not available, the furnace with nitrogen atmosphere yields good results. The third option involves use of solder past (solder powder suspended in flux). The solder is screened onto the substrate and reflowed in air.

X-Ray Inspection

Following solder reflow all substrates are subject to a radiographic inspection. They are placed on top of a photographic film and exposed to a dose of x-rays. Then the film is developed and dried. When traceability of x-rays is required by the program each substrate and the corresponding image are labeled. Voids appear as light spots on darker background. During inspection of the x-ray image, the operator evaluates the size of an individual largest void under each soldered component in accordance with established criteria. The numbers vary from 5 to 10%. Subsequently the total void area is evaluated under each chip. It should not exceed 10 to 15%. This test is subjective and depends on the ability of the operator to accurately evaluate the void area. The test can be made more accurate by using a light sensitive receiver, which quantifies the light passing through the film.

Electrical Probe Test

Power semiconductor devices used in modern electronic systems are typically expensive. When acquired in chip form for use in power hybrid, their price is even higher due to lower manufacturing quantities and additional yield losses. Rework of power chips is a labor intensive process which results in additional yield losses due to handling and exposure to high temperatures. Therefore it is prudent to take steps to lower or eliminate necessity for repairs. A simple electrical probe test at that phase shall screen all components that were either damaged during reflow and handling, or were flawed in the first place. The defective component detected at this early stage can be easily replaced or scrapped without affecting the rest of the assembly.

In-Process Inspection

All accepted substrates are visually inspected under the microscope at 10x–40x magnification for the following items:

- Component orientation
- Component position
- Component tilt or lift
- Solder wetting
- Solder appearance (depends on solder composition)
- Solder presence around the chip perimeter

• Cracks in solder

• Chip-outs on the die

• Die cracking

• Solder climbing to the top surface of the die

• Solder presence on the substrate conductors and bonding pads

Rework

Parts that need rework are sent to the appropriate work station. There they are inspected and reworked or scrapped.

(10*)—
Solder Reflow Substrate S3 in Case

Almost everything discussed in the paragraph about solder reflow of power die and tabs also applies to this operation. The difference shall comprise of assembly fixtures, furnace profile and clamps to hold the substrate in place. The solder preform used under the substrate has a lower melting temperature than the one used in the chip attach.

(11*)—
X-Ray Inspection

All reflowed cases are subject to the radiographic inspection. The process is identical to the one previously discussed, with exception that the x-ray intensity must be set much higher in order to penetrate the additional mass of the case bottom.

Rework

Rejected parts are sent for rework. Parts that cannot be repaired are scrapped.

(12*)—
In-Process Inspection

All accepted cases are visually inspected under the microscope at 10x-40x magnification for the following items:

• Substrate orientation

• Substrate position

• Solder flow around the substrate perimeter

• Solder appearance

• Solder wetting

- Solder climbing to the substrate surface
- solder presence on the substrate conductors and bonding pads

(13*)—
S1 and S2 Substrates Epoxy Mount in Case

Both substrates with die bonded and wire-bonded components are placed on top of the nonconductive epoxy preform in the designated location and clamped together. The substrate position and orientation is carefully observed before the assembly is placed into the oven for epoxy curing. Thereafter, hybrids are cooled and transferred to the next work station or to the storage bin.

(9a*)—
Die Bond Epoxy

All remaining components from the substrate 3 are die bonded to the substrate reflowed in the case. The process is identical to the die bond operation discussed earlier in this chapter.

(9b*)—
Aluminum Wire-Bond

Power transistors, power diodes and tabs are wire-bonded with large diameter aluminum wires. This operation could be done earlier on the substrate level after the electrical probe test step. Then the substrate is connected to the I/O pins using large diameter aluminum wire-bonds. This operation can be performed using manual or automatic equipment.

(9c*)—
Wire-Bond Pull Test

A sample or the entire wire-bonding lot is subjected to a nondestructive wire pull-test in accordance with the requirements of the program. The equipment used in this test is adjusted to a setting appropriate to the wire diameter. The setting is in grams. With the case secured in the work stage, the hook is placed under the wire, and the wire is pulled to a preset value on the gram gauge for a short duration not exceeding one second. If no failures occur at the preset values, the lot is acceptable. There are three basic modes of failure. First, when the wire breaks at the loop. Second, when the wire foot lifts from the bonding pad intact. Third, when the wire breaks at the wedge neck. In the event of failure, the lot is rejected and the defective wire-bonds must be replaced.

(9d*)—
In-Process Inspection

In general, large diameter aluminum wires carry heavy currents. It is essential that they are thoroughly inspected for possible defects:

• Connection of the bond to a wrong pad or component

• Evidence of under or over bonding indicating poor setting of the equipment

• Excessive deformation of the wire at the foot or neck area

• Only part of the wire-bond is overlapping the bonding pad

• Crack in the wire

• Cracking of silicon in the bond area

• Crossing wire-bonds

• Wire-bonds too closely spaced or shorted

• Scratches, cuts, nicks or sharp bends in the wire

• Missing wires

• Straight wire, insufficient loop

• Wire only partially overlaps the bonding area on the I/O pin

(9e*)—
Gold Wire-Bond

Identical to the gold wire-bond operation on the S1 substrate assembly.

(14*)—
Wire-Bond Pull Test

Identical to the wire-bond pull test operation on the S1 substrate assembly.

(15*)—
In-Process Inspection

Identical to in-process inspection operation on the S1 substrate assembly.

(16*)—
Gold Wire-Bond Jumpers and I/O Pins

Gold wire-bonds are used to interconnect conductors on the substrate and between the substrates as shown on the assembly drawing. Small signal connections to the package pins are also made at that time. The wire-bonder used in this operation depends on the wire diameter and available equipment.

(17*)—
Wire-Bond Pull Test

Identical to wire-bond pull test operation on the S1 substrate assembly.

(18*)—
In-Process Inspection

Power hybrid has been fully assembled and is inspected for the last time prior to the first electrical test. Packages with fragile leads may have a tie bar still attached. It must be trimmed off to allow for the insertion into the electrical test fixture. Two major criteria for inspection at this phase are:

• Verification that the assembled hybrid conforms to the assembly drawing

- substrate integrity (cracks, chipouts, etc.)
- substrate position and orientation
- visible damage to conductors, components or wire-bonds
- missing or improperly located wire-bonds
- correct diameter of wire-bonds

- visible damage to the case (leads, sealing surface, glass or ceramic insulators, etc.)

• Removal of all debris or foreign material that may interfere with the electrical test

- solder balls or splatter

- loose wires

- particles of foreign materials (foam, lint, etc.)

All associated paperwork is inspected and prepared for the quality control inspection.

(19*)—
QC Inspection

All hybrids with the appropriate documentation are examined by the quality control inspector. Sign-off is checked for all preceding operations on the travel cards. Paperwork is checked for completeness of data and records of rework. A sample of hybrids is inspected for evidence of damage or contamination.

(20*)—
First Electrical Test

Following approval of the QC inspector the hybrid circuits are forwarded to the electrical test station. Each hybrid should have a lid taped or otherwise secured to the case to prevent handling damage or contamination. A separate paragraph is dedicated to the discussion of test fixturization and testing of power hybrids.

Open (not sealed hermetically) hybrids can be tested only at room and high temperature extreme. Tests at cold temperature cause condensation of moisture in the internal cavity of the hybrid and may lead to erroneous data or damage. It is possible, when required to develop a test environment void of moisture to allow low temperature testing. Nevertheless the value of such tests is questionable. Typically the tests are performed only at room temperature to verify that the hybrid circuit is fully operational and the test data is complying with the specified parameter limits. The test results may be recorded for future reference if required. Hybrids that fail to operate or exhibit out of specification performance are removed from the lot and transferred for troubleshooting and subsequent repairs.

(21*)—
Pre-Lid Seal Clean

The ensuing operation is the last attempt aimed at removal of all loose particles, foreign materials and contamination prior to hermetic lid seal. Both the hybrid assembly and the lid are cleaned at that time. After cleaning all hybrids are inspected and turned over to the QC inspector for the pre-cap visual inspection.

(22*)—
QC Pre-Cap Visual Inspection

To assure that the power hybrid circuits meet the requirements of the visual

acceptance criteria in accordance with the governing standard, a sample of the units in the lot are subjected to a comprehensive visual inspection.

The detailed description of inspection criteria and limits for acceptance or rejection of high reliability power hybrids are summarized in the MIL-STD-883C, Method 2017.

When the program requires source inspection, the approved lot is held for the customer cognizant representative. A photograph of the assembled hybrid may be taken for the record.

(23*)—
Pre-Seal Bake

Hybrids are placed into a vacuum oven and baked for typically 8 hours at 150°C. After completion of bake cycle, the hybrids and the lids are transferred into the lid sealing chamber without being allowed to get in contact with the ambient air.

(24*)—
Lid Seal

Lids are sealed to the case by means of welding. The optimum welding schedule is established by adjustment of the speed of the electrode travel and the energy level. A representative sample is sealed and tested for hermeticity prior to committing the entire lot to the operation. Hybrid is placed on the work holder and secured in place. The welding electrodes are moving on two opposite sides of the lid generating high intensity heat in the place of contact by passing bursts of high energy electric pulses through the electrodes via the lid.

An alternate method for hermetic lid sealing employs brazing of the lid using a preform.

(25*)—
Stabilization Bake

This operation is performed to determine the effect of high temperature storage on the power hybrid without the application of electrical stress. The hybrid lot is placed in a temperature controlled oven for a specified time @ temperature exposure. For example, if the oven temperature is set to 150°C, the time duration is 24 hours.

(26*)—
Temperature Cycling

This test is conducted by exposing the hybrid circuits to extreme temperatures. Power hybrids are built using materials with different characteristics of strength and thermal expansion. Exposure to high or low temperature shall force the materials to expand or contract, imposing a mechanical stress at their interface. Poorly designed or built devices may sustain a permanent damage. The effects of thermal cycling can be observed in cracks, delamination, loss of hermeticity, increased electrical leakage or lower voltage breakdown, rupture of conductors or wire-bonds, etc.

During the test the hybrids are placed into a thermal chamber. The duration

of exposure and the limits are determined by a specified reference. The temperature is lowered and the hybrids are soaked at the low limit for a duration necessary to cool off. Typical value for total ramp-down and soak time is 10 minutes. The temperature is then raised to ambient and held for a specified duration, typically 5 minutes. Next, the temperature is elevated and held at the high limit for 10 minutes. Lastly, the temperature is lowered to ambient and is held for 5 minutes. This concludes one cycle. At least 10 cycles are performed during this test. The minimum/maximum temperature values vary and are determined by the program requirements. The failure of the hybrids to pass this test is concluded by visual examination for mechanical damage and electrical endpoint measurements. An accepted lot is forwarded to the next test.

(27*)—
Constant Acceleration

The main purpose of this test is to screen the devices that have structural or mechanical defects. The devices under test are mounted in carriers specially designed to prevent warping of the case and are placed in the drum rotor. The location in the drum must be balanced along the diameter axis. Each hybrid in the drum is positioned so that the lid is pointing away from the center. The drum is spun for 1 minute with rotational speed calibrated to produce the specified centrifugal force in the Y_1 direction, typically 5,000G. When other force directions (Y_2, X_1, X_2, Z_1, Z_2) are specified, hybrids are remounted in a different plane and the spin repeated. Typical failures after this test include loose wire-bonds, components or substrates.

(27*)—
Mechanical Shock

This test is performed in lieu of constant acceleration when the application may subject the hybrid to a severe mechanical shock. The peak shock levels vary from 500 g for duration of 1.0 ms to 30,000 G for duration of 0.12 ms. The shock tester provides means to prevent mechanical bouncing of the unit after each shock pulse. Hybrid is rigidly mounted to the holder in a specified direction and subjected to 5 shock pulses at the specified level and duration. Following the test the units are inspected for visual damage to the case, leads, seals and lid. Jingling noise during slight shaking of the hybrid indicates loose parts inside the hybrid.

(28*)—
Particle Impact Noise Detection Test (PIND)

Loose conductive particles left in the hybrid after lid sealing may present a danger of circuit damage. Other foreign materials may become a source of outgassing and contamination. Throughout the PIND testing the hybrid circuit is subjected to the following sequence of events:

• Initial pretest shock

• Vibration for a duration of 3—5 seconds

• Co-test shock

• Vibration for a duration of 3—5 seconds

• Co-test shock

• Vibration for a duration of 3—5 seconds

• Co-test shock

• Vibration for a duration of 3—5 seconds

The failure is detected by the threshold detector and recorded by any of the following three systems in the test equipment:

• Oscilloscope

• Audio system

• Visual indicator

Parts failing the PIND test are removed from the lot.

(29*)—
Fine Leak Test

The hermeticity of the hybrid is evaluated during this test. The test equipment includes a vacuum and pressure chamber and a mass-spectrometer leak detector. The tracer gas helium (He) is used as a detection medium. The power hybrid circuit is placed in a sealed chamber, which is then pressurized with He at the specified duration and bomb pressure. At the end of this cycle the unit is removed from the pressure chamber and placed into another chamber connected to a mass-spectrometer type leak detector. After the ambient air is evacuated from this chamber any He gas that was forced into the sealed hybrid is drawn out (helium leak). The leak rate is measured by the leak detector. Acceptable leak rates, bomb pressure, exposure and dwell times are specified by the quality department based on program requirements. Other fine leak test methods may use a radioactive tracer gas instead of helium.

(30*)—
Gross Leak Test

The fluorocarbon gross leak tester includes a pressure/vacuum chamber. Hybrids are placed in the chamber and the pressure is lowered to 5 torr for 1 hour. A volume of fluorocarbon FC-72 sufficient to cover all devices is introduced at the end of this cycle prior to the removal of vacuum. After devices are removed and dried, they are immersed into an illuminated bath filled with FC-40 or an equivalent fluid heated to +125°C ± 5°C. The immersion depth should be more than 2 inches. The immersed unit is observed using a magnifier glass for appearance of bubbles emanating from the hybrid. The observation lasts for 30 seconds. Two or more large bubbles or a string of bubbles is a cause for rejection.

(31*)—
Pre-burn-in Electrical Test

There always is a certain degree of probability that some of the hybrids which failed environmental testing escaped detection. The purpose of electrical test prior to burn-in is to isolate these failures and route them to rework. The other reason, though less typical, for the test is the recording of the pre-burn-in electrical test data. Some high reliability programs require that the hybrid circuits meet the limits imposed on parameter deviation (delta limits) before and after burn-in. Under "normal circumstances" the hybrids are tested at +25°C in accordance with the test specification requirements. The test results may or may not be recorded. When the delta limits are specified, the test results must be recorded and used for calculations after the final electrical test.

(32*)—
Burn-in

All hybrids are subjected to the burn-in test with a purpose to purge marginal devices from the lot. If not detected, these hybrids shall show up as infant mortalities or early failures in the system. To force the failure of such devices, they are stressed at or above maximum specified operating conditions. Special fixtures are designed and manufactured for that test. After loading power hybrids into the fixtures, they are placed in a temperature controlled burn-in oven. Power supply and electrical signals are applied to the circuits during the entire duration of the test. Hot air circulation in the oven helps to maintain equal temperature distribution. It is critical to calibrate the temperature of the hybrid cases particularly when they dissipate large amounts of heat. This calibration depends on the amount of hybrids in the oven, temperature of incoming air, fan speed and hybrid location. Improper thermal balance may cause an unintended hybrid overstress and damage.

A liquid burn-in bath is sometimes used for this test. Hybrids are immersed into fluorocarbon fluid which is continuously circulated through a series of filters and a refrigerating system, which keeps the temperature at a preset point with very high accuracy. Another advantage of this approach is that it keeps the temperature variations in the bath very low. The main disadvantage is expressed by evaporation of fluorocarbon into the atmosphere presenting an environmental hazard.

The burn-in test duration depends on the burn-in temperature and the required reliability level. The typical conditions are: t = 160 hours at T_a = +125°C. The ambient temperature may be revised to a lower number for high power dissipating semiconductor components if the junction temperature raises above the absolute maximum value.

(33*)—
Final Electrical Test

The entire lot of hybrids is tested at all specified temperatures per applicable acceptance test procedure. The test data is recorded and kept with the rest of the

documentation. Delta limits are calculated if applicable. Failure to function or a deviation beyond specified limits constitute a cause for rejection.

Test fixturization may be manual or automatic. The power hybrid package is secured to the heatsink in the test fixture with screws or clamps to ensure an interface with low thermal resistance. The test sockets provide electrical connections to the hybrid pins. Sockets with very low electrical contact resistance should be used in the paths of high current. A correct location for sensing must be selected when output voltages are monitored on these lines. An example is shown on Figure 6-3. Assuming that the test current flowing through this pin is $I_T = 30A$ and the resistance of the shaded area in Figure 6-3 is $R_C = 0.1\ \Omega$ we get that the power dissipated in the pin-socket-wire interface is $P_D = (I_T)^2 \times R_C = 90$ w. The voltage across that area is $V_D = I_T R_C = 3$v. Measuring the output voltage at the sense point, as shown in Figure 6-3, shall eliminate that error. Testing of power hybrids has many unique aspects. They reflect on the design of test fixturization, methods of measurements and involvement of specialized test equipment. The test conditions are formulated so that the hybrid performance is verified with a high degree of confidence of reliable performance in the system. Testing at temperature extremes behests precision monitoring of package conditions. Accurate and reliable method of control is achieved by using a thermocouple attached at a predetermined spot or several spots. Special considerations must be given to the design of the fixture used in the test set-up shown in Figure 6-4. Some good practice guidelines are listed below.

1. Test fixture must provide easy access to the hybrid and test points, wire and cable connectors, and switches.

2. The hybrid heatsink should have mounting holes for screws or clamps.

3. The heatsink must be made from material with high thermal conductivity with surface flatness sufficient to provide good heat transfer from the hybrid.

4. The fixture should allow placing of a microscope for troubleshooting or visual inspection of an open hybrid.

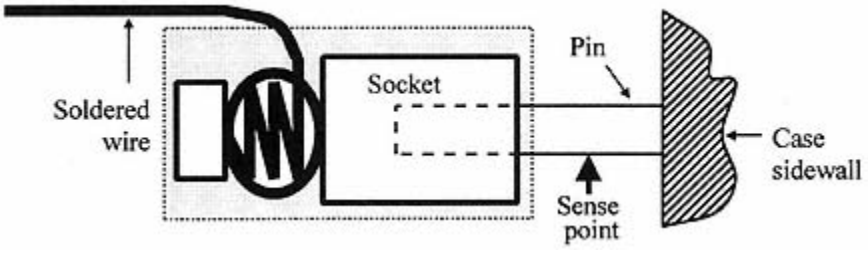


Figure 6-3
Power hybrid pin — test socket interface.

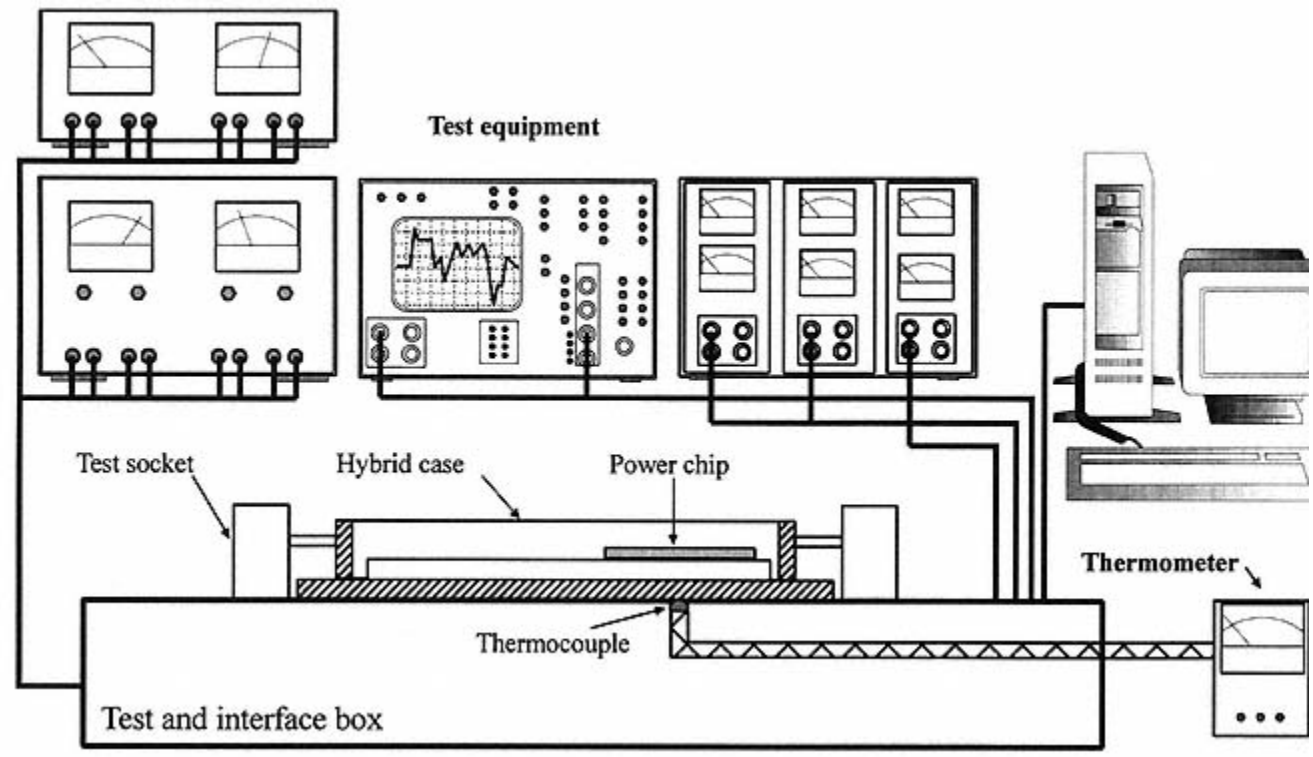


Figure 6-4
Power hybrid electrical test set-up.

5. Test sockets must provide low contact resistance and prevent pin or plating damage.

6. Voltages of high current outputs must be sensed as close as possible to the exit of the pin from the hybrid body to prevent erroneous readings.

7. The heatsink should be grounded or decoupled where practical.

8. High voltage breakdown must be prevented by increasing the spacing of critical lines or insulation. Exposed high voltage connections, which cannot be insulated, must be positioned far away from the operator to prevent accidental contact.

9. High voltage warning label must be placed in a visible location.

10. Wires and cables connecting high current and high voltage lines must be securely locked in place to prevent accidental dismantling.

11. The thermocouple should be attached to the bottom of the hybrid in the vicinity of high power dissipation to accurately measure the case temperature without obstructing the heat flow from the package to the heatsink.

12. Fan may by used to evacuate heat from the heatsink.

13. Heavy wires should be used for high current connections. Power supply lines should be filtered and decoupled close to the power hybrid.

14. Do not run signal wires close to high current, high frequency lines.

Testing at the temperature extremes merits special attention. The majority of packages used in the design of power hybrids are large and heavy. They have a significant thermal capacity and take a long time to heat-up or cool down. Standard thermal steam equipment used in the industry has a limited ability to cool hybrid assemblies. It provides a small shroud, which is placed above the hybrid. Cold air or nitrogen is circulated through the refrigeration system and via this shroud. A thermocouple attached to the controlled surface monitors the temperature. Location of the thermocouple in places other than illustrated shall produce false reading of case temperature. The set-up shown in Figure 6-4 should not be used for thermal testing, unless provisions illustrated in Figure 6-5 are made. If the thermal shroud was placed on the top of the fixture in Figure 6-4, a large portion of the cooling energy would escape, leaving the heatsink exposed to ambient air. While the thermocouple may show the temperature low enough, the temperature inside the hybrid may never reach the specified limit. Use of an insulated enclosure provides the necessary means to ensure that the hybrid is tested at the specified temperature limit after appropriate soaking in the chamber.

All hybrids which pass the electrical acceptance test requirements are collected and forwarded to the next step.

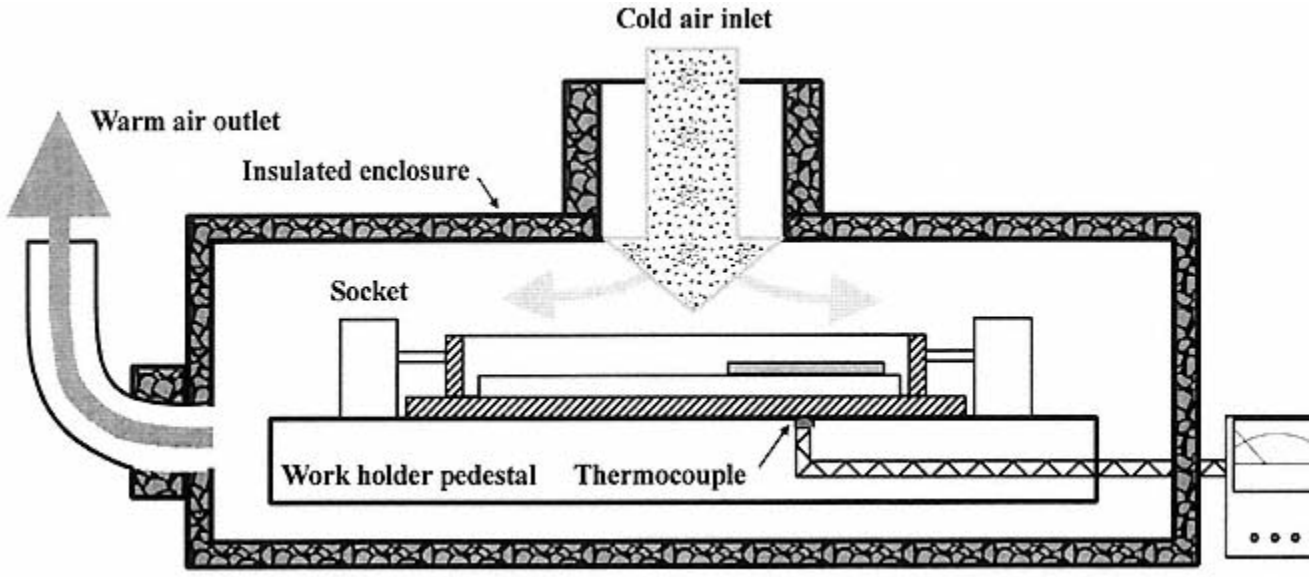


Figure 6-5
Power hybrid testing at high and low temperatures.

(34*)—
QC Inspection

The inspector verifies the completeness of the documentation, test data records, delta parameter calculations, sign-off by the operators, etc. A sample of the lot may be retested at room temperature, when required.

(35*)—
Marking

Marking requirements and practices vary among manufacturers. Nonetheless, the following general information is usually depicted:

• Manufacturer's name

• Manufacturer's logo

• Part description or model number

• Serial number

• Manufacturing lot number

• I/O function description

• Static sensitive device indicator

• "BeO" for hybrids containing beryllia

• Country of origin

Marking may be applied to the lid and the sidewalls lacking pins. The bottom of the case should never be marked with any foreign material. Presence of marking shall obstruct the heat flow and prevent good case-heatsink interface. Materials used in marking are solvent resistant and may be applied by screen printing or other equipment.

(36*)—
Lead Forming

Applications of power hybrids dictate the final appearance of the leads. They may be formed to be inserted into a socket or soldered into a printed circuit board. Leads may be formed upward or downward. Other methods of interconnection in the system include wrapping and soldering of wires and screw-in terminals. Lead forming operation may induce damaging stress in the lead insulators — glass or ceramic. Even though ceramic is less prone to damage than glass, both must be treated with great caution. At that phase the power hybrid consolidates the major bulk of materials and labor and the failure is very expensive. It is beneficial to form leads on a few sample cases to verify the die performance before committing the entire lot. This operation is done manually or semiautomatically. Power hybrid is inserted into the die. First movement of the die clamps the leads to prevent them from moving and minimize damage to the insulators. Then the lead is cut to length and formed to shape. After completion,

the hybrids are inspected for damage to the leads and insulators. Thereafter they are subjected to the hermeticity tests.

(37*)—
Fine Leak Test

This operation is identical to step (29*).

(38*)—
Gross Leak Test

This operation is identical to step (30*).

(39*)—
Final QC

The quality control inspector verifies that all assembly, environmental screening and testing operations listed on the manufacturing card were performed, dated and signed-off. All serial numbers and associated documentation are checked for compliance. The inspector also performs the final external visual and mechanical inspections. He verifies that the dimensions, appearance and marking are in accordance with the applicable drawings. As a minimum the hybrids are visually inspected for the following:

• Correlation of marking information with the drawing

• Proper orientation of marking

• Damage to the leads or other parts of the case, scratches, voids, nicks, etc.

• Evidence of corrosion or other contamination

• Flaking or peeling of the plating

• Cracks in glass

• Cracks or delamination of braze material

• Foreign materials

• Mechanical dimensions

(40*)—
Packing and Shipping

Power hybrid circuits can be packaged in a large container with multiple cells designed to secure the cases during transportation and handling. The packaging material must provide adequate ESD protection and prevent damage to the leads. It is preferred, however, that each power hybrid is packaged in an individual container. The containers are marked with pertinent order information, quantity of hybrids and their description. Warning labels for static sensitive devices are attached in visible locations.

7—
Applications

7.1—
Introduction

Power hybrid circuits are constructed by employing advanced technology to package complex electronic functions. The end use application determines the circuit functionality, outline, reliability screening and cost. Main advantages of power hybrids include reduced weight, excellent thermal management, operating efficiency, small size and reliability. The major impediments are long development cycle and a relatively high cost.

The power modules used in the commercial applications are implemented as a composite of chip and wire assembly with surface mounted discrete components. They are packaged in plastic, nonhermetic enclosures and are specified for the operation in a limited temperature range. These modules are manufactured in large quantities using inexpensive packaging materials and utilizing automated assembly, which significantly reduces product cost.

The criteria in Table 7-1 can assist in the process of selection of the right product for the application.

7.2—
Markets and Applications

The potential market for power hybrids and modules includes the following sectors:

Table 7-1 Advantages and disadvantages of using power hybrids and discrete assemblies

Key consideration	Power hybrids		Discrete assembly	
	Advantage	Disadvantage	Advantage	Disadvantage
Size	Size reduction up to 10-to-1 ratio			Very large
Weight	Significantly lighter			Heavy with large heatsinks
Reliability	Improved			Fair
Maintainability	Easy to replace in the field			Labor intensive
Cost		High	Low	
Electrical performance	Improved		Good	
Thermal performance	Improved		Good	
Availability	Fair		Very good	
Assembly in the system	Simple and fast		Sometimes complicated and time consuming	

- Aerospace
- Military
- Telecommunications and utilities
- Industrial
- Computer
- Automotive
- Consumer appliances

• Medical

Each sector can be classified by the end products specific to the applications. Some of them are listed below:

• Satellites

• Military aircraft

• Tanks and armored vehicles

• Missiles

• Commercial aircraft

• Automatic test equipment

• Power supplies

• Robotics

• Computers

• Switching voltage regulators

• Motor drive controllers

• Consumer appliances

• Electric automobiles

Specific applications for a few selected end users are shown in Figure 7-1.

The main functional applications of power hybrids and modules in the end products can be categorized as follows:

• Motion control

• Power conversion and regulation

• Power signal processing

• Line switching

• Induction heating

Modern electronic systems operate at increasing speeds and consume large amounts of power. They demand effective delivery of power to the load with low losses and efficient thermal management. The opportunities for applications of power hybrids or modules are virtually boundless. Within each category they can be characterized according to their function with either high current switching or high voltage switching. The switching frequencies vary from DC to tens of megahertz.

Space		Reaction wheels, fans, pumps, power tools, robotic arms
Military aircraft and drones		Flight control surfaces, landing gear, fans, pumps, remote power controllers, electrical distribution system, power inverter, radar
Commercial aircraft		Flight control surfaces, landing gear, fans, pumps, remote power controllers, electrical distribution system, power inverter, radar
Missiles and rockets		Fin actuators, rocket boosters
Tanks and armored personnel carriers		Power supplies, remote power controllers
Electric cars		Steering system, drive turbine, braking system, speed control, inverters, solenoid drivers, windshield wipers, climate control

Figure 7-1
End-use applications of power hybrids.

Power hybrids are complex devices utilizing sophisticated technology. Their users mostly have electrical or electromechanical background and in absence of necessary understanding of the product, they tend to reject or reluctantly accept it. Two main functional applications panoply the widest recognition and acceptance of advantages of power hybrids and modules. They are motion control and power conversion and regulation.

7.2.1— Motion Control

Electrical motors provided mechanical drive power for a long time. They drive just about everything from tiny toys to large manufacturing equipment using motors ranging from several milliwatts to tens of megawatts rated power. Recent developments in power semiconductors revolutionized the design and applications of sophisticated modern motion control and drive systems, which include software, digital control electronics, power amplifiers, sensors, and motors. The electronically controlled mechanical drives can be found today in almost every segment of the industry, home and office.

The electric motors include the following types:

• Stepping motors

• DC motors

• Synchronous and brushless DC motors

• Induction motors

Each motor type requires a particular supply configuration for its operation:

• DC motors use DC supply with variable voltage

• Induction, synchronous and sinusoidal brushless DC motors typically use a three phase AC supply with variable frequency and voltage

• Switched reluctance, stepping and trapezoidal brushless DC motors use a supply with pulsed current

The semiconductor power transistors utilized in electronic motor drives must provide low loss during conduction of motor current and infinite resistance when off, and include:

• Bipolar transistors

• MOSFETs

• IGBTs

• MCTs

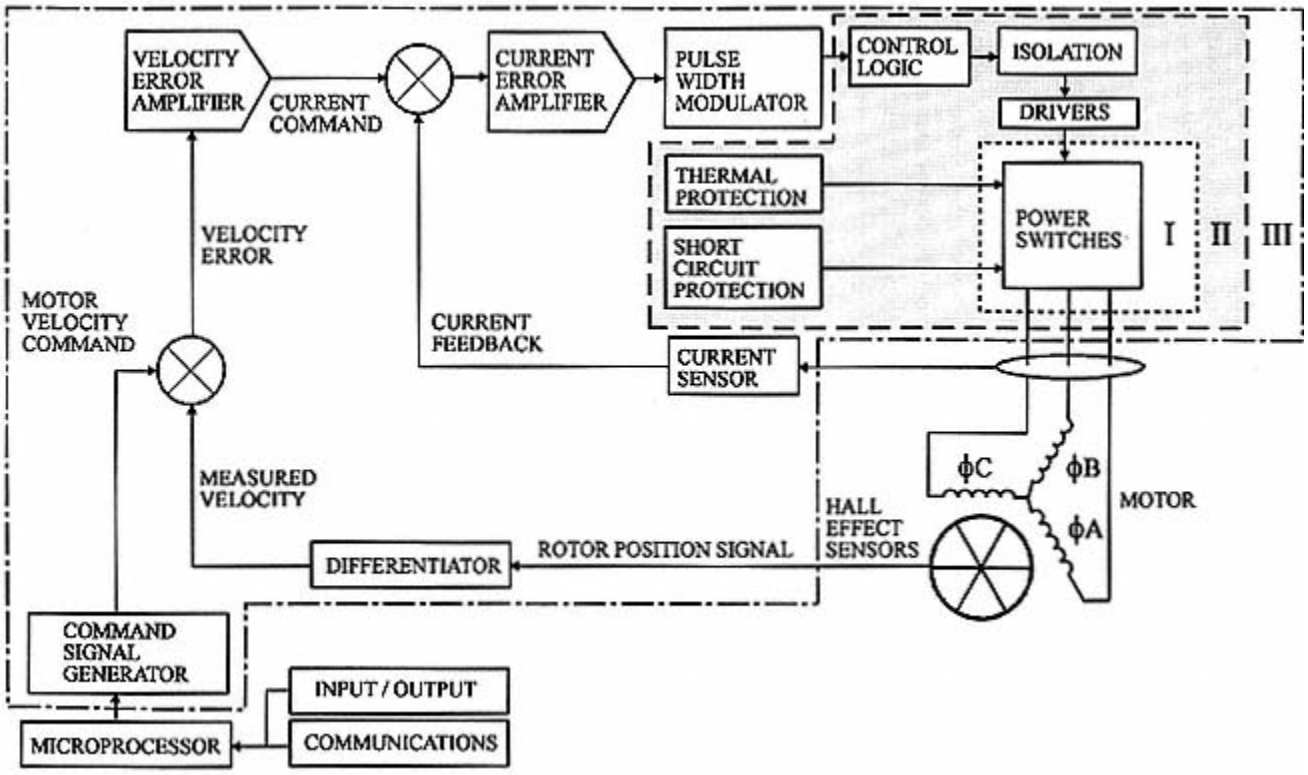


Figure 7-2
Block diagram of brushless DC motor controller-driver.

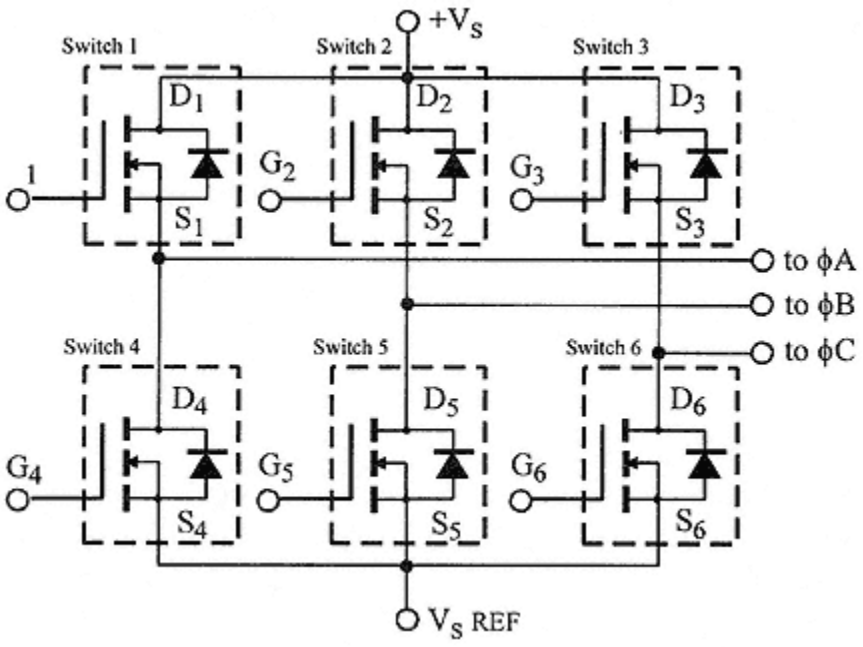


Figure 7-3
Schematic diagram, three phase brushless dc motor driver.

A more detailed description of these components can be found in Chapter 2.

A drive circuit is required to control several parameters of the motion system — torque, speed and position. A block diagram in Figure 7-2 illustrates a typical closed loop electric servo motion system with velocity and current control. The major elements of the system are:

• The servo motor, which converts the winding currents to a mechanical torque producing the motion in the system

• Rotor position sensor provides shaft position feedback to the comparator

• Comparator receives and compares the shaft position signal with position command signal. The position error signal is transmitted to the servo amplifier

• The servo amplifiers convert the comparator signals to currents in the motor windings yielding motor rotation to reduce the position error value to zero or adjust the torque

• Command signal generator provides a series of commands which determine the motion of the system

Table 7-2 Effect of implementation of sections I, II and III on system parameters

Configuration	Size reduction	Weight reduction	Reliability improvement	Cost factor
Section I	High	High	High	Lowest
Sections I + II	Higher	Higher	Higher	Higher
Sections I + II + III	Highest	Highest	Highest	Highest

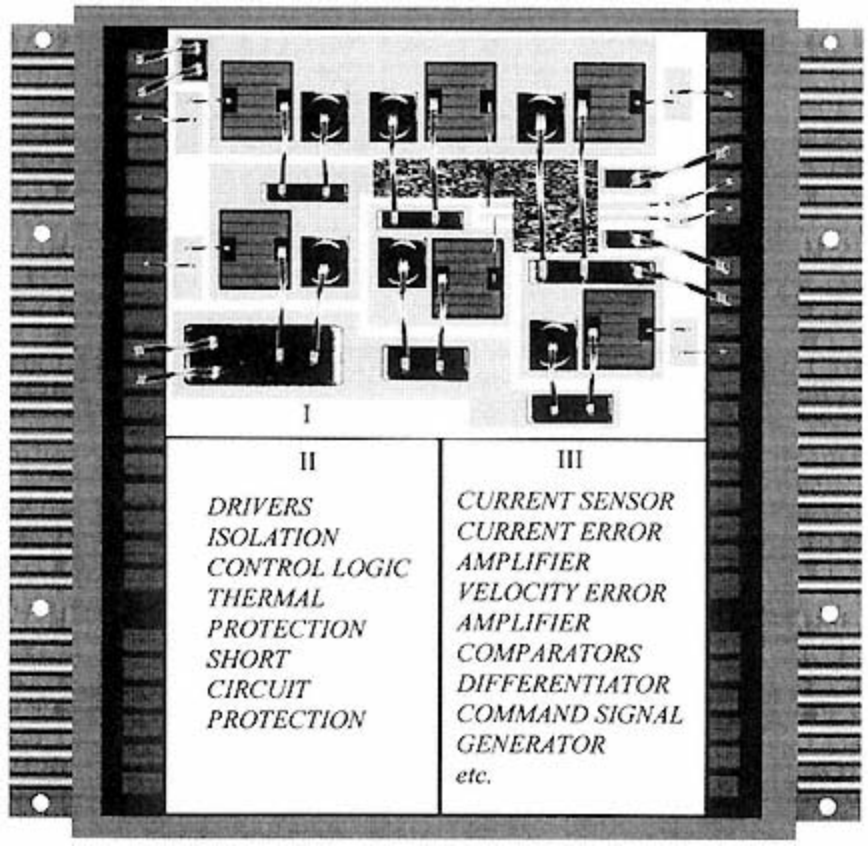


Figure 7-4
Power hybrid partitioning and design.

Three sections in the block diagram are emphasized by broken line confines — I, II and III. Section I includes the power switches in the simplest and most versatile form. The schematic diagram of this section is shown in Figure 7-3. This section is most suitable for conversion into power hybrid. It consists primarily of power semiconductors — MOSFETs and fast recovery rectifiers. Execution of this function by use of power hybrid significantly reduces weight and size with simultaneous improvement in performance and reliability. A small amount

Table 7-3 Power hybrid vs. discrete assembly manufactured by the user, cost of use comparison

Operation	Power hybrid	Discrete assembly
Procurement	Purchasing of a single part. One specification to generate	Purchasing of many parts, labor intensive. Numerous specifications to generate
Incoming inspection: • visual • counting, packing, handling • electrical test • qualification testing • kiting	One part requires very little inspection time	Considerable inspection time is required for a large quantity of parts
Assembly and testing time	Hybrid assembly is fast-only one component must be assembled	The entire circuit consisting of many different parts must be assembled, inspected and tested
Assembly yield	Hybrid is pretested and fully screened. Anticipated yield close to 100%	The assembly yield depends on circuit complexity, manufacturing practices and material quality.
Maintenance and repairability	Simple	Replacement is complicated, particularly in the field
Storage	One part to store	Many parts to store

of other components may be added to the circuit without affecting its simplicity. Figure 7-4 demonstrates how the implementation of each section may affect the appearance of the power hybrid and its essential parameters such as weight, size, performance, reliability and cost. The size of the hybrid doubles in this illustration, when the entire circuit consisting of all three sections are included in the package. Clearly, in different applications the results vary contingent on the circuit complexity. Only the upper section, which is occupied by the power switches (I) benefits from the special characteristics of the hybrid case, such as high thermal conductivity, large diameter leads and mounting flanges. Table 7-2 provides a comparison of implementation of section (I) by itself, sections (I) + (II) and sections (I) + (II) + (III). The cost factor in the table constitutes the price of the hybrid. Frequently, the fabricated power hybrid circuits are compared to discrete assemblies on the basis of bare material cost. To amend this assumption, the actual cost of use of power hybrid in the system is qualitatively compared with a discrete assembly in Table 7-3.

A servo drive system which was implemented as a power hybrid (3.7" long × 1.7" wide × 0.375" thick) is illustrated in Figure 7-5. The hybrid contains analog, digital, MOSFET, and bipolar technologies. This power hybrid circuit provides a position control by comparing the position feedback transducer output to the commanded position. The four main sections include:

• The commutation logic, which decodes the outputs of the motor rotor position sensors to properly switch the motor phases

• The error and compensation amplifiers, which compare the commanded and present position information and whose output (position error) is used to control the pulse width modulator (PWM)

• The PWM uses the position error signal to adjust the duty cycle of a high frequency square-wave, and, through the commutation logic, controls the direction and magnitude of the current in the winding

• The power stage, which takes the low level signals from the commutation logic and provides a properly sequenced voltage at high currents to the motor phases.

The main operating parameters are:

• Maximum supply voltage = 75 VDC

• Position command input signals vary between ± 12 VDC

• Position feedback signals vary between ± 12 VDC

• Output current is limited to 15 Amperes

• Weight = 5 oz

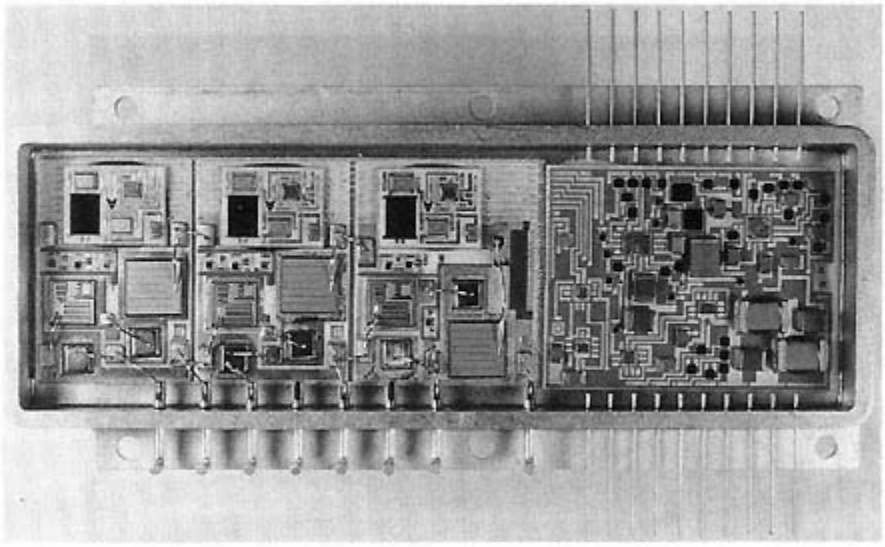


Figure 7-5
Power hybrid — servo drive system. Photo courtesy of Inland Motor, Kollmorgen Corporation.

7.2.2— Power Conversion

Power conversion and regulation represent another popular field of applications for power hybrids and modules. Voltage regulators, power inverters, synchronous rectifiers, and DC-DC converters use power devices to convert, control and deliver to load signals with high currents and voltages. Switchmode power supplies operate at very high frequencies, making use of power hybrid technology advantageous. Issues of electromagnetic compatibility also benefit from shielding provided by the metal case. High reliability hybrid DC-DC converters are shown in Figure 7-6 and Figure 7-7.

Applications vary in performance requirements and other objectives. There are voluminous considerations for and against hybridization of power circuits. Space and airborne applications are very sensitive to size and weight reductions, which eventually lead to significant cost savings. Some systems have unexpected last minute growth requirements, which can be solved only by miniaturization. Others simply do not have enough space to start with. Essential proximity to signal sources or loads in small volumes may lead to requirement of smaller components.

On the other hand, prohibitive cost of high reliability screening of power hybrids prevents their use in competitive, price sensitive applications. If other

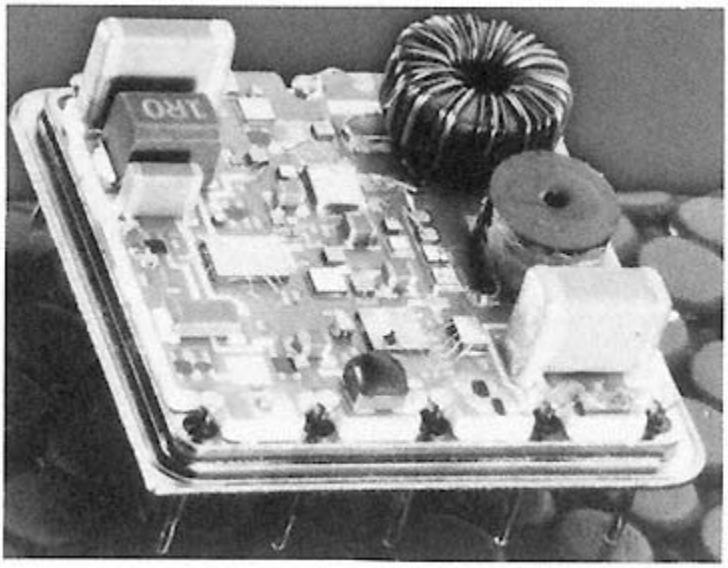


Figure 7-6
DC-DC converter, 11–50 VDC input range, 5 V output. Power density 17 W/in^3. Courtesy of Apex Microtechnology Corporation.

considerations do not apply, the discrete implementation is the right choice.

However, there is a third viable alternative — a relaxation of the specification requisites. When strict compliance with military specifications is not required, the manufacturing process may be considerably simplified, precipitating smaller labor content, higher yields and lower price.

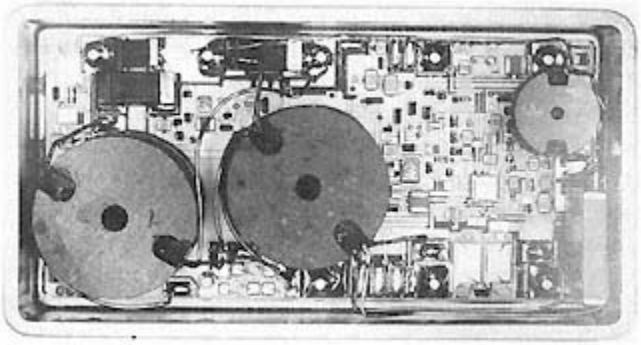


Figure 7-7
DC-DC converter, 17–40 VDC input range. ±12V or ±15V outputs. Power density 12.9 W/in^3.
Courtesy of Lambda Advanced Analog Inc.

Appendix A—
Glossary of Hybrid Microcircuits Packaging Terms

A

ABRASIVE TRIMMING: Trimming a firm resistor to its nominal value by notching resistor with a finely adjusted stream of an abrasive material, such as aluminum oxide, directly against the resistor surface.

ABSOLUTE ZERO: The lowest temperature attainable. All molecular activity is considered to cease. Its value is 0°K (–273.15°K)

AC: An abbreviation for alternating current, which refers to a current that reverses periodically with time and which has alternately positive and negative values.

ACCEPTANCE TESTS: Tests agreed upon by vendor and customer to determine the acceptability of product.

ACCURACY: A statement which is used to define the largest allowable error in a device or system. It is an indication of how close measured values are to the true values. It is expressed in measured units or percentages.

ACTIVATING: A process used to sensitize a nonconductive material to facilitate electroless deposition.

ACTIVE AREA (OF A PACKAGE): Internal area of package bottom, usually a cavity, that actually is used for substrate attachment. The term preferably is applied to package cases of all-metal construction (as opposed to glass or ceramic).

ACTIVE COMPONENTS: Electronic components, such as transistors, di-

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The Glossary of Hybrid Microcircuits Packaging Terms from Handbook of Electronic Package Design by M. Pecht was modified for use in this glossary.

odes, electron tubes and thyristors, which can operate on an applied electrical signal so as to change its basic characters e.g., rectification, amplification, switching.

ACTIVE DEVICES: Discrete devices such as diodes or transistors, or integrated devices, such as analog or digital circuits in monolithic or hybrid form.

ACTIVE ELEMENT: An element of a circuit in which an electrical input signal is converted into an output signal by the nonlinear voltage-current relationships of a semiconductor device (see active components).

ACTIVE SUBSTRATE: A substrate in which active and passive circuit elements may be formed to provide discrete or integrated devices.

ACTIVE TRIM: Trimming of circuit element (usually resistors) in a circuit that is electrically activated and operating to obtain a specified functional output for the circuit (see functional trimming).

ADD-ON COMPONENT (OR ADD-ON DEVICE): Discrete or integrated prepackaged or chip components that are attached to a film network to complete the circuit functions.

ADDITIVE PATTERNING: Processing a hybrid circuit substrate by sequentially depositing conductive, resistive, and insulative materials, each through a mask, thus defining the contours and areas of traces, pads, and elements.

ADDITIVE PROCESS: A process used to selectively deposit electrically conductive material on a clad or unclad base material.

ADHESION: The property of one material to remain attached to another; a measure of the bonding strength of the interface between film deposit and the surface which receives the deposit; the surface receiving the deposit may be another film or substrate.

ADHESIVE: A substance used for film attachment by exerting force of attraction between molecules of mating surfaces in an adhesive bond. In hybrid assembly, adhesives are basically organic polymer compounds, such as epoxies, together with their additives. When hardened after curing, adhesives will bond substrates to packages, or dice and chip carriers to substrate lands, etc.

ALLOY: A combination of two or more metallic elements in the form of a solid solution of one or more metals in another metal, or distinct phases, or components, of an alloy.

ALUMINA: Aluminum oxide (Al_2O_3), a ceramic material often used for substrates or in ceramic bottom construction packages. Most alumina substrates contain 90–99% aluminum oxide.

ALUMINUM NITRIDE: A ceramic material with high thermal conductivity and high electrical resistivity. Used in applications to high power hybrids, and modules, and when high thermal conductivity is required.

AMBIENT TEMPERATURE: Temperature of atmosphere in intimate contact with the electrical part or device.

AMPHOTERIC: Literally, partly one, and partly the other. Specifically, capable of reacting either as an acid or as a base. Amphoteric metallic coating materials may be applied to the backside of silicon VLSI wafers to promote ad-

hesion when die bonding in hybrid assembly.

ANALOG CIRCUITS: Circuits that provide a continuous (vs. discontinuous) relationship between the input and output.

ANGLE OF ATTACK: The angle between the squeegee face of a thick-film printer and the plane of the screen.

ANGLED BOND: Bond impresion of the first and second bond are not in a straight line.

ANNEALING RING: The conductive ring surrounding a hole.

ANNEALING: A method of toughening certain materials and decreasing their brittleness by heating followed by slow cooling; e.g., heating of a film resistor followed by slow cooling to relieve stresses and stabilize the resistor material.

ANODIZATION: An electrochemical oxidation process used to change the value of thin-film resistors or prepare capacitor dielectrics.

ANTI-STATIC: Electrostatic discharge (ESD)–protective material resisting triboelectric charging; usually some form of (impregnated) plastic, identified as anti-tatic, with surface resistivity controlled to be less than 10^{14} Ω/square and more than 10^{9} Ω/square.

ARRAY: A group of elements or circuits arranged in rows and columns on one substrate.

ARTWORK: The accurately scaled configuration or pattern produced usually at an enlarged ratio, to enable the product to be made therefrom by photographic reduction to a 1 : 1 working pattern; layouts and photographic films which are created to produce the working thick-film screens and thin-film masks.

ARTWORK MASTER: A dimensionally accurate imaged pattern (usually mylar or glass) used to manufacture production masters for use in photoimaging processes.

AS-FIRED: Values of thick-film resistors or smoothness of ceramic substrates as they come out of firing furnace and, respectively, prior to trimming and polishing (if required).

ASPECT RATIO: The ratio between the length of a film resistor and its width; equal to the number of squares of the resistor.

ASSEMBLY: A film circuit to which discrete components have been attached. It might also show the assembly of one or more film circuits which may include several discrete components.

ASSEMBLY DRAWING: A drawing showing all the components and interconnections mounted or soldered to the film circuit in their proper positions. It might also show the assembly of one or more film circuits which may include several discrete components.

ATTACH: An inclusive term in hybrid assembly, to denote permanent joining by means of intermediary material(s). Examples are attaching a substrate to case or a device to a substrate.

ATTACH, DEVICE TO SUBSTRATE: The process of fastening devices, components, or elements of a hybrid to a substrate in permanent bond at designated locations, properly oriented. The process varies accordint to physical configurations. Soldering is preferred

for attachment of high power dissipating active and passive component parts; conductive epoxy is the standard method for face-up semiconductor dice and resistor chips; nonconductive epoxy is used primarily for capacitors and inductors.

ATTACH, SUBSTRATE TO CASE: The process of fastening a substrate in permanent bond to the inside bottom of the package case using an intermediary material, with heat applied. The material generally is an adhesive, such as epoxy or polyimide for low power hybrids, while it commonly is a braze, or solder, or eutectic alloy preform for power hybrids.

ATTACK ANGLE: See angle of attack.

AUTOMATIC INSERTION DIP: A dual in-line package which resembles a flat package in which leads are widened at a certain distance to allow bending to form two parallel rows to position the package at a predetermined distance above the board.

AXIAL LEADS: Leads comming out of the ends of a discrete component or device along the centrlal axis rather than out the sides.

AZEOTROPIC SYSTEM: A system of a number of liquid compounds which has specific boiling point for a particular composition.

B

BACK BONDING: Bonding active chips to the substrate using the back of the chip, leaving the face, with its circuitry face up. The opposite of back bonding is face-down bonding.

BACK MOUNTING: See back bonding.

BACK RADIUS: The radius of the trailing edge of a bonding tool foot.

BACKFILL: Filling an evacuated hybrid circuit package with dry inert gas prior to hermetically sealing.

BACKPLANE: Interconnection layer for a multilayer hybrid.

BAKE-OUT: Subjecting an unsealed hybrid circuit package to an elevated temperature to bake out moisture and unwanted gases prior to final sealing.

BALL BOND: A bond formed when a ball shaped end interconnecting wire is deformed by thermocompression or thermosonic bonding against a metallized pad. The bond is also designated a nail head bond from the appearance of a flattened ball.

BARIUM TITANATE ($BaTiO_3$): The basic raw material used to make high dielectric constant ceramic capacitors. Also used in high-ε thick-film ceramic pastes.

BARRELL PLATING: A technique of plating large numbers of small parts in a rotating drum.

BASE MATERIAL: The rigid, or flexible dielectric material, or insulated metal sheet that forms the base for a conductive pattern.

BATCH PROCESSING: Manufacturing method whereby a particular process sequence operates on a large number of components simultaneously.

BATHTUB PACKAGE: A boxlike solid sidewall package wherein the substrate is mounted.

BEAM LEAD: A long structural member not supported everywhere along its length and subject to the forces of flexure, one end of which is permanently attached to a chip device and the other end intended to be bonded to another material, providing an electrical interconnection or mechanical support or

both.

BEADS: See glass preforms.

BEAM LEAD DEVICE: An active or passive chip component possesing beam leads as its primary interconnection and mechanical attachment means to a substrate.

BELLOWS CONTACT: A flat folded spring connector contact providing uniform spring rate over the mating contact tolerance range.

BERYLLIA OR BERYLLIUM OXIDE (Beo): A substrate material widely used in power hybrids where high thermal conductivity is needed.

BIFURCATED CONTACT: A flat lengthwise-slotted contact that permits independent contact points.

BINDERS: Materials added to thick-film compositions and unfired substrates to give sufficient strength for prefire handling.

BLACK OXIDE: A technique for making matched seals by forming a controlled thickness oxide on each of the mating surfaces of a package prior to sealing.

BLANK: A rough-dimensioned printed board cut from a panel of base material that is either unprocessed or partially processed.

BLEEDING: The lateral spreading or diffusion of printed film into adjacent areas, beyond the geometric dimensions of the printing screen. This may occur during drying, or firing.

BLENDING: Different viscosities of the same types of materials may be blended together to achieve intermediate viscosities. This term is also applied to resistive inks that can be blended with each other to achieve intermediate resistivities.

BLIND VIA: An interstitial via connecting a top conductive layer with one or more inner conductive layers.

BLISTER: Raised parts of a conductor or resistor formed by the outgassing of the binder or vehicle during the firing cycle.

BLOCK: To plug-up open mesh in a screen to prevent resistor or conductor pastes from being deposited in unwanted areas.

BLOCK DIAGRAM: A circuit diagram in which the essential units of the functional system are drawn in the form or blocks and the relationship between blocks is indicated by appropriate connecting lines.

BLOCK-OFF: See block.

BLOW HOLE: A surface anomaly formed by outgassing as solder solidifies.

BOAT: A container for materials to be vacuum-evaporated or fixed.

BOILING POINT: The temperature of a liquid at which its vapor pressure is equal to the pressure of the atmosphere surrounding the fluid.

BOMB: A chamber for applying various levels of positive or negative pressure on a package or component.

BOND: An interconnection which performs a permanent electrical and/or mechanical function.

BOND DEFORMATION: The change in the form of the lead produced by the bonding tool, causing plastic flow, in making the bond.

BOND ENVELOPE: The range of bonding parameters over which acceptable bonds may be formed.

BOND INTERFACE: The interface be-

tween the lead and the material to which it was bonded on the substrate.

BOND LIFT-OFF: The failure mode whereby the bonded lead separates from the surface to which it was bonded.

BOND-OFF: See bond lift-off.

BOND PAD: See bonding area.

BOND SCHEDULE: The values of the bonding machine parameters used when adjusting for bonding. For example, in ultrasonic bonding, the values of the bonding force, time, and ultrasonic power.

BOND SEPARATION: The distance between the attachment points of the first and second bonds of a wire bond.

BOND SHEAR STRENGTH: In hybrids, it is to be calculated as the limiting stress, measured as a true shear force (in grams or newtons) applied uniformly along the complete length of an item's side or contour, moving parallel to the bond interface and divide by the sheared-off bond surface area. Applicable to shearing a substrate from package bottom, or a die or device from a substrate surface.

BOND SITE: The portion of the bonding areas where the actual bonding took place (see bonding area).

BOND STRENGTH: In wire bonding, the pull force at rupture of the bond interface measured in the unit gram-force.

BOND-TO-BOND DISTANCE: The distance measured from the bonding site on the die to the bond impression on the post, substrate land, or fingers, which must be bridged by a bonding wire or ribbon.

BOND-TO-CHIP DISTANCE: In beam lead bonding the distance from the heel of the bond to the component.

BOND TOOL: The instrument used to position the lead(s) over the desired bonding area and impart sufficient energy to the lead(s) to form a bond.

BONDABILITY: Those surface characteristics and conditions of cleanliness of a bonding area which must exist in order to provide a capability for successfully bonding an interconnection material by one of several methods, such as ultrasonic, or thermosonic, or thermocompression wire bonding.

BONDING, DIE: Attaching the semiconductor chip to the substrate, either with epoxy, eutectic or solder alloy.

BONDING AREA: The area, defined by the extent of a metallization land or the top surface of the terminal, to which a lead is or is to be bonded.

BONDING ISLAND: Same as bonding pad.

BONDING PAD: A metallized area at the end of a thin metallic strip to which a connection is to be made.

BONDING WIRE: Fine gold or aluminum wire for making electrical connections in hybrid circuits between various bonding pads on the semiconductor device substrate and device terminals or substrate lands.

BOROSILICATE GLASS: A sealing glass providing a close coefficient of thermal expansion match between some metal leads, and ceramic, and metal, or glass packages.

BOW: A flatness deviation caused by a roughly cylindrical curvature of a board with the corners remaining in the same plane.

BRAZE: A joint formed by a brazing al-

loy. To join metals with a nonferrous filler metal at temperatures above 427°C.

BRAZING: Also called hard soldering. Similar to soldering, it is the joining of metals with a nonferrous filler metal at temperatures above 427°C.

BREAK LOAD: See bond strength.

BREAKAWAY: In screen printing the distance between the upper surface of the substrate and the lower surface of the screen when the screen is not deflected by the squeegee.

BREAKDOWN VOLTAGE: The voltage threshold beyond which there is a marked (almost infinite rate) increase in electrical current conduction.

BRIDGING: A defect condition, where the locallized separation between any two conductor lines (paths, traces) is reduced to less than the minimum allowable. In the extreme, it becomes a short. Bridging may be caused by misalignment, screening, solder splash, smears, or attached foreign material.

B-STAGED RESIN (B-STAGE): A partially cured resin which is used in the lamination process (see also prepreg).

BUGGING HEIGHT: The distance between the hybrid substrate and the lower surface of the beam lead device which occurs because of deformation of beam leads during beam lead bonding.

BULK CONDUCTANCE: Conductance between two points of a homogeneous material.

BURIED VIA: An interstitial via connecting inner conductive layers of a printed board, or multilayer substrate but not extending to either surface.

BURN-IN: The process of electrically stressing a device (usually in an elevated temperature environment) for an adequate period of time to cause failure of marginal devices.

BURN-IN (DEBUGGING): A reliability conditioning procedure which is a method of aging by operating the equipment under specified environmental test conditions in accordance with an established test conditioning specification. The purpose is to eliminate early failures and thus age or stabilize the operation of the equipment.

BURN-OFF: See flame-off.

BUS BAR: A conductor usually used to distribute high current from power supplies to backplanes; also conductors for distributing power on printed boards.

C

CAMBER: A term that describes the amount of overall warpage present in a substrate, camber = C/D where C = z- displacement, D = diagonal (longest distance) of the substrate surface. The out-of-plane deflection of a flat cable or flexible laminate of specified length.

CAPACITANCE DENSITY: Also referred to as sheet capacity. A term used to describe the amount of capacitance available per unit area (pF/mm^2 or $\mu F/cm^2$).

CAPACITIVE COUPLING: Electrical interaction between two conductors due to their shared capacitance.

CAPILLARY: A hollow bonding tool used to guide the bonding wire and to apply pressure to the wire during the bonding cycle.

CAPILLARY TOOL: A tool used in bonding where the wire is fed to the bonding surface of the tool through a bore located along the long axis of the

tool.

CASE: The bottom portion of a device package, usually a flat pack, it contains one or more cavities and all exit terminals (leads, pins). The case contributes to the hermetic and environmental protection of the (assembly of) electronic component parts within and, at the same time, determines the (hybrid) device's form factor.

CATALYST: Any substance which affects the rate of chemical reaction, but which itself may be recovered unchanged to the end of the reaction.

CAVITY: In microelectronic devices, the cavity is the sometimes recessed or hollowed-out area in the package bottom; the site of the device die or substrate circuitry when installed.

CENTERLINE AVERAGE (CLA): The atrithmetic average (AA) of measured deviations in a surface profile from an imaginary mean centerline located between the peaks and valleys. The *rms* reading for a given surface finish is about 11% higher than the AA reading.

CENTERWIRE BREAK: The failure mode in a wire pull test where the wire fractures at approximately mid-span.

CENTRIFUGE: Testing the integrity of bonds in a hybrid circuit by spinning the circuit at a high rate of speed, thereby imparting a high *g* loading on the interconnecting wire bonds and bonded elements.

CERAMIC: Inorganic nonmetallic material such as alumina, beryllia, aluminum nitride, steatite, or forsterite, whose final characteristics are produced by treatment at high temperatures (and sometimes also under applied pressure), often used in microelectronics as part of components, substrate, or package.

CERMET: A solid homogeneous material usually consisting of a finely divided admixture of a metal and ceramic in intimate contact.

CHARACTERISTIC IMPEDANCE: The voltage-to-current ratio of an electrical signal propagating through a transmission line.

CHASE: A voice-like tool or instrument with adjustable, flexible draw bars for prestretching wire-mesh cloth prior to installing it in a thick-film screen frame. The wire mesh that is to be gauged for prescribed tension.

CHEMICAL VAPOR DEPOSITION: Depositing circuit elements on a substrate by chemical reduction of a vapor on contact with the substrate.

CHESSMAN: The disk, knob, or lever used to manually control the position of the bonding tool with respect to the substrate.

CHIP: The uncased and normally leadless form of an electronic component part, either passive or active, disrete or integrated.

CHIP-AND-WIRE: A hybrid technology employing face-up-bonded chip devices exclusively, interconnected to the substrate conventionally; e.g., by flying wires.

CHIP CARRIER: A special type of enclosure or package to house a semiconductor device or a hybrid microcircuit and which has metallized castellations as usually electrical terminations around its perimeter, as well as solder-pads on its underside, rather than an ex-

tended lead frame or plug-in pins.

CHIP-IN-TAPE: See tape automated bonding (TAB).

CHIPOUT: A discontinual defect along the edge of a semiconductor or a ceramic substrate; damage caused by inadvertent mechanical impact, most often due to careless handling.

CHISEL: A specially shaped bonding tool in the shape of a chisel used for wedge bonding and ultrasonic bonding of aluminum or gold wires to elements or package leads.

CHLORINATED HYDROCARBON SOLVENTS: See Halogenated hydrocarbon solvents.

CHOPPED BOND: Those bonds with excessive deformation such that the strength of the bond is greatly reduced.

CHUCK: Portion of the bonding machine that holds the unit to be bonded.

CIRCUIT: The interconnection of a number of electrical elements and/or devices, performing the desired electrical functions. A circuit must contain one or more active elements (devices) in order to distinguish it from a network.

CIRCUMFERENTIAL SEPARATION: A crack formed around the circumference of a plated through hole or any other cylindrical interconnection made by plating or solder.

CLAD: A condition of one or both sides of the base material characterized by a thin layer of bonded metal foil.

CLAMPLNG FORCE: Force applied to a bonding tool to effect a bond.

CLEAN ROOM: A special manufacturing area where the air is filtered to remove dust particles and precautionary measures are used to keep contamination away from the unprotected circuit during processing.

CLINCH: A method of mechanically securing components prior to soldering, by bending that portion of the component lead that extends beyond the lip of the mounting hole, against a pad area.

CLINCHED LEAD: The formed portion of the component lead extending through a hole in a printed board which prevents the component from falling out during the solder process.

COATED METAL-CORE SUBSTRATE: A substrate consisting of a glossy, inorganic coating bonded to metal by firing at a temperature about 500°C.

COEFFICIENT: The ratio of change under specified conditions of temperature, length, etc.

COEFFICIENT OF THERMAL EXPANSION: The ratio of the change in dimensions to the change in temperature.

COEFFICIENT OF VISCOSITY: A measure of the tendency of a fluid to resist shear. The unit of viscosity is the poise.

CO-FIRING: Processing the thick-film conductors and resistors through the firing cycle at the same time.

COINED: A screen which contains the impression of a substrate because it has been subject to abuse is said to be coined. The term can also refer to a screen manufactured with a coined impression for the purpose of screening media in a special designed substrate with a cavity that standard screens cannot achieve. It is also used to describe the process by which the base of a package has been formed.

COINED LEAD: A cylindrical lead that

has been flattened to form a ribbon lead.

COINING: See coined.

COLD SOLDER CONNECTION: A soldered connection where the surfaces being bonded moved relative to one another while the solder was solidifying, causing an uneven solidification structure which may contain microcracks. Such cold joints are usually dull and grainy in appearance.

COLD SOLDER JOINT: A poorly wetted grayish-colored solder joint due to insufficient heating, solder contaminants, or inadequate presolder cleaning.

COLD-WELD: Forming a hermetic seal in a metal package by welding the lid to the frame using pressure alone.

COLLECTOR ELECTRODE: The metallized bonding pad making ohmic contact with the collector of a transistor element.

COMB PATTERN: A test pattern formed on a substrate in the shape of a comb.

COMPATIBLE MATERIALS: Materials that can be mixed or blended or brought into contact with each other with minimum reaction or separation taking place; or each material added will not degenerate the performance of the whole.

COMPENSATION CIRCUIT: A circuit which alters the functioning of another circuit to which applied with the goal of achieving a desired performance; temperature and frequency compensation are the most common.

COMPENSATION NETWORK: Same as compensation circuit devices in which a large number of elements are integral to each device.

COMPLEX ARRAY: An array of integrated devices in which a large number of elements are integral to each device.

COMPLIANT BOND. A bond which uses an elastically and/or plastically deformable member to impart the required energy to the lead. This member is usually a thin metal foil that is expendable in the process.

COMPLIANT MEMBER: The elastically and/or plastically deformable medium which is used to impart the required energy to the lead(s) when forming a compliant bond

COMPONENT: A diversely used term, which, dependent on context, may mean active or passive element, device, integrated or functional circuit, functional unit, or part of an operating system.

COMPONENT DENSITY: The number of components per unit area.

COMPOUND (CHEMICAL): A substance consisting of two or more elements chemically united in definite proportions by weight.

COMPRESSION SEAL: A seal made between an electronic package and its leads. The seal is formed as the heated metal, when cooled, shrinks around the glass insulator, thereby forming a tight joint.

CONDITIONING: Exposure of a test specimen to a specified environment(s) for a limited time prior to testing.

CONDUCTIVE ADHESIVE: An adhesive material that has metal powder added to increase electrical conductivity.

CONDUCTIVE EPOXY: An epoxy materlal (polymer resin) that has been

made conductive by the addition of a metal powder, usually gold or silver.

CONDUCTIVE FOIL: The conductive material covering one or both sides of the base material used to form the conductive pattern.

CONDUCTIVE PATTERN: The design or configuration formed in the conductive foil or layer. When applied to ceramic-bottom flat packages, a conductive pattern is one brought about by screened-on melallization, forming the internal portions of leads and other conductive areas.

CONDUCTIVE PROTECTIVE MATERIAL: In ESD control, a material, usually some form of plastic, is said to be conductive if its surface resistivity is less than 10^5 ohms/sq., and its volume resistivity is less than 10^3 ohm-cm.

CONDUCTIVITY: The ability of a material to conduct electricity, the reciprocal of resistivity.

CONDUCTOR: A class of materials that conduct electricity easily, i.e., have low resistivity ($\ll 10^{-4}$ Ω-cm). A single conductive path formed in the conductive foil or layer.

CONDUCTOR BASE SPACING: The spacing between conductors at the surface of the base material.

CONDUCTOR BASE WIDTH: The width of the conductors at the surface of the base materials.

CONDUCTOR LAYER: The entire conductive layer formed on one side of the base material.

CONDUCTOR SPACING: The distance between adjacent conductor film edges.

CONDUCTOR WIDTH: The width of individual conductors in a conductive film pattern.

CONFIDENCE INTERVAL: The maximum and minimum limits defining the range within which it is expected that an observation will occur in accordance with a degree of certainty as dictated by the confidence level.

CONFIDENCE LEVEL (ONE-TAIL): The degree of certainty, expressed as a percentage, that a given hypothesis is true within a specified limit and that the probability of its being outside this limit is proportional to the area of the tail of the probability distribution which exceeds the limit.

CONFIDENCE LEVEL (TWO-TAIL): The degree of certainty, expressed as a percentage, that a given hypothesis is true within a specified limit and that the probability of its being outside this limit is proportional to the area in the left and right tails of the probability distribution.

CONFIDENCE LIMITS: Boundaries which take sampling and other statistical fluctuations into consideration.

CONFORMAL COATING: A thin non-conductive coating, either plastic (e.g., poly-*p*-xylylene) or inorganic, applied to a circuit for environmental and/or mechanical protection.

CONTACT ANGLE: The angle made befween the bonding material and the bonding pad.

CONTACT AREA: The common area between two mating conductors permitting the flow of electric current.

CONTACT PRINTING: A method of screen printing where the screen is almost (within a few mils) in contact with the substrate. Used for printing

with metal mask.

CONTACT RESISTANCE: In electronic elements, such as capacitors or resistors, the apparent resistance between the terminating electrode and the body of the device. The electrical resistance between two mating conductors.

CONTACT SPACING: The centerline-to-centerline spacing of adjacent contact areas.

CONTINUITY: The uninterrupted path of current flow in an electrical circuit.

CONTINUOUS BELT FURNACE: A firing furnace that has a continuous belt carrying the unfired substrates through the firing cycle.

CONTROLLING COLLAPSE: Controlling the reduction in height of the solder balls in a flip-chip processing operation.

COORDINATOGRAPH: A drafting machine of great accuracy used in making original artwork for integrated circuits or hybrid microcircuits

COPLANAR LEADS (FLAT LEADS): Ribbon-type leads extending from the sides of the circuit package, all lying in the same plane.

COPLANARITY: Property of lying in the same plane.

COPOLYMER: A compound, resulting from the chemical reaction, polymerization, of two chemically different monomers with one another. The resulting larger molecules contain repeating structural units of the original molecules.

CORONA: The flow of small erratic current pulses resulting from discharges in voids in a dielectric during the voltage stress; also discharge resulting from ionisation of gas surrounding a conductor (frequently luminous) which occurs when the potential gradient exceeds a certain value but is not sufficient to cause sparking.

CORROSIVITY (CONDUCTOR TRACES): That characteristic of a conductor metallization on a substrate which causes a resistance change greater than 10 percent, and/or causes it to show visible evidence of corrosion with discoloration when in physical touch with an (epoxy) adhesive, and is concurrently exposed to moderate humidity and temperature effects, anytime after completed cure schedule.

COUPLING CAPACITOR: A capacitor that is used to block DC signals, and to pass high-frequency signals between parts of an electronic circuit.

COVER: The top portion of a package to be joined to the bottom portion to form a sealed unit. A cover has an internal depth (sometimes referred to as a cavity) distinguishing it from a lid which is flat

COVER LAYER: Outer layer of insulating material covering the conductive pattern on the printed board.

COVER SEAL: It denotes the seal at the perimeter of the cover or lid, when joined to the package body; or in hybrid fabrication, the cover-sealing operation itself. The seal may be accomplished by resistance welding, cold weld (solid-phase bond), brazing, soldering, or by other means.

CRACKING: Breaks in the metallic and/or nonmetallic layers extending through to an underlying surface.

CRATERING: Defect in which portion of the chip under ultrasonic bond is

torn loose by excessive amount of energy transmitted through the wire bond leaving a pit.

CRAZING: Fine cracks which may extend on or through layers of plastic or glass materials.

CREEP: The dimensional change with time of a material under load.

CRITICAL PRESSURE: The pressure under which a substrate may exist as a gas in equilibrium with liquid at the critical temperature.

CRITICAL TEMPERATURE: The temperature above which the gas cannot be liquefied by pressure alone.

CROSSOVER: The transverse crossing of metallization paths without mutual electrical contact and achieved by the deposition of an insulating layer between the conducting paths at the area of crossing.

CROSSTALK: Signals from one line leaking into another nearby conductor because of capacitance or inductive coupling or both (e.g., owing to the capacitance of a thick-fiim crossover).

CRYOGENICS: The science involving phenomena at very low temperatures less than -100°C.

CRYSTAL GROWTH: The formation of crystals in a material over a period of time and at an established temperature.

C-STAGED RESIN (C-STAGE): Completed cured resin.

CURE TIME: The total elapsed time between the addition of a catalyst and a complete hardening of a material; also the time for hardening of pre-mixed, frozen, or refrigerated epoxy adhesives.

CURIE TEMPERATURE (CURIE POINT): Critical temperature above which ferromagnetic materials lose their permanent spontaneous magnetization and ferroelectric materials lose their spontaneous polarization.

CURING AGENT: A material which when added to a second material activates a catalyst already present in the second material, thereby bringing about a chemical reaction, usually causing a hardening of the entire mass.

CURING CYCLE: For a thermosetting material, commonly a resin compound such as a bonding adhesive, it is the combination of total time-temperature profile to achieve the desired result; for example, the complete, irreversible hardening of the material resulting in a strong bond. The malerial is undergoing initial, intermediate, and final curing phases – the latter in a curing oven (furnace) – from the time of its removal from controlled storage at a specified temperature (when pre-mixed), or from the time of admixing a catalyst intended for activating a hardener additive to the time of achieving three-dimensional cross-linking (i.e., polymerization).

CURLS: Extruded material coming out from the edge of a bond.

CURRENT CARRYING CAPACITY: The maximum current which can be continuously carried by a circuit without causing objectable degradation of the electrical or mechanical properties.

CUSTOM CIRCUITS: Circuits designed to satisfy a single application requirement (hybrid or monolithic).

CUSTOM HYBRID: A hybrid integrated microcircuit device, designed by or for

a particular customer, and fabricated on a hybrid production line, dedicated at the time to satisfying the contract with that customer. The term is used as opposed to "standard hybrid", generally produced in volume.

CUT AND STRIP: A method of producing artwork using a two-ply laminated plastic sheet, by cutting and stripping off the unwanted portion of the opaque layer from the translucentlayer, leaving the desired artwork configuration.

CUTOFF: The operation following the final bonding step that separates the bond from the wire magazine.

CUTOFF SCISSORS: The scissors on a bonder to sever the wire after bonding.

CYCLIC STRESS: A completed circuit subjected to stress by cycling temperature and load over a period of time to cause premature failure.

D

DC VOLTAGE COEFFICIENT: The measure of changes in the primary characteristics of a circuit element as a function of the voltage stress applied.

DEFECT: A characteristic which does not conform to applicable specification requirements and adversely affects or potentially affects the quality of a device.

DEFINITION: The sharpness of a screen printed pattern – the exactness with which a pattern is printed.

DEGRADATION: Change for the worse in the characteristics of an electric element because of heat, high voltage, etc. A gradual deterioration in performance as a function of time.

DEIONIZED WATER: Water that has been purified by removal of ionizable materials.

DELAMINATION: A separation between the laminated layers of base material and/or base material and conductive foil.

DELTA [Δ] LIMIT: The maximum change in a specified parameter reading which will permit a hybrid microcircuit to be accepted on the specified test, based on a comparison of the final measurement with a specified previous measurement. (Note: when expressed as a percentage value, it shall be calculated as a proportion of the previous measured value).

DENDRITIC GROWTH: Growth of metallic filaments between conductors due to condenced moisture and electrical bias.

DENSITY: Weight per unit volume of a substance.

DERATING: The practice of subjecting parts or components to lesser electrical or mechanical stresses than they can withstand in order to increase the life expectance of the part or component.

DETRITUS: Loose material, dislodged during resistor trimming but remaining in the trim area.

DEVICE: A single discrete electronic element such as a transistor or resistor, or a number of elements integrated within one die, which cannot be further reduced or divided without eliminating its stated function. Preferred usage is die or dice, bare or prepackaged.

DEVITRIFICATION: The action or process of devitrifying or state of being devitrified—the conversion of a glassy matter into crysalline. Contamination, e.g., grease, will accelerate devitrifica-

tion.

DEVITRIFY: To deprive of glassy luster and transparency—to change from a vitreous to a crystalline condition.

DEWETTING: The condition in a soldered area in which liquid solder has not adhered intimately and has pulled back from the conductor area.

DEW POINT: The temperature at which liquid first condenses when a vapor is cooled.

DICE: The plural of die.

DICING: Total separation of diece from the wafer, usually by sawing.

DIE: An uncased discrete or integrated device obtained from a semiconductor wafer (see chip).

DIE ATTACH: The technique of mounting chips to a substrate. Methods include eutectic bonding, various solders, and conductive, and nonconductive epoxies.

DIE BOND: Attachment of a die or chip to the hybrid substrate (see die attach).

DIE-SHEAR STRENGTH: The effective die-shear strength is the measured true shear force (for example, in grams) applied parallel with the plane of the substrate with uniform distribution against the complete length of the bonded die's edge, via a linear motion of flat contact tool and sufficient to shear the die off its mounting, when divided by the area of the sheared-off surface. Choice of units: grams/mil^2; kg/inch^2; lb/inch^2 (psi); or newtons/inch^2

DIELECTRIC: (1) Any insulating medium which intervenes, between two conductors. (2) A material with the property that energy required to establish an electric field is recoverable in whole or in part as electric energy.

DIELECTRIC CONSTANT: The term used to describe a material's ability to store charge when used as a capacitor dielectric. The greek letter "ε" is to be used (not K). The property of a dielectric which determines the electrostatic energy stored per unit volume for unit potential gradient.

DIELECTRIC LAYER: A layer of dielectric material between two conductor plates.

DIELECTRIC LOSS: The power dissipated by a dielectric as the friction of its molecules opposes the molecular motion produced by an alternating electric field. The time rate at which electrical energy is transformed into heat in a dielectric when it is subjected to a changing electrical field.

DIELECTRIC PROPERTIES: The electrical properties of a material such as insulation resistance, breakdown voltage, etc.

DIELECTRIC STRENGTH: The maximum electric field that a dielectric will withstand without breaking down (physically). Expressed in volts per unit distance, such as centimeter (preferred) not inches.

DIFFUSION: The phenomenon of movement of matter at the atomic level from regions of high concentration to regions of low concentration. A thermal process by which minute amounts of impurities are deliberately impregnated and distributed into semiconductor material.

DIFFUSION BOND: See solid-phase bond.

DIFFUSION CONSTANT: The relative

rate at which diffusion takes place with respect to temperature.

DIGITAL CIRCUITS: Applied normally for switching applications where the output of the circuit normally assumes one or two states (binary operation); however, three-state operation is possible.

DIMENSIONAL STABILITY: A measurement of dimensional change of a material due to various environmental factors.

DIP SOLDERING: Soldering process for populated printed boards accomplished by dipping the exposed leads and conductive pattern in a bath of static molten solder.

DIRECT BOND COPPER: A process for eutectical attachment of copper foil to one or both sides of a ceramic substrate. This allows the substrate to handle power at substantially higher levels; it is used in power hybrid or power module assemblies.

DIRECT CONTACT: A contact made to the semiconductor die when the wire is bonded directly over the part to be electrically connected, as opposed to the expanded contact.

DIRECT EMULSION: Emulsion applied to a screen in a liquid form as contrasted to an emulsion that is transferred from a backing film of plastic.

DIRECT EMULSION SCREEN: A screen whose emulsion is applied by painting directly onto the screen, as opposed to indirect emulsion type.

DIRECT METAL MASK: A metal mask made by etching a pattern into a sheet of metal.

DISCRETE: As applied to components used in thin-film and thick-film hybrid circuits; the elements that are added separately are discrete elements (or devices), as opposed to those that are made by screen printing or other deposition methods as parts of the film network.

DISCRETE COMPONENTS: Individual components or elements such as resistors, capacitors, transistors, diodes, inductors, and others as self-contained entities.

DISSIPATION FACTOR (ALSO LOSS TANGENT): It is the measure of the deviation of a material from an ideal dielectric. It is the ratio of the reactance (X_p) to the resistance (R_p) in an equivalent parallel circuit.

DISTRIBUTION, PROBABILITY: A distribution which describes the probability of occurence of the chance or event under consideration.

DOPING: The addition of an ionic impurity to a semiconductor to alter its conductivity in desired well-defined areas and to a specified depth.

DOUBLE-SIDED SUBSTRATE: As the name implies, a substrate carrying active circuitry on both its topside and bottomside, electrically connected by means of metallized through-holes or edge metallization or both.

DRIFT: Permanent change in value of a device parameter over a period of time because of the effects of temperature, aging, humidity, etc.

DROSS: Oxide and other contaminants found on the surface of molten solder.

DRY AIR: Air that has been circulated through a drying process to remove water molecules.

DRY INERT ATMOSPHERE: An inert

gas such as nitrogen that has been circulated through a drying process to remove water molecules.

DRY PACK: Also known as waffle pack, it is a flat container for the storage of sorted dice or chips in a grid of individual compartments or cavities. The drypack and its closely fitting cover or lid usually are made of antistatic plastic material.

DRY PRESSING: Pressing and compacting of dry powdered materials with additives together in rigid die molds under heat and pressure to form a solid mass, usually followed by sintering as for alumina substrates.

DRY PRINT: The screened resistor and conductors that have gone through the drying cycle removing the solvents from the ink.

DRYER: A drying tube containing silica gel or a similar moisture absorbent chemical.

DUAL-IN-LINE PACKAGE (DIP): A package having two rows of leads extending at right angles from the base and having standard spacings between leads and between rows of leads.

DUCTILITY: That property which permits a material to deform plastically without fracture. Prpoperty that allows the material to absorb large overloads.

DYE PENETRANT: A dye, usually red, used in a carrier fluid to find the location of a rather gross leak in a package when injected first, then how and where the dye colors a white coating sprayed onto the package is observed.

DYNAMIC PRINTING FORCE: The fluid lorce which causes a pseudo plastic paste to flow through a screen mesh and wet the surface beneath. Its absolute value is a complex function of all screen printer operating parameters together with the rheological properties of the fluid being printed.

DYNAMIC TESTING: Testing a hybrid circuit where reactions to AC (especially high frequency) are evaluated.

E

EDGE DEFINITION: The reproduced pattern edge fidelity compared to the production master.

EDGE METALLIZATION: The metallization applied to the edge of a substrate, wraparound fashion, such that it established an electrical connection between circuitry installed on two opposite surfaces of the substrate.

ELASTIC MODULUS: A constant of proportionality which is indicative of the stiffness or rigidity of the material.

ELECTRIC FIELD: A region where there is a voltage potential, the potential level changing with distance. The strength of the field is expressed in volts per unit distance.

ELECTRICAL ISOLATION: Two conductors isolated from each other electrically by an insulating layer.

ELECTRICAL PROPERTIES: The properties of a device or material that effect its conductivity or resistivity to the flow of an electric current.

ELECTRICALLY CONDUCTIVE EPOXY: An organic polymer epoxy adhesive having metallic particles such as gold, silver, palladium, etc. included as fillers in its formulation.

ELECTRICALLY HOT CASE: A hybrid circuit package that is used as part of the grounding circuit.

ELECTRODES: The conductor or con-

ductor lands of a hybrid circuit. Also the metallic portions of a capacitor structure.

ELECTROLESS PLATING: Deposit of a metallic material on a surface by chemical deposition as opposed to the use of an electric current.

ELECTRON BEAM BONDING: Bonding two conductors by means of heating with a stream of electrons in a vacuum.

ELECTRON-BEAM PATTERNING: E-beam, or EB, patterning of resist produces the required thin lines (as in VLSI) by evaporation from the heat supplied by the energy of a narrowly focused electron beam.

ELECTRONIC PACKAGING: The technical discipline of designing a protective enclosure for an electronic circuit so that it will both survive and perform under a plurality of environmental conditions.

ELECTROPLATING: Deposition of an adherent metallic coating onto a conductive object placed into an electrolytic bath composed of a solution of the salt of the metal to be plated. Using the immersed object as the cathode and the other terminal as the anode (possibly of the same metal as the one used for plating), a DC current is passed through the solution affecting transfer of metals ions onto the cathodic surface.

ELECTROSTATIC DISCHARGE: ESD is the instantaneous transfer of charges accumulated on a nonconductor, along a conductor into ground; caused either by direct contact or induced by an electrostatic field. If an ESDS (an ESD-Sensitive item such as a MOS die) happens to be in the discharge path, it may suffer obvious destruction or latent damage, even if the ESD event was too weak to be felt.

ELEMENT: A constituent unit which contributes to the operation of a hybrid microcircuit. Integral elements include deposited or screened passive circuit elements, metallization paths, and deposited or formed insulation. Discrete or integrated electronic parts including dice, chips, and other microcomponents; also mechanical piece parts as cases, covers, and certain wires, all contibuting to the operation of a hybrid microcircuit.

ELONGATION: The ratio of the increase in wire length at rupture, in a tensile test, to the initial length, given in percent.

EMBEDDED: Enclosed in plastic material.

EMITTER ELECTRODE: The mettalic pad making ohmic contact to the emitter area of a transistor element.

EMULSION: The light-sensitive material used to coat the mesh of a screen.

ENCAPSULATION: The process of completely enclosing an article in an envelope of dielectric material.

ENTRAPPED MATERIAL: Gas or particles (inclusions) bound up in a solid or in an electrical package.

ENVIRONMENT: The physical conditions, including climate, mechanical, and electrical conditions, to which a product may be exposed during manufacture, storage, or operation.

ENVIRONMENTAL TEST: A test or series of tests used to determine the sum of external influences affecting the

structural, mechanical, and functional integrity of any given package or assembly.

EPOXY ADHESIVE: An organic polymer compound consisting of a thermosetting resin, a filler, a binder, a hardening agent, with a catalyst added, together with minor additives. The resin is one in which an oxigen atom is joined to each of the two other connected atoms. Epoxy is commonly used in paste form for bonding in hybrid assembly; it subsequently undergoes a curing cycle (polymerization) for hardening.

ETCHBACK: Process for removing controlled amounts of dielectric material from hole sidewalls.

ETCHED METAL MASK: A metal mask used for screening where-in the pattern is created in a sheet of metal by the etching process.

ETCH FACTOR: Ratio of etch depth to lateral etch in a conductor pattern.

ETCHING: The chemical, or chemical and electrolytic, removal of selected conductive material to form a conductive pattern.

EUTECTIC: (1) A term appleid to the mixture of two or more substances which has the lowest melting point. (2) An alloy or solution having its components in such proportion that the melting point is lowest possible with those components.

EUTECTIC ALLOY: An alloy having the same temperature for melting and solidus.

EUTECTIC DIE ATTACH: A technique in microelectronic assembly where a preform of eutectic alloy (AuGe, AuSi, SnPb, etc.) is placed between a surface spot such as a substrate land and the part of element to be bonded (a device die, usually with gold backing, for example), to subsequently be brought to the eutectic melting temperature, yielding a strong, permanent bond upon cooling.

EXPANDED CONTACT: A contact made to the semiconductor die where the sire bonded to an area remote from the part to be electrically connected so that a lateral interconnection path for the current is required.

EXPONENTIAL (WEAROUT) FAILURES: Failures that occur at an exponentially increasing rate.

EXTERNAL LEADS: Electronic package conductors for input and output signals, power, and ground. Leads can be either flat ribbons or round wires.

EYELET TOOL: A bonding tool with a square protuberance beneath the bonding tool surface which presses into the conductor and prevents the slippage between wire or conductor and tool interface. Used primarily for ribbon wire bonding.

F

FACE BONDING: The opposite of back bonding. A face bonded semiconductor chip is one that has its circuitry side facing the substrate. Flip-chip and beam lead bonding are the two common face bonding methods.

FAILURE: Inability of a product to meet its performance specifications.

FAILURE ANALYSIS: The analysis of a circuit to locate the reason for the failure of the circuit to perform to the specified level.

FAILURE MECHANISM: Ther physical or chemical process by which a device proceeds to the point of failure.

FAILURE MODE: The cause for rejection of any failed device as defined in terms of the specific electrical or physical requirement that it failed to meet.

FAILURE RATE: The rate at which devices from a given population can be expected (or were found) to fail as a function of time (e.g., %/1000 hr of operation).

FARADAY CAGE SHIELDING BAG: Embodied in the static-shielding bag, it is a conductive semitransparent, flexible, high strength, heat sealable container which, being an equipotential surface, prevents external electrical fields (created by any charged object or person) from causing induced charge potential differences inside. (The bag is to limit capacitive coupling of the external charge through its contents. Another form of construction for such a bag is the conductive grid bag.) Constructed, is one realization, as an outer polyester material bearing a thin metallic film with a transparent, abrasion-resistant overcoating, laminated to an inner layer of anti-static polyethylene film. The latter's function is to prevent triboelectric static charge generation by items inside the bag.

FATIGUE: Used to describe a failure of any structure caused by repeated application of stress over a period of time.

FATIGUE FACTOR: The factor causing the failure of a device under repeated stress.

FEATHERS: See curles.

FEEDTHROUGH: A conductor through the thickness of a substrate, thereby electrically connecting both surfaces.

FERRITE: A powdered, compressed, and sintered magnetic material having high resistivity; cores made of sintered powers are used for ferromagnetic applications.

FERROELECTRIC: A crystalline dielectric that exhibits dielectric hysteresis—an electrostatic analogy to ferromagnetic material.

FERROMAGNETIC: A material that has a relative permeability noticeably exceeding unity and generally exhibits hysteresis.

FIELD TRIMMING: Trimming of a resistor to set an output voltage, current, etc.

FILLER: A substance, usually dry and powdery or granular, used to thicken fluids or polymers.

FILLET: A concave junction formed where two surfaces meet.

FILM: Single or multiple layers or coating of thin-film or thick material used to form various elements (resistors, capacitors, inductors) or interconnections and crossovers (conductors, insulators). Thin-films are deposited by vacuum evaporation or sputtering and/or plating. Thick-films are deposited by screen printing.

FILM CONDUCTOR: A conductor formed in situ on a substrate by depositing a conductive material by screening, plating, or evaporation techniques.

FILM NETWORK: An electrical network composed of thin-film and/or thick-film components and interconnections deposited on a substrate.

FINAL SEAL: The manufacturing operation that completes the enclosure of

the hybrid microcircuits so that further internal processing cannot be performed without delidding the package.

FINE LEAK: A leak in a sealed package less tham $10^{-5}cm^3$/sec at 1 atmosphere of differential air pressure.

FIRE: When reffered to a thick-film pattern, it denotes the act of high-temperature heating in a furnace so that resistors, conductors, insulators, capacitors, etc. be transformed into their final form, generally fused.

FIRING SENSITIVITY: Refers to the percentage change caused in the fired film characteristics due to a change in peak firing temperature. The firing sensitivity is expressed in units of %/°C.

FIRST ARTICLE: A preproduction assembly used to ensure that the manufacturing process will be capable of producing acceptable product.

FIRST BOND: The first bond in a sequence of two or more bonds made to form a conductive connection.

FIRST RADIUS: The radius of the front edge of a bonding tool foot.

FIRST SEARCH: That period of machine cycle at which final adjustment in the location of the first bonding area (see first bond) under the tool are made prior to lowering the tool to make the first bond.

FISSURING: The cracking of dielectric or conductors. Often dielectrics, if incorrectly processed, will crack in the presence of conductors because of stresses occuring during firing.

FLAG: Support area on lead frame for die.

FLAME-OFF: The procedure in which the wire is severed by passing a flame across the wire, thereby melting it. The procedure is used in gold wire thermocompression bonding to form a ball for making a ball bond.

FLATNESS: The deviation from a perfect plane normally expressed in decimals or fractions of an inch per inch, but sometimes in T.I.R. Flatness of a package is measured by putting it in a three-point suspension on the plane from which the deviation is to be measured.

FLATPACK: An integrated circuit, or hybrid circuit package having its leads extended from the sides and parallel to the base or are bent as specified.

FLEXIBLE COATING: A plastic coating that is still flexible after curing.

FLEXIBLE PRINTED CIRCUIT: Patterned printed components and board utilizing flexible base material.

FLEXIBLE PRINTED WIRING: Patterned printed board utilizing flexible base material.

FLEXURAL STRENGTH: Strength of the laminate when it is measured by bending.

FLIP-CHIP: A leadless monolithic structure, containing circuit elements, which is designed to electrically and mechanically interconnect to the hybrid circuit by means of an appropriate number of bumps located on its face which is covered with a conductive bonding agent.

FLIP-CHIP MOUNTING: A method of mounting flip chips on thick-film or thin-film circuits without the need for subsequent wire bonding.

FLOATING GROUND: An electrical ground circuit that does not allow con-

nection between the power and signal ground for the same circuit.

FLOOD BAR: A bar or other device on a screen printing device that will drag paste back to the starting point after the squeegee has made a printing stroke. The flood stroke returns the paste without pushing it through the meshes, so it does no printing, only returns the past supply to be ready for the next print.

FLUX: In soldering, a material that chemically attacks surface oxides and tarnishes so that molten solder can wet the surface to be solderd.

FLUX RESIDUE: Particles of flux remaining on a circuit after soldering and cleaning operations.

FOAM (ANTI-STATIC): A static-free cushioning material, usually made from some virgin or blended, closed-cellular expanded polymer, impregnated with an internal, anti-static, or electrically-conductive agent. In packaging microcircuits, it provides protection against ESD and mechanical shock during handling, transport, shipping, and storage as well as shunt protection for leads.

FOIL BURR: A rough edge on the foil material after same type of machining operation.

FOOT LENGTH: The long dimension of the boncing surface of a wedge-type bonding tool.

FOOTPRINT: The area needed on a substrate for a component or element. Usually refers to specific geometric pattern of a chip.

FORMING GAS: A gas (N_2, with traces of H_2 and He) used to blanket a part being processed to prevent oxidation of the metal areas.

FRIT: Glass composition ground up into a powder form and used in thick-film compositions as the portion of the composition that melts upon firing to give adhesion to the substrate and hold the composition together.

FULLY ADDITIVE PROCESS: Deposition of the entire conductive pattern thickness by electrtoless metal plating.

FUNCTIONAL TRIMMING: Trimming of a circuit element (usually resistors) on an operating circuit to set a voltage or current on the output.

FURNACE ACTIVE ZONE: The thermostatically controlled portion of a multizoned muffle furnace.

FURNACE PROFILE: A set of material dependednt temperature and belt-speed furnace parameters used to process thick-film hybrid microcircuits.

FURNACE SLAVE ZONE: That portion of a multizoned muffle furnace where the instantaneous power supplied to the heating element is a set percentage of the power supplied to the active zone. Hence temperature control in the slave zone is not accomplished by sensing thermocouples as in the case of the active zone.

FUSED COATING: A metallic coating that has been melted and solidified on the base metal (usually solder or tin).

FUSING: Melting and cooling two or more powder materials together so that they bond together in a homogeneous mass.

G

GANG BONDING: The act of bonding a plurality of mechanical and/or electrical connections through a single act or stroke of a bonding tool.

GAS BLANKET: An atmoshphere or in-

ert gas, nitrogen, or forming gas flowing over a heated integrated circuit chip or a substrate that keeps the metallization from oxiding during bonding.

GATE CHAIN: Large numbers of FETs connected in parallel, with common source, common drain, common gate and substrate. Gate chain is used in VSLI technology as a test structure, placed in the "street" (kerf) areas separating dice on a wafer, for probing; mostly for determining the levels of defects as a way of process monitoring and characterization. Benefits hybrids, using VLSI devices.

GEL TIME: The time (in seconds) required for prepreg resin to melt and solidify when heated.

GLASS BINDER: The glass powder added to a resistor or conductor ink to bind the metallic particles together after firing.

GLASSIVATION: An inert, transparent, glass-like thin layer of pyrolytic insulation material that covers (pasivates) the active device areas, including operating metallization on the wafer, but excluding bonding pads, bumps, and beam leads.

GLASS PHASE: The part of the firing cycle wherein the glass binder is in a molten phase.

GLASS TRANSITION TEMPERATURE (Tg): In polymer chemistry, the temperature below which the thermal expansion coefficient becomes nearly constant or a simple function of temperature. The temperature at which amorphous polymers change from a hard and brittle state to a soft rubbery state. Most of the material properties change rapidly and significantly at this temperature.

GLAZE: See overglaze.

GLAZED SUBSTRATE: A glass coating on a ceramic substrate to effect a smooth and nonporous surface.

GLOB-TOP: A glob of encapsulant material surrounding a die in the COB (chip-on-board) assembly process. Note: the attached dice must have been pretested/inspected/passed, as rework after final curing of the epoxy or silicone globs is virtually impossible.

GLOSSY: A shiny surface usually formed by the glass matrix in a conductor or resistor ink.

GRAIN GROWTH: The increase in the size of the crystal grains in a glass coating or other material over a period of time.

GRAM-FORCE: A unit of force (nominally 9.8 mN) required to support a mass of 1 gram (1 gravity unit of acceleration time one gram of mass equals 1 gram-force). Colloquially, the term gram is used for the unit.

GREEN: A term used in ceramic technology meaning unfired. For example, a "green" substrate is one that has been formed, but has not been fired.

GROSS LEAK: A leak in a sealed package greater than 10^{-5} cm^3/sec at 1 atmosphere of differential air pressure.

GROUND: A conducting connection to earth or to some other large conducting object. Its purpose is to maintain an earth potential on the conductors connected to it, and, to conduct the ground current to and from the earth.

GROUND PLANE: A conductive layer on a substrate or buried within a substrate that connects a number of points

to one or more grounding electrodes. The conductor layer used as a common electrical circuit return, shielding and spreading heat.

GROUND PLANE CLEARANCE: The etched portion of the conductive material that provides clearance around a plated through hole.

H

HALO EFFECT: A glass, or epoxy, or any other semiclear material that diffracts light, halo around certain conductors. Generally, this is an undesirable effect to be avoided by changing the furnace profiles or material types.

HOLOGENATED HYDROCARBON SOLVENTS: Organic solvents containing the elements chlorine or fluorine used in cleaning substrates and completed circuits (e. g., trichloreothylene, various freons).

HALOING: Fracturing or delaminating of the base material usually below the surface due to a mechanical operation.

HAND SOLDERING: Forming a soldered connection with solder using a hand-held soldering iron for application of the heat.

HARD GLASS: Predominantly a borosilicate glass of high viscosity at elevated temperatures, having a TCE (temperature coefficient of expansion) very close to that of "Kovar". In packages it is used for matched seals.

HARD SOLDER: Solder that has a melting point above 425°C.

HARDNESS: A property of solids, plastics, and viscous liquids that is indicated by their solidity and firmness; resistance of a material to indentation by an indentor of fixed shape and size under a static load or to scratching; ability of a metal to cause rebound of a small standard object dropped from a fixed height; the cohesion of the particles on the surface of a mineral as determined by its capacity to scratch another or be itself scratched. Resistance of material to plastic deformation, usually by indentation. The term may also refer to stiffness, or temper, or resistance to scratching, abrasion, or cutting. Indentation hardness may be measured by various hardness tests, such as Brinell, Rockwell, and Vickers.

HAYWIRE: A program-peculiar term, referring to a special insulated magnet wire, used primarily for repairs of hybrid circuits and modules as a jumper to component leads or header pins.

HEADER: The base of a package for a (hybrid) microcircuit or a discrete semiconductor device. The bottom portion of a device package which holds the leads or pins. Also referred to as case.

HEAT CLEAN: The process of removing all organic material from glass cloth at approximately 343°C to 371°C for a period of time ranging up to 50 hours.

HEAT COLUMN: The heating element in a eutectic die bonder or wire bonder used to bring the substrate up to the bonding temperature.

HEAT FLUX: The outward flow of heat from a heat source.

HEAT SINK: The supporting member to which electronic components or their substrate or their package bottom are attached. This is usually a heat conductive metal with the ability to rapidly transmit heat from the generating source (component).

HEAT SOAK: Heating a circuit over a

period of time to allow all parts of the package and circuit to stabilize at the same temperature.

HEEL (OF THE BOND): The part of the lead adjacent to the bond that has been deformed by the edge of the bonding tool used in making the bond. The back edge of the bond.

HEEL BREAK: The rupture of the lead at the heel of the bond.

HEEL CRACK: A crack across the width of the bond in the heel region.

HELLUM LEAK CHECK: A check on the leak rate of a hermetically sealed device or package where the tracer gas employed is helium. The ionized gas outflow is analyzed instrumentally and the leak rate is expressed in units of atm-cm^3/sec.

HELIUM MASS SPECTROMETER: An instrument of interest to the hybrid technologist as part of widely used leak detector systems. The mass spectrometer generally consists of means to ionize the helium in a vacuum, to accelerate and focus the ions by application of a fixed voltage, and then to separate the helium ions from other gas or vapor constituents, sorting them by magnetic deflection according to their atomic mass number or molecular weight. The helium atoms, after passing through a slit, are collected and cause a voltage to build up on the grid of a spectrometer tube; the resulting current, then, actuates the leak-rate detector. In practice, the leak-rate meter will deflect depending on the concentration of helium available from the jet probe held against an evacuated device under test exhibiting a fine leak and being connected to a vacuum system.

HERMETIC: A description of packages that provide an absolute seal against the infusion of water to prevent degradation of the electrical components within the package. The test for hermeticity is to observe leak rates when placed in a vacuum. A plastic encapsulation cannot be hermetic by definition because there is no internal volume of gas to escape.

HERMETICITY: The ability of a package to prevent exchange of its internal gas with the external atmosphere. The figure of merit is the gaseous leak rate of the package measured in atm-cm^3/sec.

HIGH-*K* CERAMIC: A ceramic dielectric composition (usually $BaTiO_3$) which exhibits large dielectric constants, and nonlinear voltage and temperature response.

HIGH-PURITY ALUMINA: Alumina having over 99% purity of Al_2O_3.

HIGH-RELIABILITY SOLDERING: A statistically proven soldering technique that ensures a large probability of metallic joining success.

HOLE DIAMETER: Normally refers to the diameter of the hole through the bonding tool.

HOMOGENEOUS: Alike or uniform in composition. A thick-film composition that has settled out is not homogeneous, but after proper stirring it is. The opposite of heterogeneous.

HORN: Cone-shaped member which transmits ultrasonic energy from transducer to bonding tool.

HOSTILE ENVIRONMENT: An environment that has a degrading effect on an electronic circuit.

HOT SPOT: A small area on a circuit

that is unable to dissipate the generated heat and therefore operates at an elevated temperature above the surrounding area.

HOT ZONE: The part of a continuous furnace or kiln that is held at maximum temperature. Other zones are the preheat zone and cooling zone.

HYBRID CIRCUIT: A microcircuit consisting of elements which are a combination of the film circuit type and the semiconductor circuit type, or a combination of one or both of these types and may include discrete add-on components.

HYBRID DEVICE: Same as hybrid microcircuit. In this context, it encompasses categories like microwave hybrids (MIC and SLC), power hybrids, flexible hybrids (for example, on a "Kapton" substrate), firberoptic hybrids, and surface acoustic wave (SAW) devices beyond the traditional hybrids of thick-film or thin-film construction on rigid substrates.

HYBRID GROUP (ELECTRICALLY AND STRUCTURALLY SIMILAR CIRCUITS): Hybrid microcircuits which are designed to perform the same type(s) of basic circuit function(s), for the same supply, bias, and single voltages and for input-output compatibility with each other under an established set of loading rules, and which are enclosed in packages of the same construction and outline.

HYBRID INTEGRATED CIRCUIT: A microcircuit including thick-film or thin-film paths and circuit elements on a supporting substrate, to which active and passive microdevices are attached, either prepackaged or in un-cased form as chips, usually all enclosed in a suitable package (hermetic or epoxy type). Used interchangeably with hybrid circuit and hybrid microcircuil.

HYBRID MICROCIRCIIIT: A microcircuit that involves an insulating substrate on which are deposited networks, consisting generally of conductors, resistors, and capacitors, and to which are attached discrete semiconductor devices and/or monolithic integrated circuits and/or passive elemenls to form a packaged assembly. Used interchangeably with hybrid circuit and hybrid integrated circuit.

HYBRID MICROELECTRONICS: The entire body of electronic art which is connected with or applied to the realization of electronic svstems using hvbrid circuit technoloqy.

HYBRID MICROWAVE CIRCUIT: See microwave integrated circuit.

HYBRID MODULE: A special carrier of hybrid microcircuits and other components interconnected as a unit, as a component of an electronic subsystem. The module may be of single construction or made up of submodules, each usually with a compartment to house hermetically packaged hybrids and discrete passive component parts such as transtormers, axial-lead resistors, etc. Nonhermetic hybrid modules may be parylene-coated. NOTE: Microwave-hybrid modules have various specific configurations: coaxial, slotted, round, circular, oblong, etc.

I

IMBEDDED LAYER: A conductor layer having been deposited between insulating layers.

INACTIVE FLUX: Flux that becomes

nonconductive after being subjected to the soldering temperature.

INACTIVE METALLIZATION: Conductive metallized traces, paths, pads, fingers, or other areas on an active or passive substrate; metallized elements of a deposited pattern which are not being utilized at the time in the functioning circuit.

INCLINED PLANE FURNACE: A resistor firing furnace having the hearth inclined so that a draft of oxidizing atmosphere will flow through the heated zones through natural convection means.

INCOMPLETE BOND: A bond impression having dimensions less than normal size due to a portion of the bond impression being missing.

INDIRECT EMULSION: Screen emulsion that is transferred to the screen surface from a plastic carrier or backing material.

INDIRECT EMULSION SCREEN: A screen whose emulsion is a separate sheet or film of material, attached by pressing into the mesh of the screen (as opposed to the direct emulsion type).

INERT ATMOSPHERE: A gas atmosphere such as helium or nitrogen that is nonoxidizing or nonreducing of metals.

INFANT MORTALITY (EARLY FAILURES): The time regime during which hundreds of circuits may be failing at a decreasing rate (usually during the first few hundred hours of operafion).

INFRARED: The band of electromagnetic wavelengths lying between the extreme of the visible (= 0.75 μm) and the shortest microwaves (= 1000 μm). Warm bodies emit the radiation and bodies which absorb the radiation are warmed.

INJECTION MOLDED: Molding of electronic packages by injecting liquefied plastic into a mold.

INK: Synonymous with "composition" and "paste" when relating to screenable thick-film materials, usually consisting of glass frit, metals, metal oxide, and solvents.

INK BLENDING: See blending.

IN-PROCESS: Some step in the manufacturing operation prior to final testing.

INSERTION LOSS: The difference between the power received at the load before and after the insertion of apparatus at some point in the line.

INSPECTION LOT: A quantity of hybrid microcircuits, representing a production lot, submitted for inspection at one time to determine compliance with the requirements and acceptance criteria of the applicable procurement doc- ument. Each inspection sublot of hybrid microcircuits should be a group of circuits identified as having common manufacturing experience through all significant manufacturing operations.

INSULATED-METAL SUBSTRATE: A substrate, such as one made of porcelainized steel, which is not sublect to size limitations and may have superior thermal dissipation characteristics.

INSULATING LAYER: Used interchangeably with dielectric layers in hybrids, it is a thick-film or thin-film deposited layer of material separating or covering conductive layers.

INSULATION RESISTANCE (IR): The resistance to current flow when a poten-

tial is applied. IR is measured in megohms.

INSULATORS: A class of materials with high resistivity. Materials that do not conduct electricity. Materials with resistivity values of over 10^5 Ω-cm are generally classified as insulators.

INTEGRATED CIRCUIT: A microcircuit (monolithic) consisting of interconnected elements inseparable associated and formed in situ on or within a single substrate (usually silicon) to perform an electronic circuit function.

INTERCONNECTION: The conductive path required to achieve connection from a circuit element to the rest of the circuit.

INTERFACE: The boundary between dissimilar materials, such as between a film and substrate or between two films.

INTERFACIAL BOND: An electrical connection between the conductors on the two faces of a substrate.

INTERLAYER CONNECTION: A via interconnecting multiple conductive layers in a multilayer printed board.

INTERMETALLIC BOND: The ohmic contact made when two metal conductors are welded or fused together.

INTERMETALLIC COMPOUND: A compound of two or more metals that has a characteristic crystal structure that may have a definite composition corresponding to a solid solution, often refractory.

INTERNAL LAYER: A conductive layer internal to a multilayer printed substrate or board.

INTERNAL HEIGHT (FOR PACKAGE): The clearance between a package bottom's inside surface (i.e., the floor, bearing the installed substrate) and the cover cavity's inside surface. The height determining the volumetric match between an uncased hybrid microcircuit and its package after sealing.

INTERNAL VISUAL: See preseal visual.

INTRACONNECTIONS: Those connections of conductors made within a circuit on the same substrate.

IONIC CONTAMINANT: Any contaminant that exists as ions and, when dissolved in solution, increases electrical conductivity.

ION IMPLANTATION: Introducing the required dopants into a semiconductor crystalline material by accelerating charged atoms (ions) in an electric field and firing them into predetermined locations in the material. Ion implantation is more precise than doping by diffusion.

ION MIGRATION: The movement of free ions within a material or across the boundary between two materials under the influence of an applied electric field.

IONIZABLE MATERIAL: Material that has electrons easily detracted from atoms or molecules, thus originating ions and free electrons that will reduce the electrical resistance of the material.

J

JUMPER. A direct electrical connection between two points on a film circuit. Jumpers are usually portions of bare or insulated wire mounted on the component side of the substrate.

JUNCTION. (1) In solid state materials, a region of transition between *p*- and *n*-type semiconductor material as in a transistor or diode. (2) A contact be-

tween two dissimilar metals or materials (e.g., in a thermocouple or rectifier). (3) A connection between two or more conductors or two or more sections of a transmission line.

JUNCTION TEMPERATURE: The temperature of the region of transition between the *p*- and *n*-type semiconductor material in a transistor or diode element.

K

K FACTOR: This term refers to thermal conductivity, the ability of a substance to conduct heat through its mass.

KERF: The slit of channel cut in a resistor during trimming by laser beam or abrasive jet.

KEY: A device that ensures only one possible connection of two items.

KEYING: The use of features or additional devices in a design to ensure that there is only one possible mating method.

KILN: A high-temperature furnace used in firing ceramics.

KIRKENDALL VOIDS: The formation of voids by diffusion across the interface between two dissimilar materials, in the material having the greater diffusion rate into the other.

KOVAR: An alloy conforming to the ASTM designation F15. It contains nominally 17 percent cobalt, 53 percent iron, and 29 percent nickel, plus trace elements. Its usefulness for hybrids is based on the fact that its average linear coefficient of thermal expansion (TCE) matches closely that of glasses used in hermetic seals. Kovar is available in wire, rod, bar, strip, sheet, ring, and tubing

L

L-CUT: A trim notch in a film resistor that is created by the cut starting perpendicular to the resistor length and turning 90° to complete the trim parallel to the resistor axis thereby creating an L-shaped cut.

LADDER NETWORK: A series of film resistors with values from the highest to the lowest resistor reduced in known ratios.

LAMINAR FLOW: A constant and directional flow of filtered air across a clean workbench. The flow is usually parallel to the surface of the bench.

LAMINATE: A layered sandwich of sheets of substances bonded together under heat and pressure to form a single structure.

LAMINATE VOID: The absence of resin in a specific location in the laminate.

LAND: Widened conductor areas on the major substrate used as attachment points for wire bonds or the bonding of chip devices.

LAND PATTERN (FOOTPRINT): A specific conductive pattern for electrically connecting a particular component.

LAPPING: Smoothing a substrate surface by moving it over a flat plate having a liquid abrasive.

LASER BONDING: Effecting a metal-to-metal bond of two conductors by welding the two materials together using a laser beam for a heat source.

LASER TRIMMING: Adjustable automated trimming of thick-film or thin-film resistor elements on a patterned substrate, using computerized laser equipment in production.

LATTICE STRUCTURE: A stable arrangement of atoms and their electron-pair bonds in a crystal.

LAYER: One of several films in a mul-

tiple film structure on a substrate.

LAYOUT: The positioning of the conductors and/or resistors on artwork prior to photoreduction of the layout to obtain a working negative or positive used in screen preparation.

LCC: Leadless chip carrier.

LEACHING: Removing portions of material by dissolving its soluble constituents into another (solid) material. In soldering, it is the dissolving of the part or surface to be soldered into the molten solder. Specifically for hybrids, it is the undesirable action of gold dissolving, that is, leaching into solder whenever, perhaps, a thick-film fused gold pad was made of a less leach-resistant ink composition.

LEAD: A conductive path which is usually self-supporting.

LEAD EXTENSION: The portion of the component lead or wire protruding beyond the solder joint or package body.

LEADS, FLAT PACKAGE: Normally are round or rectangular in cross-section, protruding on one or all sides of flat package (flatpack). Leads in power package are made from materials with high electrical conductivity. To be differentiated from pins in plug-in package.

LEAD FRAMES: The metallic portion of the device package that completes the electrical connection path from the die or dice and from ancillary hybrid circuit elements to the outside world.

LEAD PROJECTION: The distance that a lead protrudes beyond the surface of the printed board.

LEAD WIRES: Wire conductors used for interconnections using fine wires (Cu, Au or Al), or interconnections that include input/output leads.

LEADLESS DEVICE: A chip device having no input/output leads.

LEAK RATE, MEASURED: The escape rate of the internal atmosphere, that is, the quantity of gas per unit time through single or multiple leak(s), under specified conditions, including a specified test medium; applicable to microelectronic and discrete semiconductor packaged devices with designed internal cavity, expressed in atmosphere cubic centimenters per second (atm-cm^3/sec).

LEAKAGE CURRENT: An undesirable small stray current which flows through or across an insulator between two or more electrodes, or across a back-biased junction.

LEVELING: A term describing the settling or smoothing out of the screen mesh marks in thick-films that takes place after a pattern is screen printed.

LID: A flat metal or ceramic piece, without a cavity, for the hermetic sealing of flatpacks and sidewalled packages. (See also stepped lid.)

LEGEND: Identification marks used for component identification, orientation and location during manufacturing or rework process.

LIFE DRIFT: The change in either absolute level or slope of a circuit element's parameter(s) under load. Rated as a percentage change from the original value per 1000 hours of life.

LIFE TEST: Test of a component or circuit under load over the rated life of the device.

LIFT-OFF MARK: Impression in bond areas left after lift-off removal of a bond.

LINE CERTIFICATION: Certification that a production line process sequence is under control and will produce reliable circuits in compliance with requirements of applicable mandatory documents.

LINE DEFINITION: A descriptive term indicating a capability of producing sharp, clean screen printed lines. The precision of line width is determined by twice the line edge definition/line width. A typical precision of 4% exists when the line edge definition/line width is 2%.

LINEAR CIRCUIT: A circuit with an output that changes in magnitude with relation to the input as defined by a constant factor (See analog circuits).

LINES: Conductor runs of a film network.

LIQUIDUS: The line on a phase diagram above which the system has molten components. The temperature at which melting starts.

LOAD LIFE: The extended period of time over which a device can withstand its full power rating.

LOOP: The curve or arc by the wire between the attachment points at each end of a wire bond.

LOOP HEIGHT: A measure of the deviation of the wire loop from the straight line between the attachment points of a wire bond. Usually, it is the maximum perpendicular distance from this line to the wire loop.

LOOSE FLLL (ANTI-STATIC): A type of packaging material, such as shreddings, flakes, and "peanuts" of plastic, properly treated during fabrication. The "peanuts" are electronic-grade, light-weight cushioning products usually made of expanded polystyrene and often provided with an anti-static coating.

LOSS TANGENTS: The decimal ratio of the irrecoverable to the recoverable part of the electrical energy introduced into an insulating material by the establishment of an electric field in the material.

LOW-LOSS SUBSTRATE: A substrate with high radio-frequency resistance and hence slight absorption of energy when used in a microwave integrated circuit.

M

MAGNET WIRE: Insulated copper wire, used chiefly for winding inductors and transformers used in power hybrids.

MAINTAINABILITY: The probability of completing corrective and/or preventive maintenance within a set time frame at a desired confidence level under a specified environment.

MANUAL TRIMMING: A laser trimming process in which the laser cut or notch in the deposited resistor is guided manually by the operator, based on instrument readings monitoring the results.

MARKING: The process of adding the legend to hybrid cover.

MASK: The photographic negative that serves as the master for making thick-film screens and thin-film patterns.

MASK ALIGNER: A semiautomatic machine used chiefly in hybrid technology for thin-film subtractive patterning. A first resist is applied to an area to be selectively exposed. In this process, the resist is exposed (by UV) through the first mask after aligning the glass mask artwork and the substrate in the mask

aligner; selective electroplating and photoetching follow. Upon application of a second photoresist coating, the procedure is repeated; the second glass mask, bearing the circuit image, is to be aligned precisely with ihe pattern on the substrate using the machine's X-Y chessman and microscope, prior to the second sequence of exposing by UV and photoetching.

MASS SPECTROMETER: An instrument used to determine the leak rate of a hermetically sealed package by ionizing the gas outflow permitting an analysis of the flow rate: in cm^3/sec at one atmosphere differential pressure.

MASTER BATCH PRINCIPLE: Blending resistor pastes to a nominal value of Ω/square. The nominal value is the master control number.

MASTER DRAWING: The reference design document that completely describes all conductive and nonconductive patterns, holes, and other features necessary to manufacture the product.

MASTER LAYOUT: The original layout of a circuit.

MATCHED SEAL: A metal-to-glass or metal-to-ceraminc seal, usually made up of Kovar as the metal. The metal is to be preconditioned by growing a black oxide on its surface to which the molten "hard" glass will adhere readily in a molecular bond, to result in a hermetically tight seal. The Kovar closely matches the TCE of the glasses and ceramics employed.

MATTE FINISH: A surface finish on a material that has a grain structure and diffuses reflected light.

MEAN TIME BETWEN FAILURES: The average time of satisfactory operation of a population of equipment. It is calculated by dividing the sum of the total operating time by the total number of failures.

MEAN TIME TO FAILURE: The expected value of first moment of the failure probability density function for unrepairable, one-shot products.

MEASURING JUNCTION: The junction in a thermocouple circuit which senses the temperature of the unknown object. It is commonly refered to as the hot junction.

MEDIAN: The point of continuous random variable which divides the distribution into two equal halves such that one half of the values are greater and one half smaller than the value of the subdividing point.

MESH SIZE: The number of openings per inch in a scren. A 200-mesh screen has 200 openings per linear inch, 40,000 openings per square inch.

METAL CLAD BASE MATERIAL: Base material covered on one or both sides with metallic foil.

METAL INCLUSION: Metal particles embedded in a nonmetal material such as ceramic substrate.

METAL MASK (SCREENS): A screen made not from wire or nylon thread but from a solid sheet of metal in which holes have been etched in the desired circuit pattern. Useful for precision and/or fine printing and for solder cream printing.

METALLIZATION: A film pattern (single or multilayer) of conductive material deposited on a substrate to interconnect electronic components, or the

metal film on the bonding area of a substrate which becomes a part of the bond and performs both an electrical and a mechanical function.

METAL-TO-GLASS SEAL (OR GLASS-TO-METAL SEAL): An insulating seal made between a package lead and the metal package by forming a glass bond to oxide layers on both metal parts. In this seal, the glass has a thermal coefficient of expansion that closely matches the metal parts.

METAL THERMAL VIAS: Internal risers in multilayer substrates to spread and dissipate heat by providing paths to a thermally-conducting plane which acts as a heat sink.

MICROBOND: A bond of a small wire such as 0.001-inch diameter gold to a conductor or to a chip device.

MICROCIRCUIT: A small circuit (hybrid or monolithic) having a relatively high equlvalent circuit element density, which is considered as a single part on (hybrid) or with (monolithic) a single substrate to perform an electronic circuit function. (This excludes printed wiring boards, circuit card assemblies, and modules composed exclusively of discrete electronic parts).

MICROCIRCUIT MODULE: An assembly of microcircuits or an assembly of microcircuits and discrete parts, designed to perform one or more electronic circuit functions, and constructed such that for the purposes of specification testing, commerce, and maintenance it is considered indivisible.

MICROCOMPONENTS: Small discrete components such as chip transistors and capacitors.

MICROFINISH: The term assumes different connotations for different material surfaces. For semiconductor wafers, microfinish signifies the surface condition just prior to doping; for ceramic substrates, it is a representation of the surface-roughness profile, expressed in micrometers CLA (center line average) and is indicative of the average value of peaks and valleys as measured; for metal packages, it is a plated finish free of porosity and of uniform thickness to a microinch.

MICRORACKS: A thin crack in a substrate or chip device, or in thick-film trim-kerf walls, that can only be seen under magnification and which can contribute to latent failure phenomena.

MICRON: An obsolete unit of length equal to a micrometer (μm).

MICROPOSITIONER: An instrument used in positioning a film substrate or device for bonding or trimming.

MICROPROBE: A small sharp-pointed probe with a positioning handle used in making temporary ohmic contact to a chip device or circuit substrate.

MICROSTRIP: A microwave transmission component usually on a ceramic substrate.

MICROSTRUCTURE: A structure composed of finely divided particles bound together.

MICROWAVE INTEGRATED CIRCUIT: A miniature microwave circuit usually using hybrid circuit technology to form the conductors and attach the chip devices, components.

MIGRATION: An undesirable phenomenon whereby metal ions, notable silver, are transmitted through another

metal, or across an insuiated surface, in the presence of moisture and an electrical potential.

MIL: A unit equal to 0.001 inches or 0.0254 mm.

MINIMUM ANNULAR RING: The minimum dimension between the drilled hole in a printed board or metallized ceramic substrate and the outer land edge.

MINIMUM ELECTRICAL SPACING: The minimum spacing required between electrical conductors to prevent dielectric breakdown or corona.

MISLOCATED BOND: See off bond. Misregistration: Improper alignment of successively produced features or patterns.

MODE: The maximum point of the frequency distribution of a continuous random variable.

MODULE: A generic form referring to separable units in electronic packaging.

MODULUS OF ELASTICITY: The ratio of stress to strain in a material that is elastically deformed.

MOISTURE STABILITY: The stability of a circuit under high-humidity conditions such that it will not malfunction.

MOLECULAR WEIGHT: The sum of the atomic weights of all atoms in a molecule.

MOLY TAB, OR KOVAR TAB. A small, flat piece of either metal, gold or nickel plated on both sides. In hybrid processing, a die as of a diode or a transistor, is eutectically bonded to the gold-plated surface of the tab. The moly tab (or Kovar tab) bearing the device later is epoxy attached or soldered to the substrate. Large diameter aluminum wires are bonded to nickel plated tabs for high current interconnects.

MONOCRYSTALLINE STRUCTURE: The granular structure of crystals which have uniform shapes and arrangements.

MONOLITHIC CERAMIC CAPACITOR: A term sometimes used to indicate a multilayer ceramic capacitor.

MONOLITHIC INTEGRATED CIRCUIT: An integrated circuit consisting of elements formed in situ on or within a semiconductor substrate with at least one of the elements formed within the substrate.

MOS DEVICE: Abbreviation for a metal oxide semiconductor device.

MOTHER BOARD: A circuit board used to interconnect smaller circuit boards called "daughter boards". A printed board assembly used to interconnect electronic modules.

MOUNTING SURFACE (OF A PACKAGE): The outside surface of a packaged device which is used for installing it in a second-level packaging scheme. The outside surface of a power hybrid case which is attached to heatsink for heat removal.

MULTICHIP INTEGRATED CIRCUIT: An integrated circuit whose elements are formed on or within two or more semiconductor chips which are separately attached to a substrate or header.

MULTICHIP (MICROCIRCUIT) MODULE: A microcircuit consisting solely of active dice and passive chips which are separately attached to the major substrate and interconnected to form the circuit.

MULTILAYER CERAMIC CAPACITOR:

A miniature ceramic capacitor manufactured by paralleling several thin layers of ceramic. The assembly is fired after the individual layers have been electroded and assembled.

MULTILAYER CIRCUITS. A composite circuit consisting of alternate layers of conductive circuitry and insulating materials (ceramic or dielectric compositions) bonded together with the conductive layers interconnected as required.

MULTILAYER SUBSTRATES. Substrates that have buried conductors so that complex circuitry can be handled. Assembled using processes similar to those used in multilayer ceramic capacitors. Fabricated either as a conventional MLC, or a co-fired multilayer ceramic (CMC) hybrid structure, in high and low temperature versions. They also include packages with CMC bottoms.

MULTILAYERED METALLIZATION: It denotes a processed substrate with two or more conductive (metal) layers which are not separated by an insulator; for example, nichrome, deposited gold, and plated gold.

MULTILAYER PRINTED BOARD: Printed circuit or printed wiring configuration that consists of more than two conductive layers bonded together to form a multiple conductive layer assembly. The term applies to both rigid and flexible multilayer boards.

MULTILEVEL PROCESSING: It concerns the stepwise processing required in producing a multilevel substrate using thick-film technology. The sequence consists of nominal steps which are repeated as specified. For example, screen print the first conductor layer through artwork, dry and fire; screen print insulative layer, dry and fire; backfill vias, dry and fire; screen print another insulative layer, dry and fire; backfill vias, dry and fire, screen print a third dielectric overprint, dry and fire; screen print the second conductive layer, dry and flire; and continue this sequence, as noted above. Note: The three layers of insulator are necessary for qood measure, to enhance reliability by eliminating the hazard of in-line pinholes possibly leading to internal shorts, and by assuring attainment of the full dielectric value.

MULTILEVEL SUBSTRATE. A processed hybrid substrate carrying several layers of conductive (metallized) patterns, each one separated by an insulative layer and interconnected by via holes. Two to five-level substrates are customary to accommodate fairly complex circuitry.

MULTIPLE CIRCUIT LAYOUT: Layout of an array of identical circuits on a substrate.

N

NAILHEAD BOND: See ball bond.

NAIL HEADING: Flaring of the conductive inner layers around drilled holes in a multilayered board.

NECK BREAK: A bond breaking immediately above gold ball of a thermocompression bond.

NEGATIVE ETCHBACK: Etchback characterized by recessed conductor layer material relative to the surrounding base material.

NEGATIVE IMAGE: The reverse print of a circuit.

NEGATIVE RESIST: Photoresist that is

polymerized by a specific wavelength of light and remains on the surface of a laminate after the unexposed areas are developed away.

NEGATIVE TEMPERATURE COEFFICIENT: The device changes its value in the negative direction with increased temperature.

NOBLE METAL PASTE: Paste materials composed partially of noble metals such as gold, platinum, palladium, or ruthenium.

NOISE: Random small variations in voltage or current in a circuit due to the quantum nature of electronic current flow, thermal considerations, etc.

NOMINAL RESISTANCE VALUE: The specified resistance value of the resistor at its rated load.

NONCONDUCTIVE EPOXY: An epoxy material (polymer resin) either without a filler or with a ceramic powder filler added to increase thermal conductivity and improve thixotropic properties. Nonconductive epoxy adhesives are used in chip or element to substrate bonds where electrical conductivity to the bottom of the chip is unnecessary or in substrate-to-package bonding.

NONCONDUCTIVE PATTERN: The pattern formed in the dielectric, resist, etc.

NONFUNCTIONAL LAND: A land that is not connected to the conductive pattern on that layer.

NONLINEAR DIELECTRIC: A capacitor material that has a nonlinear capacitance–voltage relationship. Titanate (usually barium titanate) ceramic capacitors (Class II) are nonlinear dielectrics. NPO and Class I capacitors are linear by definition.

NONPOLAR SOLVENTS: Solvents which are insufficiently ionized to be electrically conductive and which cannot dissolve polar compounds but can dissolve nonpolar compounds.

NONWETTING: A condition in which the solder has not adhered to all of the base metal, leaving some of the base metal exposed.

NUGGET: The region of recrystallized material at a bond interface which usually accompanies the melting of the materials at the interface.

O

OCCLUDED CONTAMINANTS: Contaminants that have been absorbed by a material.

OFF BOND: Bond that has some portion of the bond area extending off the bonding pad.

OFF CONTACT (SCREEN PRINTING): The opposite of contact printing in that the printer is set up with a space between the screen and the substrate and contacts the substrate only when the squeegee is cycled across the screen.

OFF CONTACT SCREENER: A screener machine that uses off contact printing of patterns onto substrates.

OFFSET LAND: A land pattern that is offset from its associated component.

OHMIC CONTACT: A contact that has linear voltage current characteristics throughout its entire operating range.

OHMS/SQUARE (Ω/SQUARE): The unit of sheet resistance or, more properly, of sheet resistivity.

OPERATOR CERTIFICATION: A program wherein an operator has been qualified and certified to operate a machine.

ORGANIC FLUX: A flux composed of

rosin base and a solvent.

ORGANIC VEHICLE: The organic vehicle in a flux is the rosin base material.

OUTGAS: The release of gas from a material over a period of time.

OUTGASSING: Gaseous emission from a material when exposed to reduced pressure and/or heat.

OUTGROWTH: Increase in conductor width beyond the conductor-resist boundary due to a plating buildup.

OVERBONDING: See chopped bond.

OVERCOAT: A thin-film of insulating material, either plastic or inorganic (e.g., glass or silicon nitride) applied over integral circuit elements for the purposes of mechanical protection and prevention of contamination.

OVERGLAZE: A glass coating that is grown, deposited, or secured over another element, normally for physical or electrical protection purposes.

OVERHANG: The amount of conductor and plating that extends beyond the conductor edge as defined at the conductor-base matcrial interface, which may be expressed as the sum of the outgrowth and undercut.

OVERLAP: The contact area between dissimilar (film) materials, e.g., between a film resistor and its termination(s).

OVERLAY: One material applied over another material.

OVERSPRAY: The unwanted spreading of the abrasive material coming from the trim nozzle in an abrasive resistor trimming machine. The overspray affects the values of adjacent resistors not intended to be trimmed.

OVERTRAVEL: The excess downward distance of a squeegee blade would push the screen if the substrate were not in position.

OXIDIZING ATMOSPHERE: An air or other oxygen-containing atmosphere in a firing furnace which oxidizes the resistor materials while they are in the molten state, thereby increasing their resistance.

P

PACKAGE: The container for an electronic component(s) with terminals to provide electrical access to the inside of the container. In addition, the container usually provides hermetic and environmental protection for, and a particular form factor to, the assembly of electronic components. A package generally consists of the bottom part called the case or header, and the top part, called the cover or lid; these are sealed into one unit.

PACKAGE CAP: The cuplike cover that encloses the package in the final sealing operation.

PACKAGE LID: A flat cover plate that is used to seal a package cavity.

PACKAGING DENSITY: The amount of function per unit volume, often defined qualitatively as high, medium, or low.

PAD: A metallized area on the surface of an active substrate as an integral portion of the conductive interconnection pattern to which bonds or test probes may be applied.

PAD GRID ARRAY: A package that is an SMT derivative of PGA; substituting soldering pads on the underside for the customary pins.

PANEL: A rectangular or square section of base material containing printed boards and any required test coupons.

PANEL PLATING: A plating process in which the holes and surface of the panel are all plated.

PARALLEL-GAP SOLDER: Passing a high current through a high-resistance gap between two electrodes to remelt solder, thereby forming an electrical connection.

PARALLEL-GAP WELD: Passing a high current through a high-resistance gap between two electrodes that are applying force to two conductors, thereby heating the two workpieces to the welding temperature and effecting a welded connection.

PARALLELISM (SUBSTRATE): The degree of variation in the uniform thickness of a given substrate.

PARASITIC LOSSES: Losses in a circuit often caused by the unintentional creation of capacitor elements in a film circuit by conductor crossovers, or between a substrate metallization pattern and case.

PARTIAL LIFE: A bonded lead partially removed from the bonded area.

PASSIVATED REGION: Any region covered by glass, SiO_2, nitride, or other protective material.

PASSIVATION: The formation of an insulating layer directly over a circuit or circuit element to protect the surface from contaminants, moisture, or particles.

PASSIVE COMPONENTS (ELEMENTS): Elements (or components) such as resistors, capacitors, and inductors which do not change their basic character when an electrical signal is applied. Transistors, diodes and electron tubes are active components.

PASSIVE NETWORK: A circuit network of passive elements such as film resistors that are interconnected by conductors.

PASSIVE SUBSTRATE: A substrate that serves as a physical support and thermal sink for a film circuit that does not exhibit transistance.

PASTE: Synonymous with "composition" and "ink" when relating to screenable thick-film materials.

PASTE BLENDING: Mixing resistor pastes of different Ω/square value to create a third value in between those of the two original materials.

PASTE SOLDERING: Finely divided particles of solder suspended in a flux paste. Used for screening application onto a film circuit and reflowed to form connections to chip components.

PASTE TRANSFER: The movement of a resistor, conductor, or solder paste material through a mask and deposition in a pattern onto a substrate.

PATTERN: The outline of a collection of circuit conductors and resistors that defines the area to be covered by the material on a film circuit substrate.

PATTERN PLATING: A process in which a selective conductive pattern is plated.

PEAK FIRING TEMPERATURE: The maximum temperatures seen by the resistor or conductor paste in the firing cycle as defined by the firing profile.

PEEL BOND: Similar to lift-off of the bond with the idea that the separation of the lead from the bonding surface proceeds along the interface of the mettallization and substrate insulation rather than the bond-metal surface.

PEEL STRENGTH (PEEL TEST): A measure of adhesion between a conduc-

tor and the substrate. The test is performed by pulling or peeling the conductor off the substrate and observing the force required. Preferred unit is g/mm or kg/m of conductor width.

PERCENT DEFECTIVE ALLOWABLE (PDA): The maximum observed per cent defective which will permit the lot to be accepted after the specified 100% test.

PERIMETER SEALING AREA: The sealing area surface of an electronic package that follows the perimeter of the package cavity and defines the area used in bonding to the lid or cap.

PERMANENT MASK: A masked pattern from resist that is not removed after processing.

PERMEABILITY: (1) The passage by diffusion (or rate of passage) of a gas, vapor, liquid, or solid through a barrier without physically or chemically affecting it. (2) The ability of a material to carry magnetism, compared to air, which has a permeability of 1.

PHASE: (As glassy phase or metal phase). Refers to, the part or portion of materials system that is metallic or glassy in nature. A phase is a structurally homogeneons physically distinct portion of a substance or a group of substances which are in equilibrium with each other.

PHASE DIAGRAM: State of a metal alloy over a wide temperature range. The phase diagram is used to identify eutectic solders and their solidus/liquidus point.

PHOTO ETCH: The process of forming a circuit pattern in metal film by light hardening a photosensitive plastic material through a photo negative of the circuit and etching away the unprotected metal.

PHOTOGRAPHIC REDUCTION DIMENSION: Dimensions called out on the artwork master indicating the amount of photographic reduction required.

PHOTORESIST: A photosensitive plastic coating material which when exposed to UV light becomes hardened and is resistant to, etching solutions. Typical use is as a mask in photochemical etching of thin-films.

PIGTAIL: A term that describes the amount of excess wire that remains at a bond site beyond the bond. Excess pigtail refers to remnant wire in excess of three wire diameters.

PIN: Round, cross-sectional electrical terminal and/or mechanical support. Used in plug-in type packages in several forms, such as straight cut, upset, turreted, nail head, stepped, flattened, flat and pierced, or bent. The pin's primary functions are, internally, to support a wire bond or other joint, and externally, to plug into second level packaging loci to provide electrical connection and mechanical support.

PIN, COPPER CORED: A round pin formed of sealing alloy around a central core of copper.

PIN DENSITY: The number ot pins per unit area on a printed board.

PINHOLE: Small holes occurring as imperfections which penetrate entirely through film elements, such as metallization films or dielectric films.

PINOUT: Slang expression for "pin pattern".

PIN PATTERN: The outline of package pins with reference to package outline.

PITCH: The nominal centerline-to-cen-

terline dimension between adjacent conductors.

PITS: Depressions produced in metal or ceramic surfaces by nonuniform deposition.

PLANAR MOUNTED DEVICE LEAD: A component lead configuration designed to sit flush on a printed board land pattern and characterized by a gull-wing configuration.

PLASTIC: A polymeric material, either organic (e.g., epoxy) or silicone used for conformal coating, encapsulation, or overcoating.

PLASTIC DEVICE: A device wherein the package, or the encapsulant material for the semiconductor die, is plastic. Such materials as epoxies, phenolics, silicones, etc. are included.

PLASTIC ENCAPSULATION: Environmental protection of a completed circuit by embedding it in a plastic such as epoxy or silicone.

PLASTIC SHELL: A thin plastic cup or box used to enclose an electronic circuit for environmental protection or used as a means to confine the plastic encapsulant used to imbed the circuit.

PLATE FINISH: The finish on the metal-clad base material after contact with the press plates during the lamination process.

PLATED THROUGH HOLE: A hole with a plated wall used for electrical interconnection between internal and/or external conductive layers.

PLATING BAR: A temporary electrically conductive bar used to interconnect areas to be electroplated.

PLATING, BURNED: Rough and dull electrodeposit plating that is caused by excessive plating current density.

PLATING UP: The process of electrochemical deposition of conductive material on activated base material.

PLUG-IN-PACKAGE: An electronic package with pins strong enough and arranged on one surface so that the package can be plugged into a test or mounting socket and removed for replacement as desired without destruction.

POINT-TO-POINT WIRING: An interconnecting technique wherein the connections between components are made by wires routed between connecting points.

POISSON RATIO: The proportionality ratio of a lateral strain to an axial strain when a material is placed in tension.

POLARIZATION: The elimination of inplane symmetry so that parts can be engaged in only one way.

POLAR SOLVENTS: Sufficiently ionized solvents that can dissolve polar solvents but cannot dissolve nonpolar compounds.

POLYCRYSTALLINE: A material is polycrystalline in nature if it is made of many small crystals. Alumina ceramics are polycrystalline, whereas glass substrates are amorphous.

POLYNARY: A material system with many basic compounds as ingredients, as thick-film resistor compositions. Binary indicates two compounds; ternary, three, etc.

POROSITY: The ratio of solid matter to voids in a material.

POSITIVE: An artwork or production master in which the transparent regions represent areas to be free of conductive material.

POSITIVE IMAGE: The true picture of a

circuit pattern as opposed to the negative image or reversed image.

POSITIVE RESIST: A resist that softens when exposed to a certain wavelength of light and that is removed after exposure and developing.

POSITIVE TEMPERATURE COEFFICIENT: The changing of a value in the positive direction with increasing tempersture.

POST: See terminal.

POSTCURING: Heat aging of a film circuit after firing to stabilize the resistor values through stress relieving.

POSTFIRING: Refiring a film circuit after having gone through the firing cycle. Sometimes used to change the values of the already fired resistors.

POSTSTRESS ELECTRICAL: The application of an electrical load to a film circuit to stress the resistors and evaluate the resulting change in values.

POTTING: Encapsulating a circuit in plastic.

POWER DENSITY: The amount of power dissipated in a component mounted on a substrate, through the substrate measured in watts/in^2.

POWER DISSIPATION: The dispersion of the heat generated from a film circuit when a current flows through it.

POWER FACTOR: The ratio of the actual power of an alternating or pulsating current as measured by an ammeter and voltmeter.

POWER HYBRID: Hybrid microcircuit which contains high power dissipating components.

POWER PACKAGE: In the microelectronics industry power package refers to an enclosure for a single power semiconductor device, or power hybrid circuit. It generally has a bottom made from materials with high thermal conductivity, and with flanges with mounting holes. Leads are made from materials with high electrical conductivity, and have large diameter; they may be formed upwards or downwards.

PREFIRED: Film conductors fired in advance of film resistors on a substrate.

PREFORM: An aid in soldering or in other types of adhesion functions. Preforms are generally circular or squareshaped, punched out of thin sheets of solder, of epoxy, or of eutectic alloy. They are placed on the spot of attachment by soldering or by bonding, prior to placing the object proper there to be heated.

PREOXIDIZED: Resistor metal particles that have been oxidized to achieve the desired resistivity prior to formulation into a resistor ink.

PREPREG: Sheet material or fabric impregnated with resin and partially cured (B-stage).

PRESEAL VISUAL: The process of visual inspection of a completed hybrid circuit assembly for defects prior to sealing the package.

PRESSED ALUMINA: Aluminum oxide ceramic formed by applying pressure to the ceramic powder and a binder prior to firing in a kiln.

PRESS-FIT CONTACT: An electrical contact that is press-fit into a hole.

PRINT AND FIRE: A term sometimes used to indicate steps in the thick-film process wherein the ink is printed on a substrate and is fired.

PRINTED BOARD: The generic term for processed printed circuit and printed wiring boards, either single or double

and multilayer boards.

PRINTED CIRCUIT BOARD: A printed board that consists of conductive pattern which includes printed components and/or printed wiring.

PRINTED CIRCUIT ASSEMBLY: One or more populated printed circuit boards that perform a specific function in a system.

PRINTED COMPONENT: A component, such as a resistor, coil, or capacitor, which is formed in the conductive pattern.

PRINTED CONTACT: A contact area that is formed in the conductive pattern.

PRINTED WIRING BOARD: A printed board containing a conductive pattern which consists only of printed wiring.

PRINTED WIRING ASSEMBLY: One or more populated printed wiring boards that perform a specific function in a system.

PRINTED WIRING LAYOUT: A design document that depicts the printed wiring, electrical, and mechanical component sizes and locations with sufficient detail that documentation and artwork may be generated from the document.

PRINT LAYDOWN: Screening of the film circuit pattern onto a substrate.

PRINTING: Same as print layout.

PRINTING PARAMETERS: The conditions that affect the screening operation such as off-contact spacing, speed and pressure of squeegee, etc.

PROBE: A pointed conductor used in making electrical contact to a circuit pad for testing.

PROCURING ACTIVITY: The organizational element (equipment manufacturer, government, contractor, subcontractor, or other responsible organization) which contracts for articles, supplies, or serviccs and has the authority to grant waivers, deviations, or exceptions to the procurement documents.

PRODUCT: An item, component, device, group of devices, or system.

PRODUCT ASSURANCE: A technical management operation reporting to top management and devoted to the study, planning, and implementation of the required design, controls, methods, and techniques to ensure a reliable product in conformity with its applicable specification.

PRODUCTION LOT: Hybrid microcircuits manufactured on the same production line(s) by means of the same production techniques, materials, controls, and design. The production lot is usually date coded to permit control and traceability required for maintenance of reliability programs.

PRODUCTION MASTER: A 1:1 scale pattern for all the layers required to manufacture a printed board base on the master drawing. The production master may have more than one pattern for making more than one printed board on a panel.

PROPERTY: The physical, chemical, or electrical characteristic of a given material.

PULL STRENGTH: The values of the pressure achieved in a test where a pulling stress is applied to determine breaking strength af a lead or bond.

PULL TEST: A test for bond strength of a lead, interconnecting wire, or conductor.

PULSE SOLDERING: Soldering a connection by melting the solder in the joint area by pulsing current through a high-resistance point applied to the joint area and the solder.

PURGE: To evacuate an area or volume space of all unwanted gases, moisrure, or contaminants prior to backfilling with an inert gas.

PURPLE PLAGUE: One of several gold-aluminum compounds formed when bonding gold to aluminum and activated by reexposure to moisture and high temperature (>340°C). Purple plague is purplish in color and is very brittle, potentially leading to time-based failure of the bonds. Its growth is highly enhanced by the presence of silicon to form ternary compounds.

PUSH-OFF STRENGTH: The amount of force required to dislodge a chip device from its mounting pad by application of the force to one side of the device, parallel to the mounting surface.

PYROLYZED (BURNED): A material that has gained its final form by the action of heat is said to be pyrolyzed.

Q

Q: The inverse ratio of the frequency band between half-power points (bandwidth) to the resonant frequency of the oscillating system. Refers to the electromechanical system of an ultrasonic bonder, or sensitivity of the mechanical resonance to changes in driving frequency.

QUALITY ASSURANCE: A technique or science which uses all the known methods of quality control and quality engineering to ensure the manufacture of a product of acceptable quality standards.

QUALITY CONFORMANCE TEST CIRCUITRY: A section of a printed board containing test coupons used to determine the board's acceptability.

R

RADIOGRAPHS: Photographs made of the interior of a package by use of X-rays to expose the film.

RANDOM FAILURES: Circuit failures which occur randomly with the overall failure rate for the sample population being nearly constant.

RC NETWORK: A network composed only of resistors and capacitors.

RCL NETWORK: A network composed only of resistors, and capacitors, and inductors.

REACTIVE METAL: Metals that readily form compounds.

REAL ESTATE: The surface area of an integrated circuit or of a substrate. The surface area required for a component or element.

REBOND: A second bonding attempt after a bond made on top of a removed or damaged bond or a second bond made immediately adjacent to the first bond.

REDUCING ATMOSPHERE: An atmosphere containing a gas such as hydrogen that will reduce the oxidation state of the subject compound.

REDUCTION DIMENSION: A dimension specified on enlarged scale matrices between a pair of marks which are positioned in very accurate alignment with the horizontal center locations of two manufacturing holds and their locationally coincident targets. This dimension is used to indicate and verify the exact horizontal distance required between the two targets when the matrices are photographically reduced to full

size.

REDUNDANCY: The existence of more than one means of accomplishing a given task where all means must fail before there is an overall failure of the system. Parallel redundancy applies to systems in which both means are working at the same time to accomplish the task and either of the systems is capable of handling the job itself in case of failure of the other system. Standby redundancy applies to a system in which there is an alternative means of accomplishing the task that is switched in by a malfunction-sensing device when the primary system fails.

REFERENCE EDGE: The edge of a cable or conductor used as a reference for making measurements.

REFERENCE JUNCTION: The junction in a thermocouple circuit which is maintained at a constant, known temperature. It is also refered to as the cold junction and as a standard it is usually maintained at 0°C, however, any temperature can be used.

REFIRING: Recycling a thick-film resistor through the firing cycle to change the resistor value.

REFLOW SOLDERING: A method of soldering involving application of solder prior to the actual joining. To solder, the parts are joined and heated, causing the solder to remelt, or reflow.

REFRACTORY METAL: Metal having a very high melting point, such a molybdenum.

REGISTRATION: The alignment of a circuit pattern on a substrate.

REGISTRATION MARKS: The marks used for aligning successive processing masks.

REINFORCED PLASTIC: Plastic having reinforcing materials such as fiberglass embedded or laminated in the cured plastic.

RELIABILITY: The probability that a product will perform a stated function satisfactorily at a desired confidence level for a set period of time under a specified environment.

RELIABILITY ASSURANCE: A technique or science which assesses the reliability of a product by means of surveillance and measurement of the factors of design and production which affect it.

REPAIR: An operation performed on a nonconforming part or assembly to make it functionally usable but which does not completely eliminate the nonconformance.

RESIDUAL GAS ANALYSIS (RGA): A method of analysis to determine the composition of a hermetically sealed device's internal atmosphere. It is capable of detecting among the released gases, the exact water-vapor content in parts per million for a given volume package. In this method, the device, placed in a vacuum opening chamber, pumped down and baked out, is mechanically pierced through its enclosure and the escaping gas and water vapor are led through a transfer passage to a mass spectrometer for analysis and interpretation.

RESIST: A protective coating that will keep another material from attaching or coating something, as in solder resist, plating resist, or photoresist.

RESISTANCE SOLDERING: A soldering

process in which current passing through one or more electrodes heats the soldering area.

RESISTANCE WELD: The joining of two conductors by heat and pressure with the heat generated by passing a high current through the two mechanically joined materials.

RESISTIVITY: A proportionality factor characteristic of different substances equal to the resistance that a centimeter cube of the substance offers to the passage of electricity, the current being $R = \rho L/A$, where R is the resistance of a uniform conductor, L its length, A its cross-sectional area, and ρ its resistivity. Resistivity is usually expressed in ohm–centimeters. The ability of a material to resist passage of electrical current either through its bulk or on a surface.

RESISTOR DRIFT: The change in resis- tance of a resistor through aging and usually rated as percent change per 1000 hr.

RESISTOR GEOMETRY: The film resistor outline.

RESISTOR OVERLAP: The contact area between a film resistor and a film conductor.

RESISTOR PASTE CALIBRATION: Characterization of a resistor paste for Ω/square value, TCR, and other specified parameters by screening and firing a test pattern using the paste and recording the results.

RESISTOR TERMINATION: See resistor overlap.

RESOLUTION: The degree of fineness or detail of a screen printed pattern (see line definition).

REVERSE CURRENT CLEANING: Electrolytic cleaning using the part to be cleaned as the anode.

REVERSE IMAGE: The resin pattern on a printed board exposing the conductive areas to be plated.

REVERSION: A chemical reaction resulting in a polymerized material that degenerates to a lower polymeric state or to the original monomer.

REWORK: An operation performed on a nonconforming part or assembly that restores all nonconforming characteristics to the requirements in the contract, specification, drawing, or other approved product description.

RHEOLOGY: The science dealing with deformation and flow of matter.

RIBBON INTERCONNECT: A flat narrow ribbon of metal such as nickel, aluminum, copper or gold used to interconnect circuit elements or to connect the element to the output pins.

RIBBON WIRE: Metal in the form of a very flexible flat thread or slender rod or bar tending to have a rectangular cross section as opposed to a round cross section.

RIGID COATING: A conformal coating of thermosetting plastic that has no fillers or plasticizers to keep the coating pliable.

RING FRAME: A one-piece, flange-like frame, square or rectangular or of another shape which, after its attachment, forms the package sidewalls in planar metal or in plug-in metal packages, or the sidewalls of a ceramic chip carrier, fitting its substrate contour, thereby creating a cavity.

RISERS: The conductive paths that run vertically from one level of conductors to another in a multilayer substrate or

screen-printed film circuit.

ROADMAP: A pattern printed on nonconductive material used to delineate components and circuitry to facilitate repair and servicing.

ROSIN FLUX: A flux having a rosin base which becomes interactive after being subjected to the soldering temperature.

ROSIN SOLDER CONNECTION (ROSIN JOINT): A soldered joint in which one of the parts is surrounded by an almost invisible film of insulating rosin, making the joint intermittently or continuously open even though the joint looks good.

S

SAGGING OR WIRE SAG: The failure of bonding wire to form the loop defined by the path of the bonding tool between bonds.

SAMPLE: A random selection of units from a lot for the purpose of evaluating the characteristics or acceptability of the lot. The sample may be either in terms of units or in terms of time.

SAPPHIRE: A single-crystal Al_2O_3 substrate material used in integrated circuits.

SCALING: Peeling of a film conductor or film resistor from a substrate, indicating poor adhesion.

SCALLOP MARKS: A screening defect which is characterized by a print having jagged edges. This condition is a result of incorrect dynamic printing pressure or insufficient emulsion thickness.

SCAVENGING: Same as leaching.

SCHEMATIC: Diagram of a functional electronic circuit composed of symbols of all active and passive elements and their interconnecting matrix that forms the circuit.

SCORED SUBSTRATE (SNAPSTRATE): A substrate that has been scribed with a thin cut at the break-lines.

SCRATCH: In optical observations a surface mark with a large length-to-width ratio.

SCREEN: A network of metal or fabric strands, mounted snugly on a frame, and upon which the film circuit patterns and configurations are superimposed by photographic means.

SCREEN DEPOSITION: The laydown of a circuit pattern on a substrate using the silk screening technique.

SCREEN FRAME: A metal, wood, or plastic frame that holds the silk or stainless steel screen tautly in place.

SCREENING: The process whereby the desired film circuit patterns and configurations are transferred to the surface of the substrate during manufacture, by forcing a material through the open areas of the screen using the wiping action of a soft squeegee.

SCREEN PRINTING: The process in which an image is transferred to a substrate by forcing screen-printable material through a stencil or image screen using a squeegee.

SCRIBE COAT: A two-layer system, sometimes used for the preparation of thick-film circuit artwork, consisting of a translucent, dimensionally stable, polyester base layer covered with a soft, opaque, strippable layer and normally processed on a coordinatograph machine (see cut and strip).

SCRUBBING ACTION: Rubbing a chip device around on a bonding pad during the bonding operation to break up the oxide layer and improve wettability of

the eutectic alloy used in forming the bond.

SEALING: The process of permanently attaching a lid or cover to a hybrid case using seam weld, solder, or epoxy.

SEAL RING: A rectangular frame of metal or metallized insulator (like ceramic, glass, or plastic) assuming the contour of a backage base, chip carrier, or substrate while permanently attached to it, providing a weldable or solderable surface when being joined to a cover or a lid in a sealing operation.

SEAM WELD: Weld used to seal the lid on a package by performing a series of overlapping spot welds simultaneously on the opposite sides of the lid. The welder's electrodes stay in constant contact with the lid and move continuously while the power supply is rapidly pulsed. This process usually requires a stepped lid.

SEARCH HEIGHT: The height of the bonding tools above the bonding area at which final adjustments in the location of the bonding area under the tool are made prior to lowering the tool for bonding.

SECOND BOND: The second bond of a bond pair made to form a conductive connection.

SECOND RADIUS: The radius of the back edge of the bonding tool foot.

SECOND SEARCH: That period of machine cycle at which final adjustments in the location of the second bonding area (see second bond) under the tool are made prior to lowering the tool for making the second wire bond.

SELECTIVE ETCH: Restricting the etching action on a pattern by the use of selective chemical which attack only one of the exposed materials.

SELF-HEATING: Generation of heat within a body by chemical action. Epoxy materials self-heat in curing due to exothermic reaction.

SELF-PASSIVATING GLAZE: The glassy material in a thick-film resistor that comes to the surface and seals the surface against moisture.

SEMIADDITIVE PROCESS: An additive conductive patterning process combining electroless metal deposition on an unclad or foil substrate with electroplating, with etching, or with both.

SEMICONDUCTOR CARRIER: A permanent protective structure which provides for mounting and for electrical continuity in application of a semiconductor chip to a major substrate.

SEMICONDUCTORS: Solid materials such as silicon that have a resistivity midway between those of a conductor and a resistor. These materials are used as substrates for semiconductor devices such as transistors, diodes, and integrated circuits.

SERPENTINE CUT: A trim cut in a film resistor that follows a serpentine or wiggly pattern to effectively increase the resistor length and increase resistance.

SHEAR RATE: The relative rate of flow or movement (of viscous fluids).

SHEAR STRENGTH: The limiting stress of a material determined by measuring a strain resulting from applied forces that cause or tend to cause bonded contiguous parts of a body to slide relative to each other in a direction parallel to

their plane of contact; the value of the force achieved when shearing stress is applied to the bond (normally parallel to the substrate) to determine the breaking load. Strength to withstand shearing of a material.

SHEET RESISTANCE (RESISTIVITY): The electrical resistance of a thin sheet of a material with uniform thickness as measured across opposite sides of a unit square pattern. Expressed in Ω/square.

SHELF LIFE: The maximum length of time, usually measured in months, between the date of shipment of a material to a customer and the date by which it should be used for best results.

SHIELDING, ELECTRONIC: A barrier designed to reduce the interaction of components and portions of circuits with magnetic fields.

SHORT-TERM OVERLOAD: Overload of a circuit with current or voltage for a period too short to cause breakdown of the insulation.

SIGNAL: An electrical impulse of specified voltage, current, polarity, and pulse width.

SIGNAL CONDUCTOR: An electrical conductor used to transmit a signal.

SIGNAL PLANE: A conductive layer designed to carry signals, as opposed to ground or fixed voltages.

SILICON MONOXIDE: A passivating or insulating material that is vapor deposited on selected areas of a thin-film circuit.

SILK SCREEN: A screen of a closely woven silk mesh stretched over a frame and used to hold an emulsion outlining a circuit pattern and used in screen printing of film circuits. Used generically to describe any screen (stainless steel or nylon) used for screen printing.

SINGLE-SIDED BOARD: A printed board with only one conductive layer.

SINKING: Shorting of one conductor to another on multilayer screen printed circuits because of a downward movement of the top conductor through the molten crossover glass.

SINTERING: Heating a metal powder under pressure and causing the particles to bond together in a mass. Alternately, subjecting a ceramic-powder mix to a firing cycle whereby the mix is less than completely fused and shrinks.

SKIN EFFECT: The increase in resistance of a conductor at high frequencies because of the tendency for current to concentrate at the conductor surface.

SLICE: A thin crosssection of a crystal such as silicon that is used for semiconductor substrates.

SLIVERS: Plating material overhanging a conductor edge or completely detached from the rest of the plating which can cause potential electrical shorts.

SLUMP: A spreading of printed thick-film composition after screen printing but before drying. Too much slumping results in loss of definition.

SLURRY: A thick mixture of liquid and solids, the solids being in suspension in the liquid.

SMEARED BOND: A bond impression that has been distorted or enlarged by excess lateral movement of the bonding tool, or by the movement of the device-holding fixture.

SNAPBACK: The return of a screen to

normal after being deflected by the squeegee moving across the screen and substrate.

SNAP-OFF DISTANCE: The screen printer distance setting between the bottom of the screen and top of the substrate (see breakaway).

SNAPSTRATE: A scribed substrate that can be processed by gang deposition in multiples of circuits and snapped apart afterward.

SOAK TIME: The length of time a ceramic material (such as a substrate or thick-film composition) is held at the peak temperature of the firing cycle.

SOFT SOLDER: A low temperature melting solder, generally a lead, tin, indium containing alloy, with a melting point below 425°C.

SOLDER ACCEPTANCE: Same as solderability.

SOLDER BALLS: Small solder spheres that adhere to the surface of the printing board after reflow or wave soldering. The solder balls are more predominant with an uncontrolled soldering process using solder paste.

SOLDER BRIDGING: A short between two or more conductors due to solder.

SOLDER BUMPS: The round solder balls bonded to a transistor contact area and used to make connection to a conductor by face-down bonding techniques.

SOLDER COAT: A solder layer applied directly to the surface conductive layer of a printed board or ceramic substrate through exposure of molten solder.

SOLDER CONNECTION: An electrical or mechanical connection between two metal parts formed by solder.

* Disturbed solder connection — a cold solder joint resulting from movement of one or more of the parts during solidification.

* Excess solder connection — a solder joint containing so much solder that the joined part contours are not visible. Also refers to solder that has flowed beyond the designated solder area.

* Insufficient solder connection — a solder joint characterized by one or more of the parts incompletely covered by solder.

* Overheated solder connection — a solder joint characterized by a dull, chaulky, grainy, and porous/pitted appearance which is the result of excess heat application during the solder process.

* Preferred solder connection — a smooth, bright, and well-wetted solder connection with no exposed bare lead material and no sharp protrusions or embedded foreign material with the lead contours visible.

* Rosin solder connection — a solder connection which has a cold solder joint appearance but is further characterized by rosin flux entrapment separating the surfaces to be joined.

SOLDER CUP TERMINAL: A metallic terminal with a cylindrical feature at one end used for soldering one or more leads or wires.

SOLDER DAM: A dielectric composition screened across a conductor to limit molten solder from spreading further onto solderable conductors.

SOLDER FILLET: A rounded and blended solder configuration around a component or wire lead and the land

pattern.

SOLDER GLASSES: Glasses used in package sealing that have a low melting point and tend to wet metal and ceramic surfaces.

SOLDER IMMERSION TEST: A test that immerses the electronic package leads into a solder bath to check resistance to soldering temperatures.

SOLDER LEVELING: A process using heated gas or other material to remove excess solder.

SOLDER PASTE: A composition of metal (Sn/Pb) powder, flux, and other orpanic vehicles.

SOLDER PROJECTION: An undesirable solder protrusion from a solidified joint.

SOLDER RESIST: A material used to localize and control the size of soldering areas, usually around component mounting and wirebonding pads. The solderable areas are defined by the solder resist matrix.

SOLDERABILITY: The ability of a conductor to be wetted by solder and to form a strong bond with the solder.

SOLDERING: The process of joining metals by fusion and solidification of an adherent alloy having a melting point below about 427°C.

SOLDERING IRON TIP: The end of a soldering iron that has been plated with iron, nickel, chromium, or a similar metal which is used to heat solder to reflow temperature.

SOLDER SIDE: The side of the board opposite the component bodies and where the leads are soldered to the conductive pattern on the printed board.

SOLDER WICKING: The rising of solder between individual strands of wire due to capillary action.

SOLID METAL MASK: A thin sheet of metal with an etched pattern used in contact printing of film circuits.

SOLID-PHASE BOND: The formation of a bond between two parts in the absence of any liquid phase at any time prior to or during the joining process.

SOLID STATE: Pertaining to circuits and components using semiconductors as substrates.

SOLID TANTALUM CHIP CAPACITOR: A chip or leadless capacitor whose dielectric (Ta_2O_5) is formed with a solid electrolyte instead of a liquid electrolyte.

SOLIDUS: The locus of points in a phase diagram representing the temperature, under equilibrium conditions, at which each composition in the system begins to melt during heating, or complete freezing during cooling.

SOLUBILITY: The ability of a substance to dissolve into a solvent.

SOLVENT: A material that has the ability to dissolve other materials.

SOLVENT-RESISTANT MATERIAL: A material that is unaffected by solvents and does not degrade when cleaned in solvents.

SPACING: The distance between adjacent conductor edges.

SPAN: The distance between the reference edges of the first and last conductors.

SPECIFIC GRAVITY: The density (mass/unit volume) of any material divided by that of water at a standard temperature.

SPECIFIC HEAT: The ratio of the heat capacities of a body and water at a reference temperature; i.e., the quantity of

heat required to raise the temperature of 1 gram of a substance by 1°C.

SPECIMEN: A sample ot material, device, or circuit representing the production lot removed for test.

SPINEL: A hard, single-crystal mineral of magnesium aluminum oxide, $MgAl_2O_4$ used as substrate in special integrated circuit structures.

SPLAY: A drill bit's tendency to produce off center, out-of-round, and nonperpendicular holes.

SPUTTERING: The removal of atoms from a source by energetic ion bombardment, the ions supplied by a plasma. Process is used to deposit films for various thin-film applications.

SQUASHOUT: The deformed area of a lead which extends beyond the dimensions of the lead prior to bonding.

SQUEEGEE: The part of a screen printer that pushes the composition across the screen and through the mesh onto the substrate.

STABILIZATION BAKE: Application of heat treatment to completed (hybrid) devices aimed at stabilizing circuit parameters. Baking is done in an air oven at specified temperature for specified length of time.

STAINLESS STEEL SCREEN: A stainless steel mesh screen stretched across a frame and used to support a circuit pattern defined by an emulsion bonded to the screen.

STAIR-STEP PRINT: A print which retains the pattern of the screen mesh at the line edges. This is a result of inadequate dynamic printing pressure on the paste or insufficient emulsion thickness coating the screen.

STAMPED PRINTED WIRING: Wiring produced by stamping and mounting to a dielectric base material.

STANDARD DEVIATION: A statistical term that helps describe the likely value of parts in a lot or batch of components in comparison with the lot's average value. Practically all of a lot will fall within 3 standard deviations of the average value if it is a normal distribution.

STANDOFF: A connecting post of metal bonded to a conductor and raised above the surface of the film circuit.

STEATITE: A ceramic consisting chiefly of a silicate of magnesium used as an insulator or circuit substrate.

STENCIL: A thin sheet material with a circuit pattem cut into the material. A metal mask is a stencil.

STEP-AND-REPEAT: A process wherein the conductor or resistor pattern is repeated many times in evenly spaced rows onto a single film or substrate.

STEP SCALE STEP-WEDGE: A scale of evenly spaced tones ranging from clear to black through intermediate shades of gray used as a reference in photographic reproductions.

STEP SOLDERING: A soldering process using solder alloys with different melting points.

STEPPED LID: A flat lid with a flange on the outside of the lid to make it self locating. The flange is normally thinner than the lid, which aids in welding

STITCH BOND: A bond made with a capillary-type bonding tool when the wire is not formed into a ball prior to bonding.

STRATIFICATION: The separation of

nonvolatile components of a thick-film into horizontal layers during firing, due to large differences in density of the component. It is more likely to occur with a glass containing conductor paste and under prolonged or repeated firing.

STRAY CAPACITANCE: Capacitance developed from adjacent conductors separated by an air dielectric or dielectric material.

STRESS RELIEVE: A process of reheating a film resistor to make it stress free. A portion of a component or wire lead, or wire bond that is sufficiently long to minimize stresses.

STRESS-FREE MATERIAL: The annealed or stress-relieved material in which the molecules are no longer in tension.

STRIPLINE: A microwave conductor on a substrate. A transmission line configuration consisting of a conductor equally spaced between two parallel ground planes.

STYLUS: A sharp-pointed probe used in making an electrical contact on the pad of a leadless device or a film circuit.

SUBCARRIER SUBSTRATE: A small substrate of a film circuit which is mounted in turn to a larger substrate.

SUBSTRATE (OF A MICROCIRCUIT OR INTEGRATED CIRCUIT): The supporting material upon which the elements of a hybrid microcircuit are deposited or attached or within which the elements of an integrated circuit are fabricated.

SUBSYSTEM: A smaller part of an electronic system which performs a part of the system function but can be removed intact and tested separately.

SUBSTRACTIVF PROCESS: The process of selectively removing unwanted portions of a conductive layer using an etching proccss.

SUPERCONDUCTIVITY: The phenomenon of almost no electrical resistance in materials when their temperatures are reduced.

SURFACE CONDUCTANCE: Conductance of electrons along the outer surface of a conductor.

SURFACE INFUSION: The high temperature injection of atoms into the surface layer of a semiconductor material to form the junctions. Usually, a gaseous diffusion process.

SURFACE FINISH: The peaks and valleys in the surface of a substrate rated in μm/mm deviation.

SURFACE MOUNTING: The interconnection of components to the top conductive layer of a printed board or metallized ceramic substrate without the use of through holes.

SURFACE NUCLEATION: The change in phase or state of the surface on a substrate. Applicable to the beginning of formation of evaporated thin-film.

SURFACE RESISTIVITY: The resistance to a current flow along the surface of an insulator material.

SURFACE TENSION: An effect of the forces of attraction existing between the molecules of a liquid. It exists only on the boundary surface.

SURFACE TEXTURE: The smoothness or lack of it on the surface of a substrate.

SURFACTANT: A contraction for the term "surface-active agent."

SWAGED LEADS: Component leads

which are mechanically flattened or swaged to the printed board or ceramic substrate during the manufacturing process.

SWIMMING: Lateral shifting of a thick-film conductive pattern while on molten glass, for example, upon reheating.

SYSTEM: A product which for most considerations is repairable. Examples include computers, radars, and power supplies.

T

TACKY STATE: A material is in a tacky state when it exhibits an adhesive bond to another surface.

TAIL (OF THE BOND): The free end of wire extending beyond the bond impression of a wire bond from the heel.

TAIL PULL: The act of removing the excess wire left when a wedge of ultrasonic bond is made.

TANTALUM CAPACITOR: Capacitors that utilize a thin tantalum oxide layer as the dielectric material.

TAPE ALUMINA: Alumina (substrates) made by tape casting of slurry into strips of green alumina of a predetermined thickness. This is followed by stamping, cutting in the green state, then firing.

TAPE AUTOMATED BONDING (TAB): The utilization of a metal or plastic tape material as a support and carrier of a microelectronic component in a gang bonding process.

TAPED COMPONENTS: Components that are attached to a tape material forming a continuous roll for use in automatic insertion or placement machines.

TARNISH: Chemical accretions on the surface of metals, such as sulfides and oxides. Fluxes have to remove tarnish in order to allow wetting by solder.

TEAR STRENGTH: Measurement of the amount of force needed to tear a solid material that has been nicked on one edge and then subjected to a pulling stress. Measured in g/cm.

TEMPERATURE AGING: Aging or stressing of a film circuit in an elevated temperature over a period of time.

TEMPERATURE COEFFICIENT OF CAPACITANCE (TCC): The amount of capacitance change of a capacitor with temperature, commonly expressed as the average change over a certain temperature range in ppm/°C.

TEMPERATURE COEFFICIENT OF RESISTANCE (TCR): The amount of resistance change of a resistor (or resistor material) with temperature, commonly expressed as the average change over a certain temperature range in ppm/°C.

TEMPERATURE CYCLING: An environmental test in which the film circuit is subjected to several temperature changes from a low temperature to a high temperature over a period of time.

TEMPERATURE EXCURSION: The extreme temperature difference seen by a film circuit under operating conditions.

TEMPERATURE TRACKING: The ability of a component to retrace its electrical readings going up and down the temperature scale.

TEMPERING: A method of heating a material followed by rapid cooling.

TENSILE STRENGTH: The pulling stress which has to be applied to a material to break it, usually measured in Pa.

TENTING: The manufacturing process for covering the surface of the printed

board, usually with a dry film resist.

TERMINAL: A metal lead used to provide electrical access to the inside of the device package. A metallic part used for electrical interconnection.

TEST BOARD: A printed board that is manufactured using the same process that will be used for production quantities of product to ensure product acceptability.

TEST COUPON: A portion of the quality control test area used for acceptance tests or other related tests.

TEST PATTERN: A circuit or group of substrate elements processed on or within a substrate to act as a test site or sites for element evaluation or monitoring of fabrication processes. A pattern used for testing and/or inspection.

TEST POINT: A point used for access to the electrical circuit for testing purposes.

THERMAL CONDUCTIVITY: The amount of heat per unit time per unit area that can be conducted through a unit thickness of a material at a difference in temperature.

THERMAL DESIGN: The schematic heat flow path for power dissipation from within a film circuit to a heat sink.

THERMAL DRIFT: The drift of circuit elements from nominal value due to changes in temperature.

THERMAL DROP: The difference in temperature across a boundary or across a material.

THERMAL GRADIENT: The plot of temperature variances across the surface or the bulk thickness of a material being heated.

THERMAL MISMATCH: Difference of thermal coefficients of expansion of materials which are bonded together.

THERMAL NOISE: Noise that is generated by the random thermal motion of charged particles in an electronic device.

THERMAL RELIEF: Crosshatching used to minimize warping and/or blistering during the soldering process.

THERMAL RUNAWAY: A condition wherein the heat generated by a device causes an increase in heat generated. This spiraling rise in dissipation usually continues until a temperature is reached that results in destruction of the device.

THERMAL SHIFT: The permanent shift in the nominal value of a circuit element due to heating effect.

THERMAL SHOCK: A condition whereby devices are subjected alternately to extreme heat and extreme cold. Used to screen out processing defects.

THERMOCOMPRESSION BONDING: A process involving the use of pressure and temperature to join two materials by interdiffusion across the boundary.

THERMOCOUPLE: A temperature sensor formed by joining two dissimilar metals and applying a temperature differential between the measuring junction and the reference junction.

THERMOPLASTIC: A substance that becomes plastic (malleable) on being heated; a plastic material that can be repeatedly melted or softened by heat without change or properties.

THERMOSONIC BONDING: A bonding process which uses a combination of thermocompression (TC) bonding and ultrasonic bonding. It is done on what

amounts to a gold-wire TC bonder with ultrasonic power applied to the capillary. Thus, the bond (weld) is made with temperature, metal squashing, and ultrasonic scrubbing action.

THERMOSWAGING: Heating a pin that is inserted in a hole and upsetting the hot metal so that it swells and fills the hole, thereby forming a tight bond with the base material.

THICK-FILM: A film deposited by screen printing processes and fired at high temperature to fuse into its final form. The basic processes of thick-film technology are screen printing and firing.

THICK-FILM CIRCUIT: A microcircuit in which passive components of a ceramic-metal composition are formed on a suitable substrate by screening and firing.

THICK-FILM HYBRID CIRCUIT: A hybrid microcircuit that has add-on components, usually chip devices added to a thick-film network to perform an electronic function.

THICK-FILM NETWORK: A network of thick-film resistors and/or capacitors, or inductors interconnected with thick-film conductors on a ceramic substrate, formed by screening and firing.

THICK-FILM TECHNOLOGY: The technology whereby electrical networks or elements are formed by applying a liquid, solid, or paste coating through a screen or mask in a selective pattern onto a supporting material (substrate) and fired. Films so formed are usually 5 μm or greater in thickness.

THIN-FILM: A thin-film (usually less than 5 μm thickness) is one that is deposited onto a substrate by an accretion process such as vacuum evaporation, sputtering, chemical vapor deposition, or pyrolytic decomposition.

THIN-FILM HYBRID CIRCUIT: A hybrid microcircuit that has add-on components, usually chip devices added to a thin-film network to perform an electronic function.

THIN-FILM INTEGRATED CIRCUIT: A functioning circuit made entirely of thin-film components. Also used to mean thin-film hybrid circuit.

THIN-FILM NETWORK: A resistor and/or capacitor and conductor network formed on a single substrate by vacuum evaporation and sputtering techniques.

THIN-FILM TECHNOLOGY: The technology whereby electronic networks or elements are formed by vacuum evaporation or sputtering films onto a supporting material (substrate). Films so formed are less than 5μm and usually of the order 0.3μm to 1.0 μm in thickness.

THIN FOIL: Metal sheet stock less than 0.0007 inches thick.

THIXOTROPIC: A fluid that gets less viscous as it is stirred (or moved). The term is sometimes applied to these fluids (e.g., most thick-film inks).

THROUGH CONNECTION: An electrical connection between different conductive layers.

THROWAWAY MODULE: A functional circuit in a modular form factor that is considered expendable and will not be repaired because of its low cost.

TINNED: Literally, coated with tin, but commonly used to indicate coated with

solder.

TINNING: To coat metallic surfaces with a thin layer of solder.

TIP: That portion of the bonding tool which deforms the wire to cause the bond impression.

T.I.R: An abreviation for "Total indicated reading", the total amont of variation, both positive and negative, from the correct dimension.

TO PACKAGE: Abbreviation for transistor outline, established as an industry standard by JEDEC of the EIA.

TOE: See tail (of the bond).

TOOLING FEATURE: A specific feature on a printed board or panel that facilitates alignment during the manufacturing process.

TOP-HAT RESISTORS: Film resistors having a projection out one side allowing a notch to be cut into the center of the projection to form a serpentine resistor and thereby increase the resistivity.

TOPOGRAPHY: The surface condition of a film—bumps, craters, etc.

TOPOLOGY: The surface layout design study and characterization of a microcircuit. It has application chiefy in the preparation of the artwork for the layout masks used in fabrication.

TOROIDS: A helical winding on a ring-shaped core (doughnut-shaped coil). A popular form used for inductors.

TORQUE TEST: A test for determining the amount of torque required to twist off a lead or terminal.

TRACKING: Two similar elements on the same circuit that change values with temperature in close harmony are said to track well. Tracking of different resistors is measured in ppm/°C (difference). Tracking is also used in reference to temperature hysteresis performance and potentiometer repeatability.

TRANSDUCER: A device actuated by one transmission system and supplying related energy to another transmission system.

TRANSFER MOLDING: Molding circuit modules by transferring molten piastic into a cavity holding the circuit by using a press.

TRANSFER SOLDERING: A hand soldering process using ball, chip, or disk solder preforms.

TRANSMISSION CABLE: Two or more transmission lines forming either a flat cable or a round structure.

TRANSMISSION LINE: A signal carrying line with controlled electrical characteristics used to transmit high-frequency, or narrow-pulse signals.

TRAPEZOIDAL DISTORTION: Distortion that can occur during photoreduction. As a result, a square shape in the original master will be transformed into a trapezoid at the reduced position.

TREATMENT TRANSFER: The transfer of copper foil treatment to the base material which is characterized by black, brown, or red steaks after the copper has been removed.

TRIM NOTCH: The notch made in a resistor by trimming to obtain the design value (see kerf).

TRIMMING: Notching a resistor by abrasive or laser means to raise the nominal resistance value.

TRUE POSITION: The theoretical location of a hole or feature defined by ba-

sic dimension.

TRUE POSITION TOLERANCE: The movement around the true position defined by a diameter and called out on the master drawing.

TWIST: A deformation of a rectangular sheet characterized by one corner being out of a plane defined by the other three corners.

U

ULTRASONIC BONDING: A process involving the use of ultrasonic energy and pressure to join two materials.

ULTRASONIC CLEANING: A method of cleaning that uses cavitation in fluids caused by applying ultrasonic vibrations to the fluid.

ULTRASONIC POWER SUPPLY: An electronic high-frequency generator that provides ultrasonic power to a transducer.

UNCASED DEVICE: A chip device.

UNDERBONDING: In wire bonding, insufficient deforming the wire with the bonding tool during the bonding process.

UNDERCUT: The distance from the outermost base conductor edge, excluding any additional cover plating, to the innermost point at the conductor-base material interface.

UNDERDEFORMING: Insufficient deforming of the wire by the bonding tool occurring during the bonding operation.

UNDERGLAZE: A glass or ceramic glaze applied to a substrate prior to the screening and firing of a resistor.

UNIVERSAL LEAD FRAME: Lead frame in which flag is not supported by any lead.

UNSUPPORTED HOLE: A hole that is not supported by any type of reinforcement.

USEFUL LIFE: The length of time a product functions with a failure rate which is considered to be satisfactory.

V

VACUUM BAKEOUT: Bakeout of hybrid devices just prior to cover sealing. Its purpose is to drive out all moisture before package closure, thereby inhancing high reliability. Hybrids, or other devices, are processed in a vacuum chamber at a preset temperature (about 150°C), then are transfered directly to the interior of the cover-sealing machine under inert atmosphere, without having been exposed to room air.

VACUUM DEPOSITION: Deposition of a metal film onto a substrate in a vacuum by evaporation or sputtering techniques.

VACUUM PICKUP: A handling instrument with a small vacuum cup on one end used to pick up chip devices.

VAPOR DEPOSITION (VAPOR EVAPORATION): Same as vacuum deposition.

VAPOR PHASE: The state of a compound when it is in the form of a vapor.

VAPOR PRESSURE: The pressure exerted by a vapor in equilibrium with the liquid phase of the same material.

VARNISH: A protective coating for a circuit to protect the elements from environmental damage.

VEHICLE: A thick-film term that refers to the organic system in the paste.

VIA: An opening in the dielectric layer(s) through which a riser passes, or else whose walls are made conductive.

VIA HOLE: A plated through hole providing electrical interconnection for two or more conductive layers but not intended to have a component lead inserted through it.

VINTAGE CONTROL NUMBER: An alphanumeric code related to changes made on manufactured products. The vintage control code generally follows the time part number.

VISCOSIMETER (VISCOMETER: A device that measures viscosity. Viscometers for thick-film compositions must be capable of measuring viscosity under conditions of varying shear rates.

VISCOSITY: A term used to describe the fluidity of material, or the rate of flow versus pressure. The unit of viscosity measurement is poise, more commonly centipoise. Viscosity varies inversely with temperature.

VISCOSITY COEFFICIENT: The coefficient of viscosity is the value of the tangential force per unit area which is necessary to maintain unit relative velocity between two parallel planes a unit distance apart.

VISUAL EXAMINATION: Qualitative ex- amination of physical characteristics using the unaided eye or defined levels of magnification.

VITREOUS: Having the nature of glass.

VITREOUS BINDER: A glassy material used in a compound to bind other particles together. This takes place after melting the glass and cooling.

VITRIFICATION: The progressive reduction in porosity of a ceramic material as a result of heat treatment or some other process.

VOID: In visual inspection of solid materials, a space not filled with the specific solid material, such as a gap or opening which is an unintentional defect in the material. In power hybrid, trapped air, flux or foreign material in solder interface between die and substrate, between substrate and case.

VOLTAGE GRADIENT: The voltage drop (or change) per unit length along a resistor or other conductance path.

VOLTAGE PLANE: A conductor layer in a printed board that is held at a some specified voltage; it may also be used for shielding or heat sinking.

VOLTAGE RATING: The maximum voltage which an electronic circuit can sustain to ensure long life and reliable operation.

VOLUME RESISTIVITY: The resistance of a material to an applied electrical voltage as a function of the configuration of the material.

W

WAFER: A slice of semiconductor crystal ingot used as a substrate for transistors, diodes, and monolithic integrated circuits.

WAFFLE PACK: Also known as a "dry pack", it is a small flat, square container divided into rows of cavities and supplemented by a tight fitting lid, held in place by clamps. The cavities are of suitable sizes, all uniform for a given waffle pack, each one to cradle an individual die. The dice are shipped, inspected, handled, and stored while in waffle packs.

WARP AND WOOF: Threads in a woven screen which cross each other at right angles.

WARPAGE: The distortion of a substrate or case bottom from a flat plane.

WEDGE BOND: A bond made with a wedge tool. The term is usually used to differentiate thermocompression wedge bonds from other thermocompression bonds. (Almost all ultrasonic bonds are

wedge bonds.)

WEDGE TOOL: A bonding tool in the general form of a wedge with or without a wire-guide hole to position the wire under the bonding face of the tool, as opposed to a capillary-type tool.

WETTING: The spreading of molten solder on a metallic surface, with proper application of heat and flux.

WHISKERS: Needle-shaped metallic growths between conductors.

WICKING: The flow of solder along the strands and under the insulation of stranded lead wires.

WIRE BOND: A completed wire connection which includes all its constituents providing electrical continuity between the semiconductor die (pad) and a terminal. These constituents are the fine wire; metal bonding surfaces like die pad and package land; metallurgical interfaces underneath the bonded-wire deformation; underlying insulating layer (if present); and substrate.

WIRE BONDING: The method used to attach very fine wire to semiconductor components to interconnect these components with each other or with package leads, or with conductors.

WIRE CLAMP: A device designed to hold the wire during the cutoff operation.

WIRE LEAD: A length of uninsulated solid or twisted wire which may be formed to make an electrical interconnection.

WIRE SPOOL: The wire magazine.

WOBBLE BOND: A thermocompression, multicontact bond accomplished by rocking (or wobbling) a bonding tool on the beams of a beam lead device.

WORST-CASE ANALYSIS: The analysis of a circuit function under tolerance extremes of temperature, humidity, etc. to determine the worst possible effect on the performance parameters.

WOVEN SCREEN: A screen mesh used for screen printing, usually made of nylon, or stainless steel, or possible silk.

Y

YIELD: The ratio of usable components at the end of a manufacturing process to the number of components initially submitted for processing. Can be applied to any input-output stage in processing, and so must be carefully defined and understood.

YIELD STRENGTH: Strength at a point at which the strain begins to increase very rapidly without a corresponding increase in stress.

Z

ZIF CONNECTOR: A connector used for electrical interconnection to a printed board or mating connector half that requires zero insertion force (ZIF).

ZIF SOCKET: A socket used to interconnect a component to a printed board that does not require any solder and is characterized by zero insertion force.

Appendix B—
Unit Conversion Tables

Table B-1: The Greek alphabet

Name	Large	Small	Name	Large	Small	Name	Large	Small
Alpha	A	α	Iota	I	ι	Rho	P	ρ
Beta	B	β	Kappa	K	κ	Sigma	Σ	σ
Gamma	Γ	γ	Lambda	Λ	λ	Tau	T	τ
Delta	Δ	δ	Mu	M	μ	Upsilon	Y	υ
Epsilon	E	ε	Nu	N	ν	Phi	Φ	ϕ
Zeta	Z	ζ	Xi	Ξ	ξ	Chi	X	χ
Eta	H	η	Omicron	O	o	Psi	Ψ	ψ
Theta	Θ	θ	Pi	Π	π	Omega	Ω	ω

Table B-2: Unit prefixes

Multiples	Submultiples
10^{12} = tera = T	10^{-1} = deci = d
10^{9} = giga = G	10^{-2} = centi = c
10^{6} = mega = M	10^{-3} = milli = m
10^{3} = kilo = k	10^{-6} = micro = μ
10 = hecto = h	10^{-9} = nano = n
10 = deca = da	10^{-12} = pico = p
	10^{-15} = femto = f
	10^{-18} = atto = a

Table B-3: Length

Units	Centimeter	Meter	Inch	Foot
1 centimeter	1	10^{-2}	0.3937	3.281×10^{-2}
1 meter	100	1	39.37	3.281
1 inch	2.540	2.540×10^{-2}	1	8.333×10^{-2}
1 foot	30.48	30.48×10^{-2}	12	1

Table B-4: Area

Units	cm^2	m^2	in^2	ft^2	circular mil
cm^2	1	10^{-4}	0.155	1.076×10^{-3}	1.974×10^{5}
m^2	10^{4}	1	1550	10.76	1.974×10^{9}
in^2	6.452	6.452×10^{-4}	1	6.944×10^{-3}	1.273×10^{6}
ft^2	929.0	9.290×10^{-2}	144	1	1.833×10^{8}
circular mil	5.067×10^{-6}	5.067×10^{-10}	7.854×10^{-7}	5.454×10^{-9}	1

Table B-5: Density

Units	$gram/cm^3$	kg/m^3	lb/in^3	lb/ft^3
$gram/cm^3$	1	10^{3}	3.613×10^{-2}	62.43
kg/m^3	10^{-3}	1	3.613×10^{-5}	6.243×10^{-2}
lb/in^3	27.68	2.768×104	1	1728
lb/ft^3	1.602×10^{-2}	16.02	5.787×10^{-4}	1

Table B-6: Electrical resistivity

Units	ohm-m	ohm-cm	μohm-cm	statohm-cm	ohm-circ mil/ft
ohm-m	1	100	108	1.113×10^{-10}	6.015×10^{8}
ohm-cm	0.01	1	106	1.113×10^{-12}	6.015×10^{6}
mohm-cm	10^{-8}	10^{-6}	1	1.113×10^{-18}	6.015
statohm-cm	8.987×10^{9}	8.987×10^{11}	8.987×10^{17}	1	5.406×10^{18}
ohm-circ mil/ft	1.662×10^{-9}	1.662×10^{-7}	0.1662	1.850×10^{-19}	1

Table B-7: Thermal conductivity

Units	Multiplier			
	$m/cal/cm^2sec°C/cm$	$Watts/cm^2°C/cm$	$Watts/in^2°C/in$	$Btu/ft^2hr°F/ft$
$Btu/ft^2hr°F/in$	2902.758	693.481	273.0	12.005
$Kgcal/m^2hr°C/m$	360.0	85.985	33.86	1.4881
$Btu/ft^2hr°F/ft$	241.897	57.803	22.75	1.0
$Watts/in^2°C/in$	10.6326	2.540	1.0	0.04396
$Watts/cm^2°C/cm$	4.1859	1.0	0.3937	0.01730
$m/cal/cm^2sec°C/cm$	1.0	0.2389	0.09405	4.134×10^{-3}

Table B-8: Mass

Units	Grams	Kilograms	Ounces (avoir.)	Pounds (avoir.)	Ounces (troy)
Grams	1	0.001	3.527×10^{-2}	2.205×10^{-3}	3.215×10^{-2}
Kilograms	1000	1	35.274	2.2046	32.151
Ounces (avoir.)	28.350	0.028350	1	0.0625	0.91146
Pounds (avoir.)	453.59	0.45359	16.0	1	14.583
Ounces (troy)	31.103	0.03110	1.0971	0.068571	1
Pounds (troy)	373.24	0.37324	13.166	0.82286	12
Grains	0.06480	6.480×10^{-5}	2.286×10^{-3}	1.429×10^{-4}	2.083×10^{-3}
Drams (troy)	3.8879	3.888×10^{-3}	0.13714	8.571×10^{-3}	0.1250

Table B-9: Power

Units	Watts	ft-lb/sec	g-cm/sec	kg-cal/min	HP
Watts	1	0.73756	1.0197×10^{4}	0.01433	1.341×10^{-3}
ft-lb/sec	1.35582	1	1.3826×10^{4}	0.019433	$1.8182 \times 10^{-}$
g-cm/sec	9.8067×10^{-5}	7.2330×10^{-5}	1	1.4056×10^{-6}	$1.3151 \times 10^{-}$
kg-cal/min	69767	51.457	7.1146×10^{5}	1	0.093557
Horsepower (US)	745.7	550	7.6042×10^{6}	10.688	1
Lumens	1.496×10^{-3}	1.0034×10^{-3}	15.254	2.1437×10^{-5}	$2.0061 \times 10^{-}$
Joules/sec	1	0.73756	1.0197×10^{4}	0.01433	1.341×10^{-3}
BTU/hr	0.29299	0.21610	2.9878×10^{3}	4.1997×10^{-3}	$3.9291 \times 10^{-}$

Table B-10: Work and energy

Units	g-cal	Joules	BTU	ft-lb	kg-meters
g.cal.	1	4.186	3.9680×10^{-3}	3.0874	0.42685
Joules	0.23889	1	9.4805×10^{-4}	0.73756	0.10197
BTU	251.98	1054.8	1	777.98	107.56
ft-lb	0.32389	1.3558	1.2854×10^{-3}	1	0.13825
kg-meters	2.3427	9.8066	9.2967×10^{-3}	7.2330	1
L-Atm	24.206	101.328	0.09606	74.735	10.333
HP-hours	6.4130×10^{5}	2.6845×10^{6}	2454	1.9800×10^{6}	2.737×10^{5}
Watt-hours	860.01	3600	3.4130	2655.3	367.09

Table B-11: Pressure

Units	Atm	Bar	in of Hg	mm of Hg (torr)	kg/m^2	lb/in^2 (psi)	Pascal
Atm	1	0.986923	0.0334207	1.316×10^{-3}	9.6780×10^{-5}	0.068046	$9.8690 \times 10^{-}$
Bar	1.01325	1	$3.3864_2 \times 10^{-}$	1.3330×10^{-3}	9.8067×10^{-5}	0.068948	10^{-5}
in of Hg	29.9213	29.53	1	3.9370×10^{-2}	2.8960×10^{-3}	2.036	$2.9530 \times 10^{-}$
mm of Hg (torr)	760	750.06	25.400	1	7.3558×10^{-2}	51.715	$7.5020 \times 10^{-}$
kg/m^2	1.033227×10^4	1.0197×10^4	345.3	13.59	1	703.06	0.1019
lb/in^2 (psi)	14.695595	14.504	0.4912	1.9340×10^{-2}	1.4230×10^{-3}	1	$1.4500 \times 10^{-}$
Pascal	1.01325	1×10^5	3.386×10^3	1.333×10^2	9.8067	6894.8	1

Table B-12: Atmospheric pressure

	Pressure			
Altitude (feet)	inches of Hg	mm of Hg (torr)	Lb/in^2, (psi)	Pascals ($\times 10^3$)
-1,000	31.02	787.9	15.25	105.15
-500	30.47	773.8	14.94	103.01
0	29.921	760.0	14.70	101.35
500	29.38	746.4	14.43	99.49
1,000	28.86	732.9	14.18	97.77
1,500	28.33	719.7	13.90	95.84
2,000	27.82	706.6	13.67	94.25
2,500	27.31	693.8	13.41	92.46
3,000	26.81	681.1	13.19	90.94
3,500	26.32	668.6	12.92	89.08
4,000	25.84	656.3	12.70	87.56
4,500	25.36	644.2	12.45	85.84
5,000	24.89	632.3	12.23	84.32
10,000	20.58	522.6	10.10	69.64
15,000	16.88	428.8	8.28	57.09
20,000	13.75	349.1	6.75	46.54
30,000	8.88	225.6	4.36	30.06
40,000	5.54	140.7	2.72	18.75
50,000	3.426	87.30	1.689	11.65
60,000	2.132	54.15	1.048	7.226

70,000	1.322	33.59	0.649	4.475
80,000	0.820	20.83	0.403	2.779

Table B-13: Wire table – comparison of gauges

British Standard (NBS) wire gauge			American (B&S) wire gauge		
Diameter		Gauge number	Diameter		Electrical resistance o annealed copper
inches	mm		inches	mm	Ω per 1000 ft at 20°C
0.324	8.23	**0**	0.3249	8.25	0.09827
0.300	7.62	**1**	0.2893	7.35	0.1239
0.276	7.01	**2**	0.2576	6.54	0.1563
0.252	6.40	**3**	0.2294	5.83	0.1970
0.232	5.89	**4**	0.2043	5.19	0.2485
0.212	5.38	**5**	0.1819	4.62	0.3133
0.192	4.88	**6**	0.1620	4.11	0.3951
0.176	4.47	**7**	0.1443	3.67	0.4982
0.160	4.06	**8**	0.1285	3.26	0.6282
0.144	3.66	**9**	0.1144	2.91	0.7921
0.128	3.25	**10**	0.1019	2.59	0.9989
0.116	2.95	**11**	0.0907	2.30	1.260
0.104	2.64	**12**	0.0808	2.05	1.588
0.092	2.34	**13**	0.0720	1.83	2.003
0.080	2.03	**14**	0.0641	1.63	2.525
0.072	1.83	**15**	0.0571	1.45	3.184
0.064	1.63	**16**	0.0508	1.29	4.016
0.056	1.42	**17**	0.0453	1.15	5.064
0.048	1.22	**18**	0.0403	1.02	6.385
0.040	1.02	**19**	0.0359	0.912	8.051
0.036	0.914	**20**	0.0320	0.813	10.15
0.032	0.813	**21**	0.0285	0.724	12.80
0.028	0.711	**22**	0.0253	0.643	16.14
0.024	0.610	**23**	0.0226	0.574	20.36
0.022	0.559	**24**	0.0201	0.511	25.67
0.020	0.508	**25**	0.0179	0.455	32.37
0.0180	0.457	**26**	0.0159	0.404	40.81
0.0164	0.417	**27**	0.0142	0.361	51.47
0.0148	0.376	**28**	0.0126	0.320	64.90
0.0136	0.345	**29**	0.0113	0.287	81.83

0.0124	0.315	**30**	0.0100	0.254	103.2
0.0116	0.295	**31**	0.0089	0.226	130.1
0.0108	0.274	**32**	0.0080	0.203	164.1
0.0100	0.254	**33**	0.0071	0.180	206.9
0.0092	0.234	**34**	0.0063	0.160	260.9
0.0084	0.213	**35**	0.0056	0.142	329.0
0.0076	0.193	**36**	0.0050	0.127	414.8
0.0068	0.173	**37**	0.0045	0.114	523.1
0.0060	0.152	**38**	0.0040	0.102	659.6
0.0052	0.132	**39**	0.0035	0.089	831.8
0.0048	0.122	**40**	0.0031	0.079	1049.0
0.0044	0.112	**41**	0.0028	0.071	1320
0.0040	0.102	**42**	0.0025	0.064	1660
0.0036	0.091	**43**	0.0022	0.056	2140
0.0032	0.081	**44**	0.0020	0.051	2590
0.0028	0.071	**45**	0.0018	0.046	3620

Table B-14: Temperature conversion

°C	Ref.	°F	°C	Ref.	°F	°C	Ref.	°F	°C	Ref.	°F
-17.8	**0**	32	199	**390**	734	921	**1690**	3074	1643	**2990**	5414
-17.2	**1**	33.8	204	**400**	752	927	**1700**	3092	1649	**3000**	5432
-16.7	**2**	35.6	210	**410**	770	932	**1710**	3110	1654	**3010**	5450
-16.1	**3**	37.4	216	**420**	788	938	**1720**	3128	1660	**3020**	5468
-15.6	**4**	39.2	221	**430**	806	943	**1730**	3146	1666	**3030**	5486
-15.0	**5**	41.0	227	**440**	824	949	**1740**	3164	1671	**3040**	5504
-14.4	**6**	42.8	232	**450**	842	954	**1750**	3182	1677	**3050**	5522
-13.9	**7**	44.6	238	**460**	860	960	**1760**	3200	1682	**3060**	5540
-13.3	**8**	46.4	243	**470**	878	966	**1770**	3218	1688	**3070**	5558
-12.8	**9**	48.2	249	**480**	896	971	**1780**	3236	1693	**3080**	5576
-12.2	**10**	50.0	254	**490**	914	977	**1790**	3254	1699	**3090**	5594
-11.7	**11**	51.8	260	**500**	932	982	**1800**	3272	1704	**3100**	5612
-11.1	**12**	53.6	266	**510**	950	988	**1810**	3290	1710	**3110**	5630
-10.6	**13**	55.4	271	**520**	968	993	**1820**	3308	1716	**3120**	5648
-10	**14**	57.2	277	**530**	986	999	**1830**	3326	1721	**3130**	5666
-9.44	**15**	59.0	282	**540**	1004	1004	**1840**	3344	1727	**3140**	5684
-8.89	**16**	60.8	288	**550**	1022	1010	**1850**	3362	1732	**3150**	5702
-8.33	**17**	62.6	293	**560**	1040	1016	**1860**	3380	1738	**3160**	5720
-7.78	**18**	64.4	299	**570**	1058	1021	**1870**	3398	1743	**3170**	5738
-7.22	**19**	66.2	304	**580**	1076	1027	**1880**	3416	1749	**3180**	5756
-6.67	**20**	68.0	310	**590**	1094	1032	**1890**	3434	1754	**3190**	5774
-6.11	**21**	69.8	316	**600**	1112	1038	**1900**	3452	1760	**3200**	5792
-5.56	**22**	71.6	321	**610**	1130	1043	**1910**	3470	1766	**3210**	5810
-5.0	**23**	73.4	327	**620**	1148	1049	**1920**	3488	1771	**3220**	5828
-4.44	**24**	75.2	332	**630**	1166	1054	**1930**	3506	1777	**3230**	5846
-3.89	**25**	77.0	338	**640**	1184	1060	**1940**	3524	1782	**3240**	5864
-3.33	**26**	78.8	343	**650**	1202	1066	**1950**	3542	1788	**3250**	5882
-2.78	**27**	80.6	349	**660**	1220	1071	**1960**	3560	1793	**3260**	5900
-2.22	**28**	82.4	354	**670**	1238	1077	**1970**	3578	1799	**3270**	5918
-1.67	**29**	84.2	360	**680**	1256	1082	**1980**	3596	1804	**3280**	5936

-1.11	**30**	86.0	366	**690**	1274	1088	**1990**	3614	1810	**3290**	5954
-0.56	**31**	87.8	371	**700**	1292	1093	**2000**	3632	1816	**3300**	5972
0	**32**	89.6	377	**710**	1310	1099	**2010**	3650	1821	**3310**	5990
0.56	**33**	91.4	382	**720**	1328	1104	**2020**	3668	1827	**3320**	6008
1.11	**34**	93.2	388	**730**	1346	1110	**2030**	3686	1832	**3330**	6026
1.67	**35**	95.0	393	**740**	1364	1116	**2040**	3704	1838	**3340**	6044
2.22	**36**	96.8	399	**750**	1382	1121	**2050**	3722	1843	**3350**	6062
2.78	**37**	98.6	404	**760**	1400	1127	**2060**	3740	1849	**3360**	6080
3.33	**38**	100.4	410	**770**	1418	1132	**2070**	3758	1854	**3370**	6098

(table continued on next page)

Table B-14: (Continued)

°C	Ref.	°F	°C	Ref.	°F	°C	Ref.	°F	°C	Ref.	°F
3.89	**39**	102.2	416	**780**	1436	1138	**2080**	3776	1860	**3380**	6116
4.44	**40**	104	421	**790**	1454	1143	**2090**	3794	1866	**3390**	6134
5.0	**41**	105.8	427	**800**	1472	1149	**2100**	3812	1871	**3400**	6152
5.56	**42**	107.6	432	**810**	1490	1154	**2110**	3830	1877	**3410**	6170
6.11	**43**	109.4	438	**820**	1508	1160	**2120**	3848	1882	**3420**	6188
6.67	**44**	111.2	443	**830**	1526	1166	**2130**	3866	1888	**3430**	6206
7.22	**45**	113.0	449	**840**	1544	1171	**2140**	3884	1893	**3440**	6224
7.78	**46**	114.8	454	**850**	1562	1177	**2150**	3902	1899	**3450**	6242
8.33	**47**	116.6	460	**860**	1580	1182	**2160**	3920	1904	**3460**	6260
8.89	**48**	118.4	466	**870**	1598	1188	**2170**	3938	1910	**3470**	6278
9.44	**49**	120.2	471	**880**	1616	1193	**2180**	3956	1916	**3480**	6296
10.0	**50**	122.0	477	**890**	1634	1199	**2190**	3974	1921	**3490**	6314
10.6	**51**	123.8	482	**900**	1652	1204	**2200**	3992	1927	**3500**	6332
11.1	**52**	125.6	488	**910**	1670	1210	**2210**	4010	1932	**3510**	6350
11.7	**53**	127.4	493	**920**	1688	1216	**2220**	4028	1938	**3520**	6368
12.2	**54**	129.2	499	**930**	1706	1221	**2230**	4046	1943	**3530**	6386
12.8	**55**	131.0	504	**940**	1724	1227	**2240**	4064	1949	**3540**	6404
13.3	**56**	132.8	510	**950**	1742	1232	**2250**	4082	1954	**3550**	6422
13.9	**57**	134.6	516	**960**	1760	1238	**2260**	4100	1960	**3560**	6440
14.4	**58**	136.4	521	**970**	1778	1243	**2270**	4118	1966	**3570**	6458
15.0	**59**	138.2	527	**980**	1796	1249	**2280**	4136	1971	**3580**	6476
15.6	**60**	140.0	532	**990**	1814	1254	**2290**	4154	1977	**3590**	6494
16.1	**61**	141.8	538	**1000**	1832	1260	**2300**	4172	1982	**3600**	6512
16.7	**62**	143.6	543	**1010**	1850	1266	**2310**	4190	1988	**3610**	6530
17.2	**63**	145.4	549	**1020**	1868	1271	**2320**	4208	1993	**3620**	6458
17.8	**64**	147.2	554	**1030**	1886	1277	**2330**	4226	1999	**3630**	6566
18.3	**65**	149.0	560	**1040**	1904	1282	**2340**	4244	2004	**3640**	6584
18.9	**66**	150.8	566	**1050**	1922	1288	**2350**	4262	2010	**3650**	6602
19.4	**67**	152.6	571	**1060**	1940	1293	**2360**	4280	2016	**3660**	6620
20.0	**68**	154.4	577	**1070**	1958	1299	**2370**	4298	2021	**3670**	6638

20.6	**69**	156.2	582	**1080**	1976	1304	**2380**	4316	2027	**3680**	6656
21.1	**70**	158.0	588	**1090**	1994	1310	**2390**	4334	2032	**3690**	6674
21.7	**71**	159.8	593	**1100**	2012	1316	**2400**	4352	2038	**3700**	6692
22.2	**72**	161.6	599	**1110**	2030	1321	**2410**	4370	2043	**3710**	6710
22.8	**73**	163.4	604	**1120**	2048	1327	**2420**	4388	2049	**3720**	6728
23.3	**74**	165.2	610	**1130**	2066	1332	**2430**	4406	2054	**3730**	6746
23.9	**75**	167.0	616	**1140**	2084	1338	**2440**	4424	2060	**3740**	6764
24.4	**76**	168.8	621	**1150**	2102	1343	**2450**	4442	2066	**3750**	6782
25.0	**77**	170.6	627	**1160**	2120	1349	**2460**	4460	2071	**3760**	6800

(table continued on next page)

Table B-14: (Continued)

°C	Ref.	°F	°C	Ref.	°F	°C	Ref.	°F	°C	Ref.	°F
25.6	**78**	172.4	632	**1170**	2138	1354	**2470**	4478	2077	**3770**	6818
26.1	**79**	174.2	638	**1180**	2156	1360	**2480**	4496	2082	**3780**	6836
26.7	**80**	176.0	643	**1190**	2174	1366	**2490**	4514	2088	**3790**	6854
27.2	**81**	177.8	649	**1200**	2192	1371	**2500**	4532	2093	**3800**	6872
27.8	**82**	179.6	654	**1210**	2210	1377	**2510**	4550	2099	**3810**	6890
28.3	**83**	181.4	660	**1220**	2228	1382	**2520**	4568	2104	**3820**	6908
28.9	**84**	183.2	666	**1230**	2246	1388	**2530**	4586	2110	**3830**	6926
29.4	**85**	185.0	671	**1240**	2264	1393	**2540**	4604	2116	**3840**	6944
30.0	**86**	186.8	677	**1250**	2282	1399	**2550**	4622	2121	**3850**	6962
30.6	**87**	188.6	682	**1260**	2300	1404	**2560**	4640	2127	**3860**	6980
31.1	**88**	190.4	688	**1270**	2318	1410	**2570**	4658	2132	**3870**	6998
31.7	**89**	192.2	693	**1280**	2336	1416	**2580**	4676	2138	**3880**	7016
32.2	**90**	194.0	699	**1290**	2354	1421	**2590**	4694	2143	**3890**	7034
32.8	**91**	195.8	704	**1300**	2372	1427	**2600**	4712	2149	**3900**	7052
33.3	**92**	197.6	710	**1310**	2390	1432	**2610**	4730	2154	**3910**	7070
33.9	**93**	199.4	716	**1320**	2408	1438	**2620**	4748	2160	**3920**	7088
34.4	**94**	201.2	721	**1330**	2426	1443	**2630**	4766	2166	**3930**	7106
35.0	**95**	203.0	727	**1340**	2444	1449	**2640**	4784	2171	**3940**	7124
35.6	**96**	204.8	732	**1350**	2462	1454	**2650**	4802	2177	**3950**	7142
36.1	**97**	206.6	738	**1360**	2480	1460	**2660**	4820	2182	**3960**	7160
36.7	**98**	208.4	743	**1370**	2498	1466	**2670**	4838	2188	**3970**	7178
37.2	**99**	210.2	749	**1380**	2516	1471	**2680**	4856	2193	**3980**	7196
37.8	**100**	212.0	754	**1390**	2534	1477	**2690**	4874	2199	**3990**	7214
43	**110**	230	760	**1400**	2552	1482	**2700**	4892	2204	**4000**	7232
49	**120**	248	766	**1410**	2570	1488	**2710**	4910	2210	**4010**	7250
54	**130**	266	771	**1420**	2588	1493	**2720**	4928	2216	**4020**	7268
60	**140**	284	777	**1430**	2606	1499	**2730**	4946	2221	**4030**	7286
66	**150**	302	782	**1440**	2624	1504	**2740**	4964	2227	**4040**	7304
71	**160**	320	788	**1450**	2642	1510	**2750**	4982	2232	**4050**	7322
77	**170**	338	793	**1460**	2660	1516	**2760**	5000	2238	**4060**	7340

82	**180**	356	799	**1470**	2678	1521	**2770**	5018	2243	**4070**	7358
88	**190**	374	804	**1480**	2786	1527	**2780**	5036	2249	**4080**	7376
93	**200**	392	810	**1490**	2714	1532	**2790**	5054	2254	**4090**	7394
99	**210**	410	816	**1500**	2732	1538	**2800**	5072	2260	**4100**	7412
100	**212**	413	821	**1510**	2750	1543	**2810**	5090	2288	**4150**	7502
104	**220**	428	827	**1520**	2768	1549	**2820**	5108	2316	**4200**	7592
110	**230**	446	832	**1530**	2786	1554	**2830**	5126	2343	**4250**	7682
116	**240**	464	838	**1540**	2804	1560	**2840**	5144	2371	**4300**	7772
121	**250**	482	843	**1550**	2822	1566	**2850**	5162	2399	**4350**	7862

(table continued on next page)

Table B-14: (Continued)

°C	Ref.	°F	°C	Ref.	°F	°C	Ref.	°F	°C	Ref.	°F
127	**260**	500	849	**1560**	2840	1571	**2860**	5180	2427	**4400**	7952
132	**270**	518	854	**1570**	2858	1577	**2870**	5198	2454	**4450**	8042
138	**280**	536	860	**1580**	2876	1582	**2880**	5216	2482	**4500**	8132
143	**290**	554	866	**1590**	2894	1588	**2890**	5234	2510	**4550**	8222
149	**300**	572	871	**1600**	2912	1593	**2900**	5252	2538	**4600**	8312
154	**310**	590	877	**1610**	2930	1599	**2910**	5270	2566	**4650**	8402
160	**320**	608	882	**1620**	2948	1604	**2920**	5288	2593	**4700**	8492
166	**330**	626	888	**1630**	2966	1610	**2930**	5306	2621	**4750**	8582
171	**340**	644	893	**1640**	2984	1616	**2940**	5324	2649	**4800**	8672
177	**350**	662	899	**1650**	3002	1621	**2950**	5342	2677	**4850**	8762
182	**360**	680	904	**1660**	3020	1627	**2960**	5360	2704	**4900**	8852
188	**370**	698	910	**1670**	3038	1632	**2970**	5378	2732	**4950**	8942
193	**380**	716	916	**1680**	3056	1638	**2980**	5396	2760	**5000**	9032

Temperature conversion formulae:

°C = 5/9(°F - 32) °F = 9/5°C + 32
Kelvin = °C + 273.15 Rankine = °F + 459.67

Table example:

To convert 100°C to °F look up 100 in bold face in the the reference column. The corresponding Fahrenhe temperature is 212°F at the right.

To convert 100°F to °C look up 100 in bold face in the the reference column. The corresponding Centigra temperature is 37.8°C at the left.

Table B-15: Metric conversion chart

Inch	mm	Inch	mm	Inch	mm	Inch	mm
.001	0.0254	.251	6.3754	.501	12.7254	.751	19.0754
.002	0.0508	.252	6.4008	.502	12.7508	.752	19.1008
.003	0.0762	.253	6.4262	.503	12.7762	.753	19.1262
.004	0.1016	.254	6.4516	.504	12.8016	.754	19.1516
.005	0.1270	.255	6.4770	.505	12.8270	.755	19.1770
.006	0.1524	.256	6.5024	.506	12.8524	.756	19.2024
.007	0.1778	.257	6.5278	.507	12.8778	.757	19.2278
.008	0.2032	.258	6.5532	.508	12.9032	.758	19.2532
.009	0.2286	.259	6.5786	.509	12.9286	.759	19.2786
.010	0.2540	.260	6.6040	.510	12.9540	.760	19.3040
.011	0.2794	.261	6.6294	.511	12.9794	.761	19.3294
.012	0.3048	.262	6.6548	.5118	13.0000	.762	19.3548
.013	0.3302	.263	6.6802	.512	13.0048	.763	19.3802
.014	0.3556	.264	6.7056	.513	13.0302	.764	19.4056
.015	0.3810	.265	6.7310	.514	13.0556	.765	19.4310
1/64 .0156	0.3969	**17/64 .2656**	6.7469	.515	13.0810	**49/64 .7656**	19.4469
.016	0.4064	.266	6.7564	**33/64 .5156**	13.0968	.766	19.4564
.017	0.4318	.267	6.7818	.516	13.1064	.767	19.4818
.018	0.4572	.268	6.8072	.517	13.1318	.768	19.5072
.019	0.4826	.269	6.8326	.518	13.1572	.769	19.5326
.020	0.5080	.270	6.8580	.519	13.1826	.770	19.5580
.021	0.5334	.271	6.8834	.520	13.2080	.771	19.5834
.022	0.5588	.272	6.9088	.521	13.2334	.772	19.6088
.023	0.5842	.273	6.9342	.522	13.2588	.773	19.6342
.024	0.6096	.274	6.9596	.523	13.2842	.774	19.6596
.025	0.6350	.275	6.9850	.524	13.3096	.775	19.6850
.026	0.6604	.2756	7.0000	.525	13.3350	.776	19.7104
.027	0.6858	.276	7.0104	.526	13.3604	.777	19.7358
.028	0.7112	.277	7.0358	.527	13.3858	.778	19.7612
.029	0.7366	.278	7.0612	.528	13.4112	.779	19.7866

.030	0.7620	.279	7.866	.529	13.4366	.780	19.8120
.031	0.7874	.280	7.1120	.530	13.4620	.781	19.8374
1/32 .0312	0.7937	.281	7.1374	.531	13.4874	**25/32 .7812**	19.8433
.032	0.8128	**9/32 .2812**	7.1437	**17/32 .5312**	13.4937	.782	19.8628
.033	0.8382	.282	7.1628	.532	13.5128	.783	19.8882
.034	0.8636	.283	7.1882	.533	13.5382	.784	19.9136
.035	0.8890	.284	7.2136	.534	13.5636	.785	19.9390
.036	0.9144	.285	7.2390	.535	13.5890	.786	19.9644
.037	0.9398	.286	7.2644	.536	13.6144	.787	19.9898
.038	0.9652	.287	7.2898	.557	13.6398	.7874	20.0000
.039	0.9906	.288	7.3152	.538	13.6652	.788	20.0152

(table continued on next page)

Table B-15: (Continued)

Inch	mm	Inch	mm	Inch	mm	Inch	mm
.0394	1.0000	.289	7.3406	.539	13.6906	.789	20.0406
.040	1.0160	.290	7.3660	.540	13.7160	.790	20.0660
.041	1.0414	.291	7.3914	.541	13.7414	.791	20.0914
.042	1.0668	.292	7.4168	.542	13.7668	.792	20.1168
.043	1.0922	.293	7.4422	.543	13.7922	.793	20.1422
.044	1.1176	.294	7.4676	.544	13.8176	.794	20.1676
.045	1.1430	.295	7.4930	.545	13.8430	.795	20.1930
.046	1.1684	.296	7.5184	.546	13.8684	.796	20.2184
3/64 .0469	1.1906	**19/64 .2969**	7.5406	**35/64 .5469**	13.8906	**51/64 .7969**	20.2402
.047	1.1938	.297	7.5438	.547	13.8938	.797	20.2438
.048	1.2192	.298	7.5692	.548	13.9192	.798	20.2692
.049	1.2446	.299	7.5946	.549	13.9446	.799	20.2946
.050	1.2700	.300	7.6200	.550	13.9700	.800	20.3200
.051	1.2954	.301	7.6454	.551	13.9954	.801	20.3454
.052	1.3208	.302	7.6708	.5512	14.0000	.802	20.3708
.053	1.3462	.303	7.6962	.552	14.0208	.803	20.3962
.054	1.3716	.304	7.7216	.553	14.0462	.804	20.4216
.055	1.3970	.305	7.7470	.554	14.0716	.805	20.4470
.056	1.4224	.306	7.7724	.555	14.0970	.806	20.4724
.057	1.4478	.307	7.7978	.556	14.1224	.807	20.4978
.058	1.4732	.308	7.8232	.557	14.1478	.808	20.5232
.059	1.4986	.309	7.8486	.558	14.1732	.809	20.5486
.060	1.5240	.310	7.8740	.559	14.1986	.810	20.5740
.061	1.5494	.311	7.8994	.560	14.2240	.811	20.5994
.062	1.5748	.312	7.9248	.561	14.2494	.812	20.6248
1/1 .0625	1.5875	**5/16 .3125**	7.9375	.562	14.2748	**13/16 .8125**	20.6375
.063	1.6002	.313	7.9502	**9/16 .5625**	14.2875	.813	20.6502
.064	1.6256	.314	7.9756	.563	14.3002	.814	20.6756
.065	1.6510	.3150	8.0000	564	14.3256	.815	20.7010
.066	1.6764	.315	8.0010	.565	14.3510	.816	20.7264

.067	1.7018	.316	8.0264	.566	14.3764	.817	20.7518
.068	1.7272	.317	8.0518	.567	14.4018	.818	20.7772
.069	1.7526	.318	8.0772	.568	14.4272	.819	20.8026
.070	1.7780	.319	8.1026	.569	14.4526	.820	20.8280
.071	1.8034	.320	8.1280	.570	14.4780	.821	20.8534
.072	1.8288	.321	8.1534	.571	14.5034	.822	20.8788
.073	1.8542	.322	8.1788	.572	14.5288	.823	20.9042
.074	1.8796	.323	8.2042	.573	14.5542	.824	20.9296
.075	1.9050	.324	8.2296	.574	14.5796	.825	20.9550
.076	1.9304	.325	8.2550	.575	14.6050	.826	20.9804
.077	1.9558	.326	8.2804	.576	14.6304	.8268	21.0000
.078	1.9812	.327	8.3058	.577	14.6558	.827	21.0058
5/64 .0781	1.9844	.328	8.3312	.578	14.6812	.828	21.0312

(table continued on next page)

Table B-15: (Continued)

Inch	mm	Inch	mm	Inch	mm	Inch	mm
.0787	2.0000	**21/64 .3281**	8.3344	**37/64 .5781**	14.6844	**53/64 .8281**	21.0344
.079	2.0066	.329	8.3566	.579	14.7066	.829	21.0566
.080	2.0320	.330	8.3820	.580	14.7320	.830	21.0820
.081	2.0574	.331	8.4074	.581	14.7574	.831	21.1074
.082	2.0828	.332	8.4328	.582	14.7828	.832	21.1328
.083	2.1082	.333	8.4582	.583	14.8082	.833	21.1582
.084	2.1336	.334	8.4836	.584	14.8336	.834	21.1836
.085	2.1590	.335	8.5090	.585	14.8590	.835	21.2090
.086	2.1844	.336	8.5344	.586	14.8844	.836	21.2344
.087	2.2098	.337	8.5598	.587	14.9098	.837	21.2598
.088	2.2352	.338	8.5852	.588	14.9352	.838	21.2852
.089	2.2606	.339	8.6106	.589	14.9606	.839	21.3106
.090	2.2860	.340	8.6360	.590	14.9860	.840	21.3360
.091	2.3114	.341	8.6614	.5906	15.0000	.841	21.3614
.092	2.3368	.342	8.6868	.591	15.0114	.842	21.3868
.093	2.3622	.343	8.7122	.592	15.0368	.843	21.4122
3/32 .0937	2.3812	**11/32 .3437**	8.7312	.593	15.0622	**27/32 .8437**	21.4312
.094	2.3876	.344	8.7376	**19/32 .5937**	15.0812	.844	21.4376
.095	2.4130	.345	8.7630	.594	15.0876	.845	21.4630
.096	2.4384	.346	8.7884	.595	15.1130	.846	21.4884
.097	2.4638	.347	8.8138	.596	15.1384	.847	21.5138
.098	2.4892	.348	8.8392	.597	15.1638	.848	21.5392
.099	2.5146	.349	8.8646	.598	15.1892	.849	21.5646
.100	2.5400	.350	8.8900	.599	15.2146	.850	21.5900
.101	2.5654	.351	8.9154	.600	15.2400	.851	21.6154
.102	2.5908	.352	8.9408	.601	15.2654	.852	21.6408
.103	2.6162	.353	8.9662	.602	15.2908	.853	21.6662
.104	2.6416	.354	8.9916	.603	15.3162	.854	21.6916
.105	2.6670	.3543	9.0000	.604	15.3416	.855	21.7170
.106	2.6924	.355	9.0170	.605	15.3670	.856	21.7424

.107	2.7178	.356	9.0424	.606	15.3924	.857	21.7678
.108	2.7432	.357	9.0678	.607	15.4178	.858	21.7932
.109	2.7686	.358	9.0932	.608	15.4432	.859	21.8186
7/64 .1094	2.7781	.359	9.1186	.609	15.4686	**55/64 .8594**	21.8281
.110	2.7940	**23/64 .3594**	9.1281	**39/64 .6094**	15.4781	.860	21.8440
.111	2.8194	.360	9.1440	.610	15.4940	.861	21.8694
.112	2.8448	.361	9.1694	.611	15.5194	.862	21.8948
.113	2.8702	.362	9.1948	.612	15.5448	.863	21.9202
.114	2.8956	.363	9.2202	.613	15.5702	.864	21.9456
.115	2.9210	.364	9.2456	.614	15.5956	.865	21.9710
.116	2.9464	.365	9.2710	.615	15.6210	.866	21.9964
.117	2.9718	.366	9.2964	.616	15.6464	.8661	22.0000
.118	2.9972	.367	9.3218	.617	15.6718	.867	22.0218

(table continued on next page)

Table B-15: (Continued)

Inch	mm	Inch	mm	Inch	mm	Inch	mm
.1181	3.0000	.368	9.3472	.618	15.6972	.868	22.0472
.119	3.0226	.369	9.3726	.619	15.7226	.869	22.0726
.120	3.0480	.370	9.3980	.620	15.7480	.870	22.0980
.121	3.0734	.371	9.4234	.621	15.7734	.871	22.1234
.122	3.0988	.372	9.4488	.622	15.7988	.872	22.1488
.123	3.1242	.373	9.4742	.623	15.8242	.873	22.1742
.124	3.1496	.374	9.4996	.624	15.8496	.874	22.1996
1/8 .125	3.1750	**3/8 .375**	9.5250	**5/8 .625**	15.8750	**7/8 .875**	22.2250
.126	3.2004	.376	9.5504	.626	15.9004	.876	22.2504
.127	3.2258	.377	9.5758	.627	15.9258	.877	22.2758
.128	3.2512	.378	9.6012	.628	15.9512	.878	22.3012
.129	3.2766	.379	9.6266	.629	15.9766	.879	22.3266
.130	3.3020	.380	9.6520	.6299	16.0000	.880	22.3520
.131	3.3274	.381	9.6774	.630	16.0020	.881	22.3774
.132	3.3528	.382	9.7028	.631	16.0274	.882	22.4028
.133	3.3782	.383	9.7282	.632	16.0528	.883	22.4282
.134	3.4036	.384	9.7536	.633	16.0782	.884	22.4536
.135	3.4290	.385	9.7790	.634	16.1036	.885	22.4790
.136	3.4544	.386	9.8044	.635	16.1290	.886	22.5044
.137	3.4798	.387	9.8298	.636	16.1544	.887	22.5298
.138	3.5052	.388	9.8552	.637	16.1798	.888	22.5552
.139	3.5306	.389	9.8806	.638	16.2052	.889	22.5806
.140	3.5560	.390	9.9060	.639	16.2306	.890	22.6060
9/64 .1406	3.5719	**25/64 .3906**	9.9219	.640	16.2560	**57/64 .8906**	22.6219
.141	3.5814	.391	9.9314	**41/64 .6406**	16.2719	.891	22.6314
.142	3.6068	.392	9.9568	.641	16.2814	.892	22.6568
.143	3.6322	.393	9.9822	.642	16.3068	.893	22.6822
.144	3.6576	.3937	10.0000	.643	16.3322	.894	22.7076
.145	3.6830	.394	10.0076	.644	16.3576	.895	22.7330
.146	3.7084	.395	10.0330	.645	16.3830	.896	22.7584

.147	3.7338	.396	10.0584	.646	16.4084	.897	22.7838
.148	3.7592	.397	10.0838	.647	16.4338	.898	22.8092
.149	3.7846	.398	10.1092	.648	16.4592	.899	22.8346
.150	3.8100	.399	10.1346	.649	16.4846	.900	22.8600
.151	3.8354	.400	10.1600	.650	16.5100	.901	22.8854
.152	3.8608	.401	10.1854	.651	16.5354	.902	22.9108
.153	3.8862	.402	10.2108	.652	16.5608	.903	22.9362
.154	3.9116	.403	10.2362	.653	16.5862	.904	22.9616
.155	3.9370	.404	10.2616	.654	16.6116	.905	22.9870
.156	3.9624	.405	10.2870	.656	16.6370	.9055	23.0000
5/32 .1562	3.9687	.406	10.3124	.656	16.6624	.906	23.0124
.157	3.9878	**13/32 .4062**	10.3187	**21/32 .6562**	16.6687	**29/32 .9062**	23.0187
.1575	4.0000	.407	10.3378	.657	16.6878	.907	23.0378

(table continued on next page)

Table B-15: (Continued)

Inch	mm	Inch	mm	Inch	mm	Inch	mm
.158	4.0132	.408	10.3632	.658	16.7132	.908	23.0632
.159	4.0386	.409	10.3886	.659	16.7386	.909	23.0886
.160	4.0640	.410	10.4140	.660	16.7640	.910	23.1140
.161	4.0894	.411	10.4394	.661	16.7894	.911	23.1394
.162	4.1148	.412	10.4648	.662	16.8148	.912	23.1648
.163	4.1402	.413	10.4902	.663	16.8402	.913	23.1902
.164	4.1656	.414	10.5156	.664	16.8656	.914	23.2156
.165	4.1910	.415	10.5410	.665	16.8910	.915	23.2410
.166	4.2164	.416	10.5664	.666	16.9164	.916	23.2664
.167	4.2418	.417	10.5918	.667	16.9418	.917	23.2918
.168	4.2672	.418	10.6172	.668	16.9672	.918	23.3172
.169	4.2926	.419	10.6426	.669	16.9926	.919	23.3426
.170	4.3180	.420	10.6680	.6693	17.0000	.920	23.3680
.171	4.3434	.421	10.6934	.670	17.0180	.921	23.3934
11/64 .1719	4.3656	**27/64 .4219**	10.7156	.671	17.0434	**59/64 .9219**	23.4156
.172	4.3688	.422	10.7188	**43/64 .6719**	17.0656	.922	23.4188
.173	4.3942	.423	10.7442	.672	17.0688	.923	23.4442
.174	4.4196	.424	10.7696	.673	17.0942	.924	23.4696
.175	4.4450	.425	10.7950	.674	17.1196	.925	23.4950
.176	4.4704	.426	10.8204	.675	17.1450	.926	23.5204
.177	4.4958	.427	10.8458	.676	17.1704	.927	23.5458
.178	4.5212	.428	10.8712	.677	17.1958	.928	23.5712
.179	4.5466	.429	10.8966	.678	17.2212	.929	23.5966
.180	4.5720	.430	10.9220	.679	17.2466	.930	23.6220
.181	4.5974	.431	10.9474	.680	17.2720	.931	23.6474
.182	4.6228	.432	10.9728	.681	17.2974	.932	23.6728
.183	4.6482	.433	10.9982	.682	17.3228	.933	23.6982
.184	4.6736	.4331	11.0000	.683	17.3482	.934	23.7236
.185	4.6990	.434	11.0236	.684	17.3736	.935	23.7490
.186	4.7244	.435	11.0490	.685	17.3990	.936	23.7744

.187	4.7498	.436	11.0744	.686	17.4244	.937	23.7998
3/1 .1875	4.7625	.437	11.0998	.687	17.4498	**15/16 .9375**	23.8125
.188	4.7752	**7/16 .4375**	11.1125	**11/16 .6875**	17.4625	.938	23.8252
.189	4.8006	.438	11.1252	.688	17.4752	.939	23.8506
.190	4.8260	.439	11.11506	.689	17.5006	.940	23.8760
.191	4.8514	.440	11.1760	.690	17.5260	.941	23.9014
.192	4.8768	.441	11.2014	.691	17.5514	.942	23.9268
.193	4.9022	.442	11.2268	.692	17.5768	.943	23.9522
.194	4.9276	.443	11.2522	.693	17.6022	.944	23.9776
.195	4.9530	.444	11.2776	.694	17.6276	.9449	24.0000
.196	4.9784	.445	11.3030	.695	17.6530	.945	24.0030
.1969	5.0000	.446	11.3284	.696	17.6784	.946	24.0284
.197	5.0038	.447	11.3538	.697	17.7038	.947	24.0538

(table continued on next page)

Table B-15: (Continued)

Inch	mm	Inch	mm	Inch	mm	Inch	mm
.198	5.0292	.448	11.3792	.698	17.7292	.948	24.0792
.199	5.0546	.449	11.4046	.699	17.7546	.949	24.1046
.200	5.0800	.450	11.4300	.700	17.7800	.950	24.1300
.201	5.1054	.451	11.4554	.701	17.8054	.951	24.1554
.202	5.1308	.452	11.4808	.702	17.8308	.952	24.1808
.203	5.1562	.453	11.5062	.703	17.8562	.953	24.2062
13/64 .2031	5.1594	**29/64 .4531**	11.5094	**45/64 .7031**	17.8594	**61/64 .9531**	24.2094
.204	5.1816	.454	11.5316	.704	17.8816	.954	24.2316
.205	5.2070	.455	11.5570	.705	17.9070	.955	24.2570
.206	5.2324	.456	11.5824	.706	17.9324	.956	24.2824
.207	5.2578	.457	11.6078	.707	17.9578	.957	24.3078
.208	5.2832	.458	11.6332	.708	17.9832	.958	24.3332
.209	5.3086	.459	11.6586	.7087	18.0000	.959	24.3586
.210	5.3340	.460	11.6840	.709	18.0086	.960	24.3840
.211	5.3594	.461	11.7094	.710	18.0340	.961	24.4094
.212	5.3848	.462	11.7348	.711	18.0594	.962	24.4348
.213	5.4102	.463	11.7602	.712	18.0848	.963	24.4602
.214	5.4356	.464	11.7856	.713	18.1102	.964	24.4856
.215	5.4610	.465	11.8110	.714	18.1356	.965	24.5110
.216	5.4864	.466	11.8364	.715	18.1610	.966	24.5364
.217	5.5118	.467	11.8618	.716	18.1864	.967	24.5618
.218	5.5372	.468	11.8872	.717	18.2118	.968	24.5872
7/32 .2187	5.5562	**15/32 .4687**	11.9062	.718	18.2372	**31/32 .9687**	24.6062
.219	5.5626	.469	11.9126	**23/32 .7187**	18.2562	.969	24.6126
.220	5.5880	.470	11.9380	.719	18.2626	.970	24.6380
.221	5.6134	.471	11.9634	.720	18.2880	.971	24.6634
.222	5.6388	.472	11.9888	.721	18.3134	.972	24.6888
.223	5.6642	.4724	12.0000	.722	18.3388	.973	24.7142
.224	5.6896	.473	12.0142	.723	18.3642	.974	24.7396
.225	5.7150	.474	12.0396	.724	18.3896	.975	24.7650

.226	5.7404	.475	12.0650	.725	18.4150	.976	24.7904
.227	5.7658	.476	12.0904	.726	18.4404	.977	24.8158
.228	5.7912	.477	12.1158	.727	18.4658	.978	24.8412
.229	5.8166	.478	12.1412	.728	18.4912	.979	24.8666
.230	5.8420	.479	12.1666	.729	18.5166	.980	24.8920
.231	5.8674	.480	12.1920	.730	18.5420	.981	24.9174
.232	5.8928	.481	12.2174	.731	18.5674	.982	24.9428
.233	5.9182	.482	12.2428	.732	18.5928	.983	24.9682
.234	5.9436	.483	12.2682	.733	18.6182	.984	24.9936
15/64 .2344	5.9531	.484	12.2936	.734	18.6436	.9843	25.0000
.235	5.9690	**31/64 .4844**	12.3031	**47/64 .7344**	18.6532	**63/64 .9844**	25.0031
.236	5.9944	.485	12.3190	.735	18.6690	.985	25.0190
.2362	6.0000	.486	12.3444	.736	18.6944	.986	25.0444

(table continued on next page)

Table B-15: (Continued)

Inch	mm	Inch	mm	Inch	mm	Inch	mm
.237	6.0198	.487	12.3698	.737	18.7198	.987	25.0698
.238	6.0452	.488	12.3952	.738	18.7452	.988	25.0952
.239	6.0706	.489	12.4206	.739	18.7706	.989	25.1206
.240	6.0960	.490	12.4460	.740	18.7960	.990	25.1460
.241	6.1214	.491	12.4714	.741	18.8214	.991	25.1714
.242	6.1468	.492	12.4968	.742	18.8468	.992	25.1968
.243	6.1722	.493	12.5222	.743	18.8722	.993	25.2222
.244	6.1976	.494	12.5476	.744	18.8976	.994	25.2476
.245	6.2230	.495	12.5730	.745	18.9230	.995	25.2730
.246	6.2484	.496	12.5984	.746	18.9484	.996	25.2984
.247	6.2738	.497	12.6238	.747	18.9738	.997	25.3238
.248	6.2992	.498	12.6492	.748	18.9992	.998	25.3492
.249	6.3246	.499	12.6746	.7480	19.0000	.999	25.3746
1/4 .250	6.3500	**1/2 .500**	12.7000	.749	19.0246	**1/1 1.000**	25.4000
				3/4 .750	19.0500		

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