CAPITAL UNIVERSITY OF SCIENCE AND TECHNOLOGY, ISLAMABAD

Comparative Analysis of Conventional VSC and MMC on the Basis of Output Power Quality and Control Performance

by

Tanzeela Irshad

A thesis submitted in partial fulfillment for the degree of Master of Science

in the

Faculty of Engineering
Department of Electrical Engineering

2019

I dedicate this work to my dearest parents and elder sister

CERTIFICATE OF APPROVAL

Comparative Analysis of Conventional VSC and MMC on the Basis of Power Quality and Control Performance

by

Tanzeela Irshad

(MEE163014)

THESIS EXAMINING COMMITTEE

S. No.	Examiner	Name	Organization
(a)	External Examiner	Dr. Syed Ali Abbas Kazmi	NUST, Islamabad
(b)	Internal Examiner	Dr. Amir Iqbal Bhatti	CUST, Islamabad
(c)	Supervisor	Dr. Umer Amir Khan	CUST, Islamabad

Dr. Umer Amir Khan
Thesis Supervisor
April, 2019

Dr. Noor Muhammad Khan
Head
Dept. of Electrical Engineering
April, 2019

Dr. Imtiaz Ahmed Taj
Dean
Faculty of Engineering
April, 2019

Author's Declaration

I, **Tanzeela Irshad** hereby state that my MS thesis titled "**Comparative Analysis of Conventional VSC and MMC on the Basis of Power Quality and Control Performance**" is my own work and has not been submitted previously by me for taking any degree from Capital University of Science and Technology, Islamabad or anywhere else in the country/abroad.

At any time if my statement is found to be incorrect even after my graduation, the University has the right to withdraw my MS Degree.

(Tanzeela Irshad)

Registration No: MEE163014

Plagiarism Undertaking

I solemnly declare that research work presented in this thesis titled "*Comparative Analysis of Conventional VSC and MMC on the Basis of Power Quality and Control Performance*" is solely my research work with no significant contribution from any other person. Small contribution/help wherever taken has been dully acknowledged and that complete thesis has been written by me.

I understand the zero tolerance policy of the HEC and Capital University of Science and Technology towards plagiarism. Therefore, I as an author of the above titled thesis declare that no portion of my thesis has been plagiarized and any material used as reference is properly referred/cited.

I undertake that if I am found guilty of any formal plagiarism in the above titled thesis even after award of MS Degree, the University reserves the right to withdraw/revoke my MS degree and that HEC and the University have the right to publish my name on the HEC/University website on which names of students are placed who submitted plagiarized work.

(Tanzeela Irshad)

Registration No: MEE163014

Acknowledgements

After being utmost grateful to Almighty Allah who gave me help and courage to complete my M.S research work, I would like to express huge gratitude towards the person who is not only my supervisor but also my mentor **Dr. Umer Amir Khan** whose constant support, guidance and rightful critics kept me steering in the right direction during my entire research work to get through this demanding and tiresome task. I am fortunate to work with him which make me able to benefit myself from his knowledge regarding research skills and high voltage direct current transmission.

I would like to pay huge debt of gratitude to my dearest family members; my Father Muhammad Irshad, my Mother Shagufta Shaheen, my elder Brother Sami-ullah, my elder Sister Tayyaba Irshad, my younger Sister Aqsa Irshad and my younger Brother Ahmad Irshad who always supported me during thick and thin and encouraged me to stay motivated through out my degree program in order to achieve my goals.

Dr. Amir Iqbal Bhatti has always been an inspiration for me regarding his vast knowledge about control systems, for whom I am indebted for his guidance during the control design of MMC which really helped me to proceed in the right direction. Besides I am thankful to every single member at CASPR Lab with special thanks to Dr. Raheel Anjum who always helped me to get through my queries related to research, control and thesis write up.

I pay my deep regards to all of my friends especially Anum Munir, Reshail Khan, Nadir Mehmood, Zohaib Latif, Afia Qamar, Ayesha Shakeel, and Sadia Malik for always being there whenever I needed them for help. I would also like to acknowledge my colleague at ARC academy, Shakeel Ahmed who always guided me to take thesis as first priority and helped me by managing my students many times for my absentees which i made due to research work. In the end I would like to acknowledge CUST Library where I used to spend hours to carry out my

research studies and the staff also, who always provided me with the literature in time whenever I required.

(Tanzeela Irshad)

Registration No: MEE163014

Abstract

The conventional two-level voltage source converter (VSC) was first commercialized by ABB in 1997 in an HVDC project. Being cost effective, compact, having simpler design structure and stiff control, it attracted the vendors to be utilized in high voltage high power applications. But it offered certain limitations one of which includes; the requirement of bulky and expensive filters to mitigate the low frequency harmonics present in the output voltage waveform. Although the use of high switching frequency pushes the low order frequency spectrum to higher order frequencies which helps with reduced filter costs and size but corresponds another cumbersome issue of increased converter switching losses up to 1.7%. Thus there is always a conflicting design compromise between converter losses and need for filtration.

Another troublesome issue with conventional VSC is that it requires the chains of series connected IGBTs to make converter arm valves. Being low to medium voltage rated devices typically ranging from (1.7k-6.5kV), these devices does not hold the capability to withstand the high voltage operating ratings. Therefore these switching devices require sophisticated gate drives to provide dynamic and static voltage balancing to ensure the simultaneous switching of all the IGBTs in the same converter arm. This cumbersome issue corresponds a water bed situation which limits the overall working efficiency of 2-level VSC.

This work is mainly aimed to propose a compact design solution for all the foregoing problems, by using 21-level Modular multilevel converter (MMC) that being multilevel does away with massive and expensive filter requirements and being modular eliminates the need for fussy series connected IGBTs when utilized in high voltage high power applications like HVDC. The converter switches commutate at lower switching frequency thus converter losses are greatly reduced.

The design structure involves the use of 100kV converter station tied to a 220kV and 50Hz Grid station connected with two 50MW parallel loads through two

successive transmission lines of 10km. The modeling and design of grid tied conventional VSC and MMC is presented. Converter control is implemented in direct quadrature(dq0) frame using vector control technique, where active and reactive power are efficiently and independently controlled at point of common coupling (PCC). The Proportional (P) and Integral (I) gains of the PI compensator are optimized by using Modulus optimum tuning criteria. Furthermore, both conventional VSC and MMC are analyzed and compared on the basis of mathematical model of their AC side dynamics, control complexity and stability conditions, output voltage quality, switching losses, total harmonic distortion (THD), AC harmonic spectrum analysis, filter requirement, costs and design structure.

Contents

List of Figures

List of Tables

Abbreviations

HVDC	High voltage direct current
HVAC	High voltage alternating current
GTVSC	Grid tied Voltage Source Converter
GTMMC	Grid tied modular multilevel converter
PWM	pulse width modulation
SPWM	Sinusoidal pulse width modulation
PSPWM	Phase shifted pulse width modulation
LSPWM	Level shifted sinusoidal pulse width modulation
LCC	Line commutated converters
CSC	Current Source Converter
VSC	Voltage source converter
MMC	Modular multilevel converter
PCC	Point of common coupling
THD	Total harmonic Distortion
SVM	Space vector modulation
NLM	Nearest level modulation
SAM	Sampled average modulation
FC	Flying Capacitor
NPC	Neutral point clamped
CHB	Cascaded H Bridge
DQ0	Direct quadrature
AC	Alternating current
DC	Direct current
PI	Proportional Integral

GUI	Graphical user Interface
G.M	Gain Margin
P.M	Phase margin
AC	Alternating current
DC	Direct current
PI	Proportional Integral
GUI	Graphical user Interface
EMI	Electromagnetic Interference

Symbols

V_{dc}	Nominal Dc link Voltage
V_t	Converter output terminal Voltage
$R + jL$	Phase Reactance
V_{nompri}	Transformer nominal primary Voltage
V_{nomsec}	Transformer nominal secondary Voltage
K	Transformer turn ratio
f_{sw}	Converter switching Frequency
T_{spower}	Sampling time for power GUI
V_s	AC source voltage
π	Transmission line
P_g	Grid instantaneos power
f	System nominal frequency
V_p	Peak Voltage
m_f	Frequency Modulation Index
T_s	Sampling Time
f_s	Sampling Frequency
N_f	Number of cycles for FFT analysis
T_f	Time instant for FFT
h	Harmonic order
L_m	Maximum load
$\%mag$	Magnitude in percentage
A_p	Peak amplitude
$\%MOS$	Maximum overshoot percentage

t_p	Peak time
t_s	Settling time
t_r	Rise time
$\hat{m}$	Modulation index
N	Number of submodules or number ofcarriers
ϕ	Carrier Phase displacement
N_{st}	Total number of switching signals for three phase
N_s	Total number of switching signals in each phase
K_p	Proportional gain
K_i	Integral Gain
K_d	Differential gain
ω	Angular frequency
f_0	Minimum frequency
P_{nom}	Nominal power
V_d, V_q	DQ frame voltage
I_d, I_q	DQ frame current
$P\&Q$	Active and reactive power at PCC
$A_m\&A_c$	Amplitude of modulation signal and carrier wave
C	Capacitor
L_{arm}	Arm inductance
R_{arm}	Arm equivalent resistance
V_c	Capacitor voltage
$(Y_g\triangle)$	Wye grounded Delta

Chapter 1

Introduction

1.1 Background

Its been 100 years that electrical power is being generated, transmitted, distributed and apart from few traction, drives and processes it is also consumed as an alternating current (AC) [1]. In the early age of electrical power development, the presence of induction motors and transformers enabled to achieve desired power levels easily and economically therefore it was considered an effective way to be utilized at generation and distribution sides.

However, as far as matter of transmission of Bulk power over long distances is concerned, HVAC becomes an uneconomical and an inefficient way of transmitting electrical power because it offers huge line losses, costs and demands intermediate reactive power compensators which in turn limit the bulk power transmission over large distances [2]. On the other hand two asynchronous AC networks cannot be interconnected with each other due to stability concerns [3].

As there was always a need for an economical and an efficient power transmission system which could provide flexibility with asynchronous interconnections, offer lower line losses and costs during the transmission of electrical power therefore researchers started working to pursue such electrical transmission system and found HVDC as a viable alternative for HVAC transmission.

In 1929, the development of mercury arc valve rectifiers gained the attention of engineers to use high voltage direct current HVDC for the transmission of bulk power over long distances [4].

1.2 Why HVDC?

HVDC is becoming a state of art nowadays for its remarkable advantages over classical transmission of electrical power. Some of the major advantages for an HVDC link are described below [3, 4]

1. As HVDC operates at zero frequency, the transmission line has no inductive or capacitive losses, which enables the transmission of electrical power with unity power factor [2].
2. It allows the transmission of Bulk power over long distances across cities, seas and subcontinents whereas HVAC can only transmit electrical power over a distance of 40k beyond which it requires intermediate reactive power compensation [2, 5].
3. HVDC provides the stable interconnection between two or multiple asynchronous AC networks [2, 3, 5].
4. HVDC renders lower line losses and offers lower line costs as compared to HVAC.
5. It fully utilizes the conductor cross section because there is no skin affect [2].
6. After the break even distance for overhead lines which ranges from 500 to 800km, HVDC is more economical than HVAC [2].
7. HVDC is highly environment friendly and does not require large land areas for its installations [2, 6]

These advantages make HVDC transmission to be considered as viable alternative for HVAC transmission systems. The basic structure of a two terminal HVDC

transmission link is shown in Figure 1.1, it mainly constitutes two ends i.e. a transmitting end which is recognized as Rectifier Station and a receiving end which is recognized as an Inverter Station.

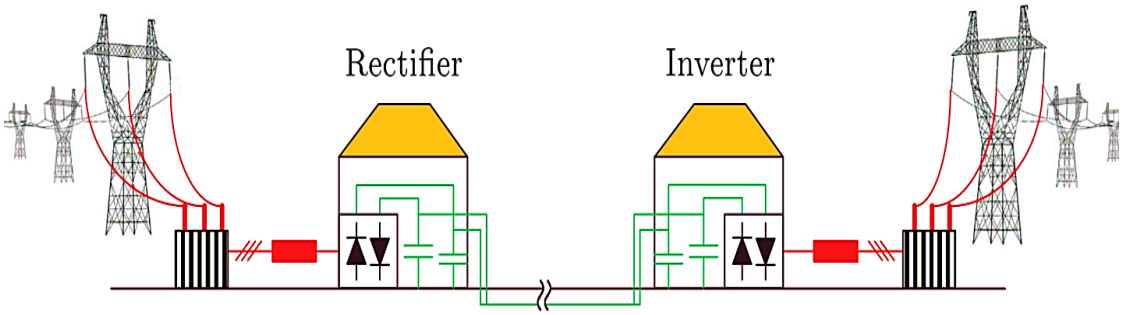

FIGURE 1.1: High Voltage Direct Transmission Layout

The rectifier station involves the conversion of electrical power from alternating current (AC) to direct current (DC) whereas the Inverter station involves the conversion of electrical power from DC to AC and in between, there is a long distance overhead/underwater transmission line which is utilized for the transmission of high voltage high power electricity [2, 3].

HVDC could only be thought of becoming a possibility on practical grounds with the help of high power converters, so power converters gained huge interest of researchers to work with and develop better converter technologies that could be utilized in HVDC [7]. On the basis of DC-link transmission systems there are two renowned converter technologies named as, Current Source Converters (CSC) and Voltage Source Converters (VSC), both are briefly discussed subsequently

1.3 Current Source Converters (CSC)

A Current source converter or simply CSC utilizes Thyristors as switching devices which commutate on line frequency therefore, also recognized as line commutated current source converters. It is a well developed and quite mature technology which is being used since 1970s for transmitting bulk electrical power over long distances.

1.3.1 Structure of CSC HVDC Converter Station

The basic structure of HVDC based CSC converter station is shown in Figure 1.2. It mainly comprises two series connected six pulse Converters, two coupling transformers one with Y-Y configuration and other with Δ-Y configuration which provides 30 deg phase shift and converts the six pulse output voltage to 12 pulse output voltage in order to enhance the output voltage quality [5, 8]. AC side harmonic filters are required to mitigate the switching frequency harmonics from the output voltage and provide reactive power required for compensation purposes [2]. DC side smoothing filters serve to mitigate the DC harmonics from the DC link voltage [5, 8]. Due to the necessity of large harmonic filters both on AC and DC side, the CSC HVDC occupies a huge space [5].

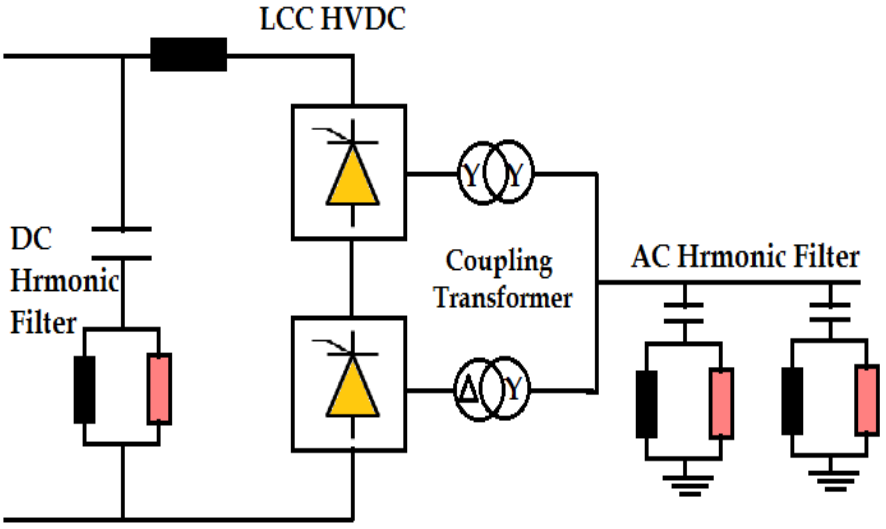

FIGURE 1.2: Lay out of CSC Based HVDC converter station [5]

As thyristors come up with highest power ratings therefore CSC based HVDC transmission is currently being considered as the only choice for the transmission of bulk power over large distances. However it may come up with certain discrepancies which require extra effort to produce the desired performance, some of these limitations are listed below;

1. Thyristors does not hold the capability to be turned off autonomously [9, 10].

2. The switching devices can commutate either with respect to line frequency or by forced commutation [2].
3. They require reactive power for the commutation of switches [10].
4. There is a demand of synchronous voltage sources to provide reactive power for the commutation of thyristors [5].
5. LCC technology needs bulky and expensive filters to not only clear the low frequency harmonic component present in the output voltage waveform but also to provide reactive power to meet its reactive power demands [5, 11] .
6. LCC converters always work with a delayed power factor [5, 10, 11].
7. It offers Poor reactive power control therefore active and reactive power cannot be controlled independently [8, 10].
8. They cannot work with isolated systems, therefore there is no black start capability with CSCs [10, 12].
9. The direction of power is reversed by reversing the voltage polarity which costs expensive cables [13].

The arrival of insulated gate bipolar transistors (IGBTs) in 1990, allowed the researchers to work for the converter technology which is more flexible and can be even used with renewable energy resources. This was the dawn of Voltage source converter (VSC) based HVDC technology and it has shown a huge development since it was first commercialized in 1997.

1.4 Voltage Source Converters (VSC)

VSC has addressed all those limitations which were encountered with CSC technology by using IGBTs as switching devices. These devices hold the capability to be turned on/off autonomously thus enabling the use of high frequency carrier pulse width modulation (PWM) to control the switching of the semiconductor devices.

1.4.1 Structure of VSC-HVDC

The basic structure of VSC based HVDC converter station is shown in Figure 1.3. It mainly comprises two DC link capacitors required to mitigate ripple in the dc link voltage, a single six pulse converter in which IGBTs are utilized for the commutation purposes, a phase reactor which is used to smooth out the harmonics in the converter output current waveform and provide interface between converter and coupling transformer, AC harmonic filter which is required for the filtration of AC output voltage harmonics and a coupling transformer which is used to provide suitable voltage levels for the grid and converter. However, it also acts as a filter which smooths out certain harmonics from converter output voltage and current waveforms.

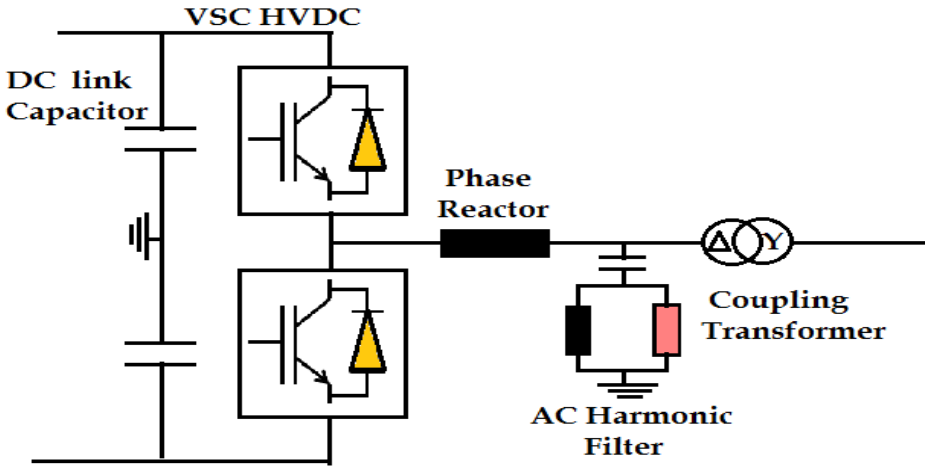

FIGURE 1.3: Lay out of VSC Based HVDC converter Station [5]

Some of the key advantages of VSC technology are discussed as under:

1. Switching devices (IGBTs) can be autonomously controlled [9, 10].
2. It allows the use of high frequency modulation techniques which considerably reduce the low frequency harmonics.
3. The need for voluminous and expensive AC harmonic filters is reduced.
4. It does not require reactive power however it can supply reactive power unlike CSC technology [10, 11].

5. It can operate with advanced as well as delayed power factor [10].
6. It shows high flexibility to independently control the active and reactive power.
7. It can work with isolated systems [12].
8. It has black start capability therefore it can even work with dead AC systems.
9. The direction of power flow is reversed by simply reversing the polarity of current [13].

The main focus of this dissertation is to analyze and discuss voltage source converter topologies regarding their technical advantages in HVDC, therefore the coming chapters are mainly dedicated towards the discussion of VSC based HVDC technology.

1.5 Thesis Objectives

This thesis is aimed to make a comprehensive comparative analysis of conventional VSC and MMC. Conventional VSC has a collection of simulation models in Matlab/Simulink but there was no MMC model present in the Simscape library therefore the first objective is to design 21-Level MMC model in Simulink which is achieved successfully. Later For the sake of standard comparison a test case is established in Matlab/Simulink environment in which both of the converters (conventional VSC and 21-Level MMC) are individually tied to a grid through phase reactor, coupling transformer, various loads and transmission lines. The case is developed to make the comparative analysis more realistic and practical.

The control structure is developed for the control of active and reactive power at point of common coupling (PCC). Later the performance is analyzed on full load conditions and compared on the basis of shape of converter output voltage waveform, its total harmonic distortion, AC harmonic spectrum, need for AC harmonic filter and switching losses. The frequency domain and time domain analysis

of both converters are made to investigate the stability margins and performance (steady state and transient state) of closed loop control respectively. Later the control complexities are also analyzed for both systems.

1.6 Thesis Overview

Chapter 1 of this thesis presents the historical background of HVDC and the developments made in the field of converter technologies along with their advantages and limitations.

Chapter 2 presents the literature review. A review of VSC topologies developed for the better performance of HVDC converters is presented through literature. The control strategies developed for the control of VSC HVDC converter is presented. Later the papers which present the comparative analysis of conventional two-level VSC and multilevel converters are also discussed. By the end of this chapter gap analysis is identified and problem statement for this thesis is defined.

Chapter 3 presents the mathematical modeling of conventional two-level grid tied VSC and 21-level grid tied Modular Multilevel Converter (MMC). Based on the mathematical models, this chapter presents the Matlab/Simulink test models which are developed for the analysis of both grid tied converter topologies.

Chapter 4 presents the control strategy adopted for the control of the inverter side dynamics of HVDC converter station. Using dq model of the 3-phase grid tied HVDC converter, the PI control is implemented. Modulus Optimum, a tuning technique is used to find out the optimum gains at which the inner current control loops are regulated.

Chapter 5 presents the results found by the comparison of conventional two-level grid tied VSC and 21-level grid tied MMC on the basis of converter output voltage and current quality. Both topologies are also analyzed on the basis of the transient and steady state behaviors during step input changes in the reference active and reactive power.

Chapter 6 concludes the whole discussion made throughout this thesis and elaborates the possible future work.

1.7 Thesis Outcomes

Thesis major outcomes are described as under.

1. Design of 21-level MMC model in Matlab/Simulink environment using Simscape Simpower library.
2. Development of 220kV, 50Hz Grid model with transmission and distribution network.
3. Successful Interface of 21-level MMC model and Grid model.
4. Development of grid tied Conventional two-level VSC model in Matlab/Simulink.
5. Design of inner current control loop in dq reference frame.
6. Active and reactive power control at PCC on various loads.
7. Transient and steady state analysis of both (21-Level MMC and 2-Level VSC) grid tied converters and later extraction of stability conditions.
8. Performance comparison on the basis of converter output voltage shapes, AC harmonic spectrum, total harmonic distortion, switching losses and AC harmonic filter requirements.
9. Finally Both converters were analyzed on the basis of control complexities.

1.8 Chapter Summary

This chapter provides a brief introduction of what HVDC is and why it is becoming more and more popular among renowned power transmission companies. Along

with its key attributes the renowned converter technologies are presented with their respective advantages and drawbacks. Towards the end of the chapter, thesis objectives and outcomes are listed to provide the overview of the entire thesis.

Chapter 2

Literature Survey

2.1 Introduction

VSC technology was first commercialized by ABB in 1997, by using two-level voltage source converters [8, 14]. The development did not clogged here due to the increased quest for economical and high quality power converters for high voltage high power applications. This made researchers to work harder and develop new multilevel converter topologies which include neutral point clamped converters (NPC), flying capacitor converters (FC), cascaded H-bridge converters (CHB) and modular multilevel converters (MMC). These converter topologies are discussed briefly along their characteristic limitations when utilized in HVDC applications. Later the gap analysis is presented for this dissertation while the problem statement is defined by the end of this chapter.

2.2 Conventional VSC

The conventional VSC is a basic two-level converter as its name indicates, its output switches between two voltage levels $+V_{dc}/2$ and $-V_{dc}/2$ [15, 16]. It uses high frequency carrier modulation for the switching purposes to produce a high

quality waveform [8, 15]. The schematic of single phase half bridge converter with its two-level output phase voltage waveform is shown in Figure 2.1.

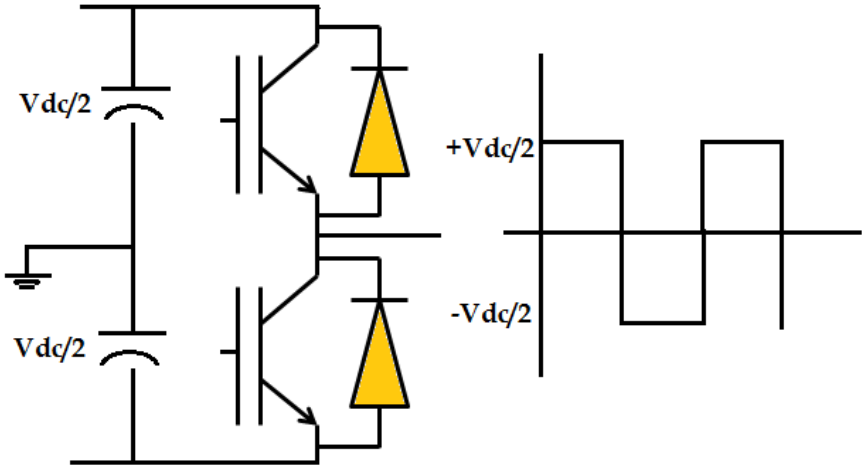

FIGURE 2.1: Single phase half bridge VSC with 2-level output voltage waveform [16]

The conventional VSC offers a number of advantages which include;

1. Simple circuit design [16, 17],
2. Compact structure [18],
3. Lower costs [18],
4. Lower control complexity [7, 17],
5. Less switching devices [17].

2.2.1 Current Role of Conventional VSC in HVDC

Conventional VSC attained huge interest of vendors due to its simple circuit design and lower control complexity which brought boom to its use in high voltage high power applications. Different renowned power companies which include ABB, ALStom and Siemens have commercialized many projects using two level VSC in

HVDC systems. A few of commercialized projects using two-level VSC since it was first developed, are presented in Table 2.1.

TABLE 2.1: List of the Conventional-VSC HVDC Commissioned Projects [14]

Name of Project	Year	Power Rating	Topology
Hellsjon	1997	3MW	2-level
Gotland HVDC Light	1999	50MW	2-level
Tajaereborg	2000	8MVA	2level
Terrenora Directlink	2000	180MW	2-level
TrolA offshore	2005	84MW	2-level
Estlink	2006	350MW	2-level
Nord.EON.1	2009	400MW	IGBTs
Vallhalloffshore	2009	78MW	2-level
Caprivilink	2010	300MW	2-level
Västlänken	ongoing	1200MW	2-level

2.3 Limitations of Conventional VSC

The market overview of conventional VSC shows that how it got success in high voltage high power applications for more than two decades and still it is being commercialized in many HVDC projects. Although two-level VSC offers lots of advantages as mentioned above but it offers certain limitations when used in high power high voltage applications preferably HVDC transmission [17, 19]. These limitations are comprehensively discussed in following sections.

2.3.1 Troublesome Series Connection of IGBTs

VSC technology uses IGBTs for the switching purposes with voltage ratings ranging from 1.7kV to 6.5kV [19, 20]. These low to medium voltage rated devices cannot withstand the stress of full DC-link voltages when used in high voltage high power applications like HVDC where the DC-link voltages are commonly more than 300kV [7, 17].

In order to achieve high voltage operating ratings there were two solutions i.e. either a step up transformer should be used at converter output to help in achieving the required voltage levels or to use the series connection of IGBTs to make converter arm valves in order to equally share the full DC-link voltage among each IGBT [7].

The first solution is not appropriate because high voltage high power transformers are costlier and increase the over all size of the converter station however second solution is considered more convenient to use as it does not effect the converter cost and size [7].

In two-level VSC, each valve comprising chain of series connected IGBTs is rated for full DC-link voltage, up to ($n > 100$) series connected IGBTs have previously been used in HVDC projects [17, 21].

Each IGBT in the converter arm valve is required to be switched simultaneously to equally share the full DC link voltage, therefore static (conduction mode) and dynamic (transient mode) voltage balancing is required for each switch cell [19].

2.3.1.1 Static Balancing

The static balancing is achieved by using a large resister R_g in parallel to every single switch cell in the entire series chain of IGBTs as shown in Figure 2.2 but at the cost of increased converter power losses [19].

2.3.1.2 Dynamic Balancing

The dynamic balancing is more serious and challenging task because the turning on and turning off time for an IGBT is very fast and in microseconds [22, 22, 23]. If dynamic balancing is not considered, the IGBT turning on first or in last will have to bear full DC-link voltage [19] which ultimately exceeds from maximum voltage rating of IGBTs and hence causes converter arm breakdown [17].

The use of RCD snubber circuits is proposed which can assist dynamic balancing by slowing the switching speed [19]. Another advantage of using snubber is that it limits the high dv/dt during turn off and di/dt during turn on of switching devices which reduces the EMI levels [19].

The use of snubber circuits can assist dynamic voltage balancing and limit di/dt and dv/dt but at the expense of reduced efficiency and increased equipment costs and power losses [19, 22]. Figure 2.2 shows the series connected IGBTs with grading resistors R_g to provide static voltage balancing, RCD snubbers to provide dynamic voltage balancing and lower dv/dt whereas series inductance L_s is used for the reduction of di/dt [19] .

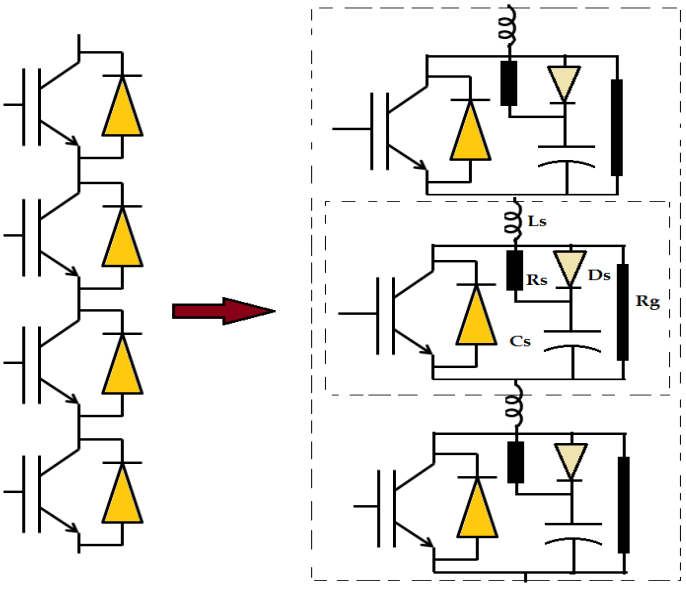

FIGURE 2.2: Static balancing by R_g, dynamic balancing by RCD snubber and L_s to limit di/dt [17, 19]

The series connection of IGBTs poses a number of contradictory design compromises [22]. For instance, if the switching speed of IGBTs is slowed down to achieve dynamic balancing by using snubbers but this tends to increase converter losses and reduces the switching(speed) frequency [22].

The high switching frequencies are ultimate requirement of conventional VSC to reduce the demand of costlier and huge size AC harmonic filters which improves the converter output power quality [16, 18, 24]. The converter is vulnerable to more switching losses at high switching frequencies [10, 24].

Electromagnetic interference (EMI) ia another design limitation which exists in power electronic circuits naturally and so that in two level VSCs also where simultaneous switching of devices at higher switching frequencies especially in the presence of high dv/dt values corresponds to greater amount of EMI, both conducted and radiated, and causes serious malfunction problems for the surrounding electronic and automatic control equipment [22, 25].

It can be controlled by reducing switching frequency but shows negative impact on conversion efficiency due to the naturally present low order harmonic content in crude AC output voltage waveform of conventional VSC [22].

Unacceptable quality factors, simultaneous switching of IGBT valves and unequal voltage distribution across IGBTs in off state are other key factors which put practical limitations to acquire any number of series connected IGBTs to make converter arm valves therefore an upper limit applies to opt how many IGBTs can be joined in converter arm valve [26].

The main shortcoming of using two-level VSC with series chain of IGBTs is that it costs additional circuitry to make it work properly at the expense of increased costs, power losses and contradictory design compromises [19, 22]. By the end all these efforts have nothing to do with the improvement of output voltage quality [7, 26]. The output voltage of conventional two-level VSC comprises only two

output voltage levels, having enormous amount of low order frequency harmonics [24]. To filter these harmonics expensive and voluminous AC harmonic filters are ultimate requirement [10].

2.3.2 Need For Bulky and Expensive Filters

To improve the output voltage quality the use of passive AC filters is mandatory but being extremely undesirable because of higher costs, large area consumption [21]. The fact that capacitive components generate reactive power to mitigate voltage harmonics is another drawback of passive AC harmonic filters which makes the VSC to absorb the reactive power for which VSC is not inherently designed, it puts limits for the VSC to perform 4-quadrant function therefore this reactive power is another leading disadvantage when passive harmonic filters are used [2, 24].

2.3.3 High Frequency Carrier PWM

The autonomous switching of IGBTs enables the use of high frequency pulse width modulation (PWM) for the switching purposes as it shifts the low frequency harmonic spectrum to higher frequencies which can be easily filtered out by using low cost and small size passive AC harmonic filters [16].

In any converter, the space contributed by filter is one-third of the area of the converter [18]. Thus PWM with carrier wave having frequency at least 40 times higher than fundamental frequency is necessary to assist a sound compromise regarding the size of passive AC harmonic filters but at the cost of increased switching losses [21].

The use of PWM is the fundamental technology for VSC regardless of the application setup. However it also brings three major by-products which includes; higher switching losses in converter arms, higher ripple in the converter output current and electromagnetic noise sources [25].

2.3.3.1 High Converter Losses

The PWM with higher switching frequencies $(1 - 2kHz)$ causes considerable amount of converter losses. The two level VSC losses, evaluated by IEC61803, constitute losses of approximately 1.6% for the total maximum rated capacity of HVDC transmission (per converter station) at rated loads. The no load losses are approximately 0.2% [27].

2.3.3.2 High dv/dt & Current Ripple

The hard switching at full DC-link voltage produces high values of dv/dt with high switching frequencies (1-2kHz). Another disadvantage is that it produces high ripple in current waveforms which may cause overheating of electronic circuitry and produces additional losses [27].

2.3.3.3 High EMI

The high speed switching of power semiconductor devices generates electromagnetic interference (EMI) [28]. EMI can be classified in to differential mode (DM) EMI and Common mode (CM) EMI [27].

The high frequency harmonics in line current are typical sources of DMEMI which is capable of contaminating the power grid which causes the electrical equipment to work in unsafe operational conditions and malfunctions the microprocessors and other automatic control devices [25].

The CMEMI is the noise which travels in the direction of high frequency common mode voltages. The current discharged by CM voltages with high values of dv/dt destroys the reliability and efficiency of electrical machines [25].

Figure 2.3 represents the design schematic of three phase high power conventional voltage source converter where each converter arm is composed of chain of series connected IGBTs and at output of the converter the bulky AC harmonic filters are

shown which are required to smooth out the crude AC waveform of conventional VSC.

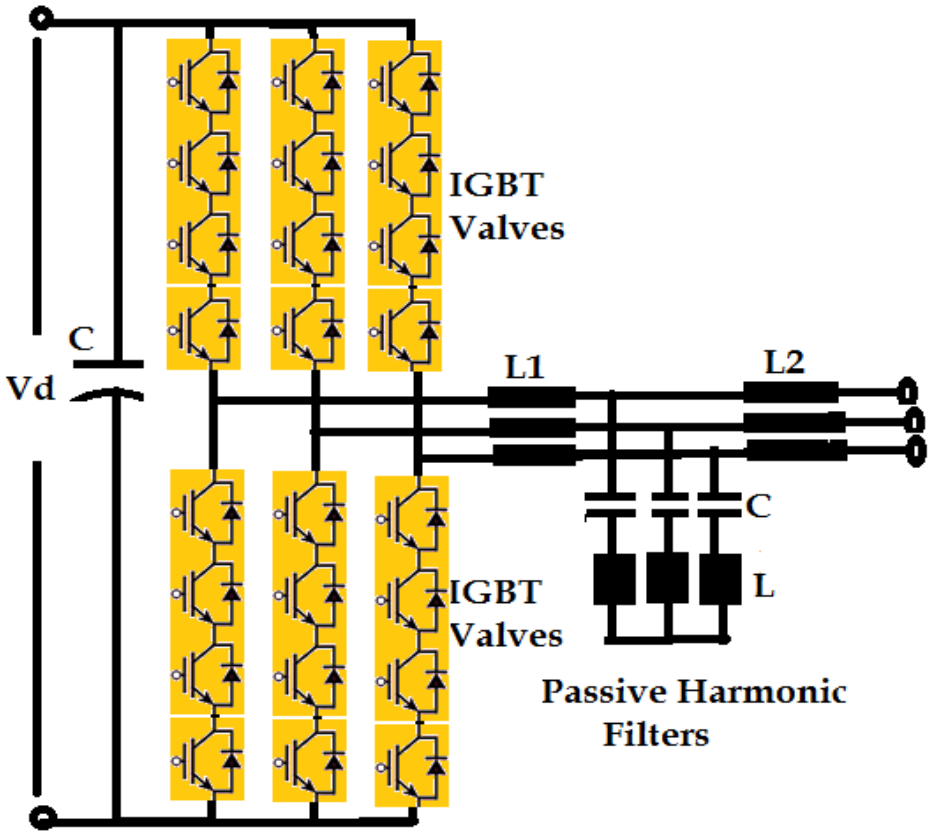

FIGURE 2.3: Arrangement of three phase 2L-VSC in HVDC [21]

2.4 Multilevel Concept

The requirement of AC harmonic filters is greatly reduced if the number of output voltage steps is increased in converter output voltage waveform which in turn decreases the voltage stress on each switching device due to lower dv/dt values. Besides, other multiple attributes can also be achieved by using multilevel voltage source converters [27].

Voltage waveform with more sinusoidal shape, offers lower levels of total harmonic distortion (THD) and lower harmonic content and hence reduces the requirement of massive and expensive AC harmonic filters [10]. The concept of multilevel

converter topology validates itself by producing minimum of three levels in its output voltage waveform [29].

The renowned basic multilevel VSC topologies (others may be their extended forms with some slight changes in structure) are Neutral point clamped multilevel converters (NPC) also known as diode clamped converters, Flying Capacitor multilevel converters (FC) also known as capacitor clamped multilevel converters, Cascaded H-Bridge multilevel converters (CHB) and modular multilevel converters (MMC/M2C) [7]. The basic structure and limitations of these multilevel converter topologies are discussed in the following subsections.

2.4.1 Neutral Point Clamped Multilevel Converter

Figure 2.4 shows schematic diagram for a three phase three-level neutral point clamped converter or simply NPC. It is also known as diode clamped multilevel converter topology. At output it produces three voltage levels $V_{dc}/2$, 0 and $-V_{dc}/2$ thus reducing the voltage stress by half of DC-link voltage per switching device [29].

It comprises of the similar structure as that of conventional VSC except having clamping diodes D_1 and D_2 in parallel which help to clamp the DC link voltage to half level. For an m-level NPC, it requires (m-1)×(m-2) clamping diodes and (m-1) DC-link capacitors where this number increases quadratically in m making it sufficiently infeasible to be utilized in high voltage direct current transmission system [16, 16, 29].

And if the PWM based NPC multilevel converter is used in high power high voltage applications than diode reverse recovery becomes a major design challenge [29].

The neutral point voltage balancing is required when the voltage levels increase more than three and it is very hard to achieve due to unequal distribution of losses between inner and outer devices because of different component ratings which makes it highly unsuitable to be used in HVDC systems [7, 30].

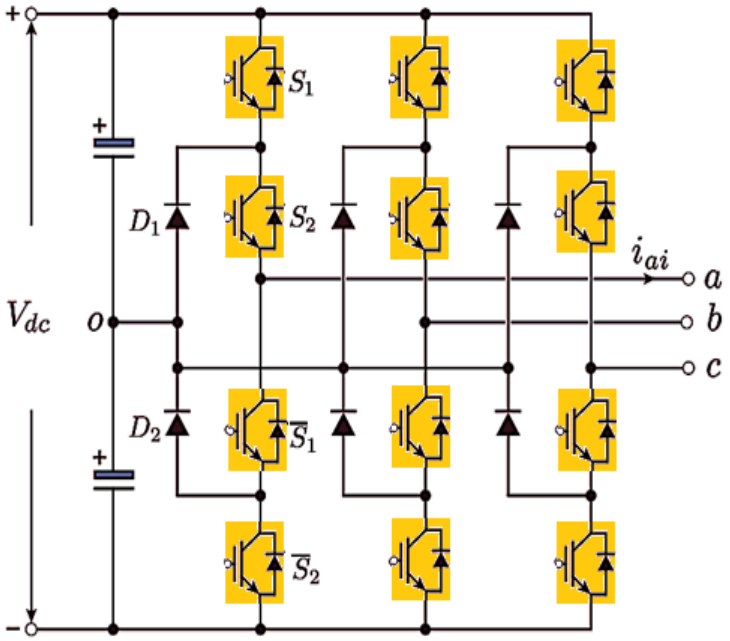

FIGURE 2.4: Arrangement of 3-Level NPC [7]

A few of the practical examples of NPC and its derivative A-NPC is presented in Table 2.2 where it is utilized by using series connection of IGBTs to reach higher operating voltage ratings in HVDC systems. This topology did not get much boom in comparison with standard conventional VSC HVDC.

TABLE 2.2: List of the NPC-VSC HVDC Commissioned Projects [14]

Name of Project	Year	Power Rating	Topology
Eagle Pass	2000	36MW	3-levelNPC
Murray-link	2002	220MW	3-level ANPC
Crosssound	2002	330MW	3-levelANPC

2.4.2 Flying Capacitor Multilevel Converters

Figure 2.5 shows the arrangement for 4-level three phase flying capacitor multilevel converter which comprises the similar structure to that of NPC with the only

exception that it uses flying capacitors instead of diodes [7]. This arrangement provides better ride through capabilities during outages but at the expense of increased circuit complexity [16].

For an m-level output voltage waveform, FC needs (m-1)×(m-2)/2 number of clamping capacitors in each phase along with additional (m-1) DC-link capacitors [29]. Increase in number of capacitors for higher voltage levels makes the converter structure less compact, bulky and expensive.

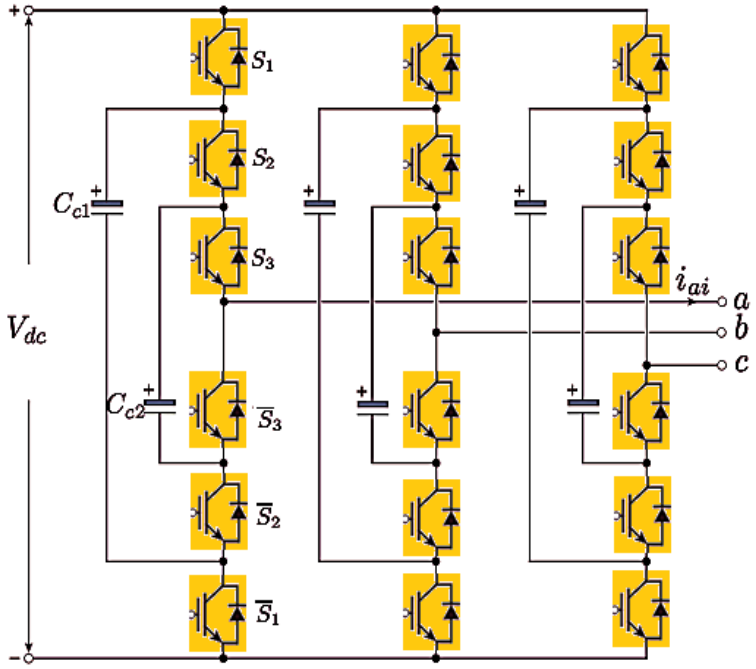

FIGURE 2.5: Arrangement of 4-Level FC [7]

Although FC provides more flexibility to produce multilevel output voltage waveform but at the same time it offers greater control complexity for capacitor voltage balancing [7].

The output voltage of FC is half of the DC link voltage which makes it unsuitable for HVDC applications therefore it has never been utilized in any of the HVDC projects practically [31]. However its practical use is found in medium to large motor drive applications [16].

2.4.3 Cascaded H-Bridge Multilevel Converters

Figure 2.6 provides the basic schematic of (2N+1) Level cascaded half bridge converter where each half bridge acts as a submodule and it is used in a modular structure which helps in synthesizing high quality staircase output voltage waveform.

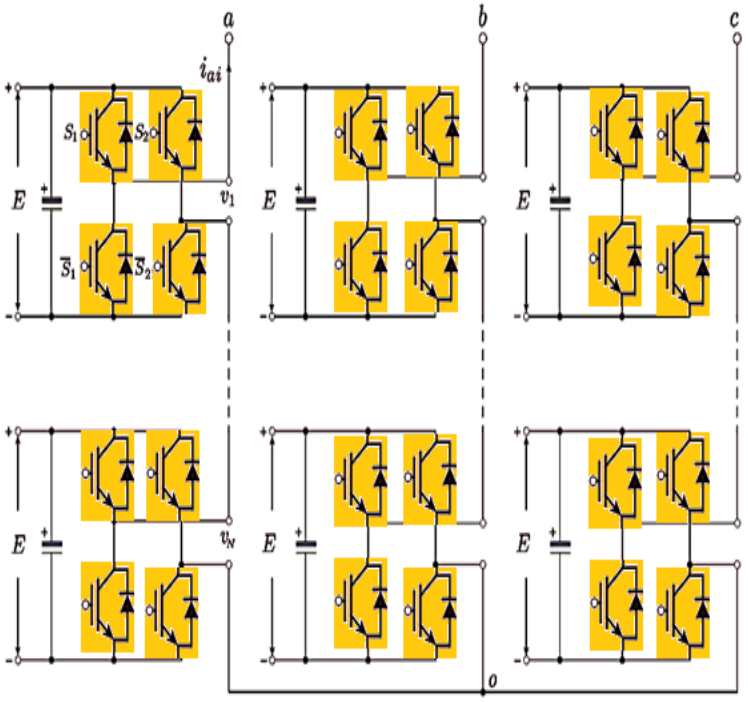

FIGURE 2.6: Arrangement of (N+1) Level CHB [7]

Each half bridge submodule comprises a DC-voltage source eliminating the need for extra clamping capacitors and diodes [16]. At the output of single half-bridge module three voltage levels are obtained i.e V_{dc}, 0 and -V_{dc} [16, 29].

Usually for an m level voltage waveform CHB requires (m-1)/2 number of half bridge modules with (m-1)/2 number of isolated DC-voltage sources. CHB topology requires least number of components as compared to other multilevel topologies to produce same output voltage level [16].

To utilize CHB in high power high voltage applications large number of isolated DC sources are required. This requirement can be fulfilled by using transformers

with special arrangement to provide phase shifted voltages for each H-bridge but this makes it highly voluminous, expensive and infeasible to be used in HVDC projects for large scale power transmission [7].

2.4.4 Modular Multilevel Converter

In 2003, the concept of modular multilevel converters was first introduced by Marquartd and commercialized for the first time by Siemens in 2010 in HVDC project [7, 10].

MMC proved itself the most promising contender to be utilized in HVDC applications because of its built in redundancy, modularity, scalability to any voltage levels, high standards of voltage quality, elimination of filter requirements, lower switching frequency and lower switching losses [10].

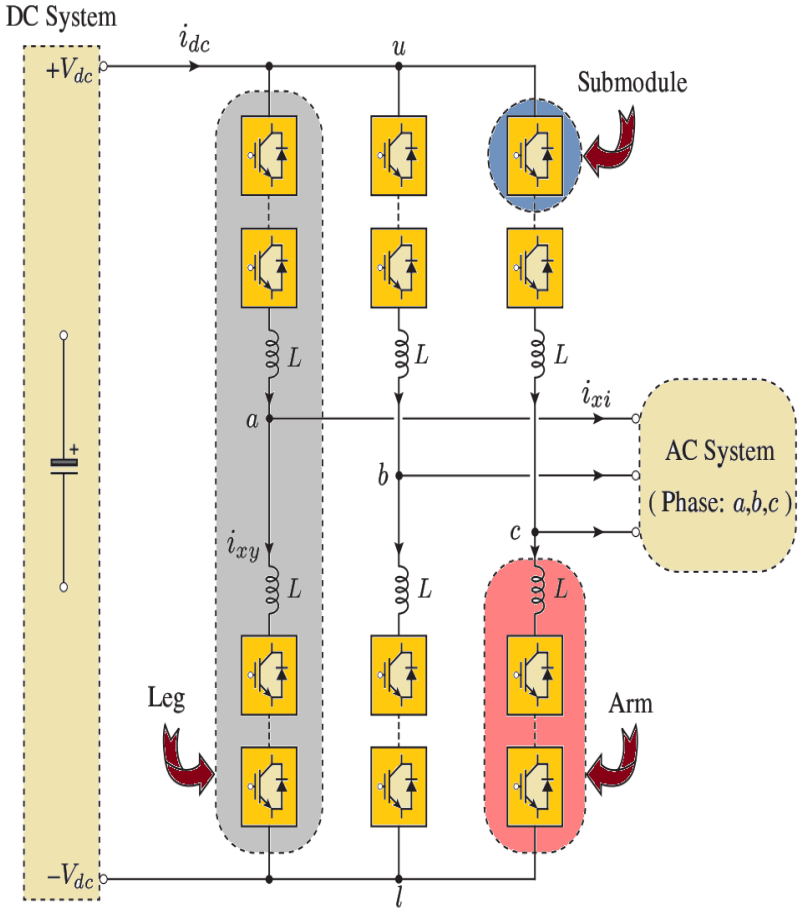

FIGURE 2.7: Three Phase Modular multilevel converter with basic Structure

The basic structure of three phase modular multilevel converter is presented in Figure 2.7 which includes three phase legs and each phase leg comprises two arms and in turn each arm comprises series connected sub modules and an arm reactor [7].

Most commonly MMC uses half-bridge topology presented in Figure 2.1 and full bridge sub modules used in cascaded H-bridge converter topology, in a series connection to reach the higher operating voltages.

2.4.4.1 A closer Look of Modular Multilevel Converter

Modular multilevel converter is a VSC topology which has proven itself a state of art because of its remarkable attributes which include higher design flexibility to reach high operating voltage ratings with ease [32].

It provides high efficiency because of lower converter losses, economical solution for high power quality and minimum filter requirements(negligible in some cases) [17, 21, 33]. The attributes of modular multilevel converter are briefly given below

1. Modularity [32]
2. Scalability [32]
3. Redundancy [17]
4. Lower Power Losses [33]
5. Reduced total harmonic distortion [33]
6. No Filter Requirements [16, 17, 33]
7. No critical capacitor voltage balancing [33]

2.4.5 Role of MMC HVDC in Current Scenario

Since MMC ′s first commercialization, it has got huge interest of vendors to invest on it because of its above mentioned attributes which make it highly suitable for

HVDC applications [34]. A few of completed and under construction MMC based HVDC projects are presented in Table 2.3.

TABLE 2.3: List of the MMC-VSC HVDC Commissioned Projects [10, 34]

Name of Project	Year	Power Rating	Topology
Trans Bay Cable	2010	400MW	MMC
Borwin2	2011	400MW	MMC
Skagerrak Pole4	2014	700MW	MMC
INELFE	2015	690MW	MMC
SylWin1	2015	864MW	MMC
HelWin1	2015	576MW	MMC
HelWin2	2015	690MW	MMC
BorWin2	2015	800MW	MMC
DolWin1	2015	800MW	MMC
Dolwin2	2016	916MW	MMC
DolWin3	2017	900MW	MMC
Caithness Moray	2018	1200MW	MMC
BorWin3	2019	900MW	MMC
ULTRANET	2019	2000MW	MMC
COBRAcable	2019	700MW	MMC
North Sea Link	2021	1400MW	MMC

2.5 Control of Grid Tied Voltage Source Converters

In [35], author discussed different types of current control strategies i.e. linear and non-linear current control of VSCs. As the nonlinear control is out of the scope of

this thesis, thus by focusing the linear control, this paper classifies linear control into different types i.e. stationary frame PI control, rotating frame PI control, state feedback control, model predictive control and deadbeat control.

The main disadvantage of the stationary frame PI control is that it has inherent tracking error i.e. this technique cannot provide zero steady state error. Whereas the model predictive control and dead beat control cannot afford to provide over current limit.

The rotating frame PI control provides zero steady state error but at the expense of dq0 transformations and an extra phase locked loop. The dynamics of current control loop in dq reference frame are fast and well damped.

In [26], the author presents two control techniques for the control of the active and reactive power in a grid tied voltage source converter which mainly include voltage mode control and current mode control.

The voltage mode control is an open loop control structure in which the real power is controlled by phase angle, and reactive power is controlled by amplitude of converter terminal voltage. This control strategy is being simpler and requires no loops. However as there is no loop closed on current therefore the system is always at the stake of over currents.

However current mode control discussed by [26] adopts the strategy in which the the converter AC side current is controlled through the converter terminal voltage using an inner control loop and later the active and reactive power are controlled by the angle and magnitude of converter AC side terminal current.

The above mentioned technique is also recognized as Vector control. It provides current regulation, protects VSC in overload conditions, provides robustness against system parametric changes (either VSC itself or AC side dynamics) and higher control accuracy.

In [10], voltage and current modulators are presented to control the output voltage and current of modular multilevel converter. The current modulators provide

fast dynamic response but it does not work with constant frequency therefore filtration is difficult with current modulators. The voltage modulator uses constant frequency, their filter requirements are simpler therefore these modulators are most commonly used.

2.6 Pulse Width Modulation

The choice for modulation is really important as there is a variety of modulation techniques being used for the switching of multilevel converters. The appropriate choice corresponds to lower total harmonic distortion values, lower losses and high quality voltage waveform [33].

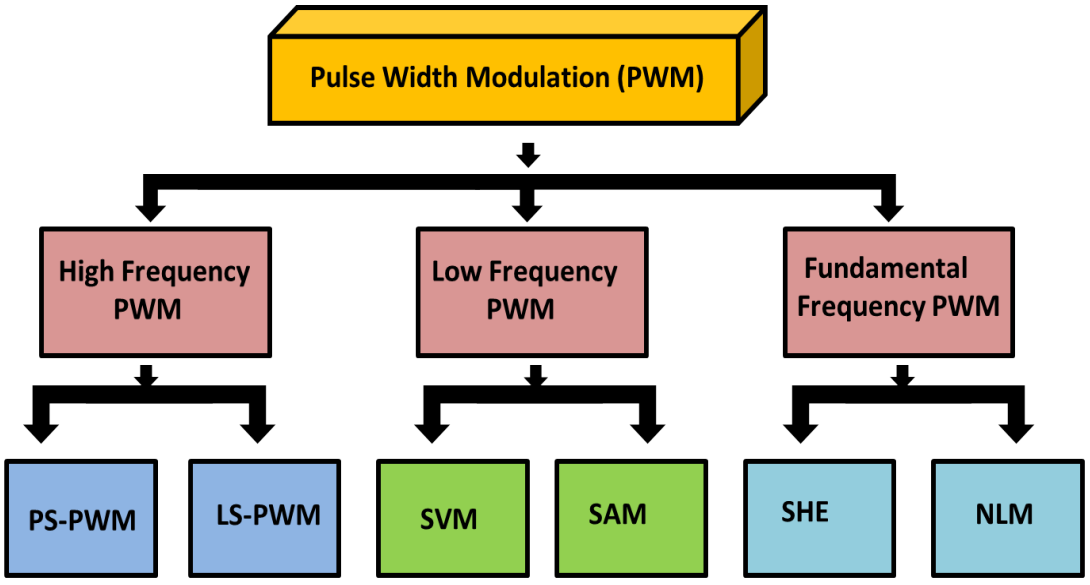

FIGURE 2.8: The classification of multilevel pulse width modulation on the basis of switching frequency [7]

In literature, different modulation techniques have been discussed for the switching of multilevel inverters. As this thesis is oriented towards the comparative performance analysis of modular multilevel converter and conventional VSC in HVDC therefore the modulation techniques are analyzed in context to their suitability for both of the converter topologies.

The modulation techniques for PWM based VSCs can be classified into three main categories; 1) high switching frequency carrier modulation, 2) low switching frequency carrier modulation and 3) fundamental or line frequency modulation [7].

Each of above mentioned three voltage modulation techniques are further classified into two subclasses as shown in Figure 2.8 and are discussed with their advantages and limitations subsequently

2.6.1 High Switching Frequency Carrier Modulation

This type of modulation technique is commonly known as sinusoidal pulse width modulation where a high frequency ($f_s w > 1$ or $2kHz$) carrier wave is compared to a low frequency reference signal and the switching pulses are generated at the corresponding intersecting instants [15].

For multilevel converters multiple carrier waveforms are generated i.e. for N level multilevel inverter, N carrier waveforms are generated and compared to the reference modulation signal and in this way N switching signals are generated for the switching of respective cells.

The sinusoidal pulse width modulation is categorized into two sub-categories Phase shifted carrier pulse width modulation (PS-PWM or PSC-PWM) and Level shifted carrier pulse width modulation (LSCPWM or LSPWM) [7].

PSPWM uses N carriers having same amplitude and frequency, where each carrier is phase displaced by some angle as shown in Figure 2.9 (a), therefore the switching of the each cell is phase delayed by the phase difference present in each carrier [36].

This enables PS-PWM to allow the natural balancing of capacitor voltages at high switching frequencies [7]. It allows equal sharing of semiconductor stress whereas power handling capability is evenly distributed across each submodule [37]. It also minimizes the current ripple at DC bus and provides better output voltage waveform hence reducing the filter requirement [38, 39].

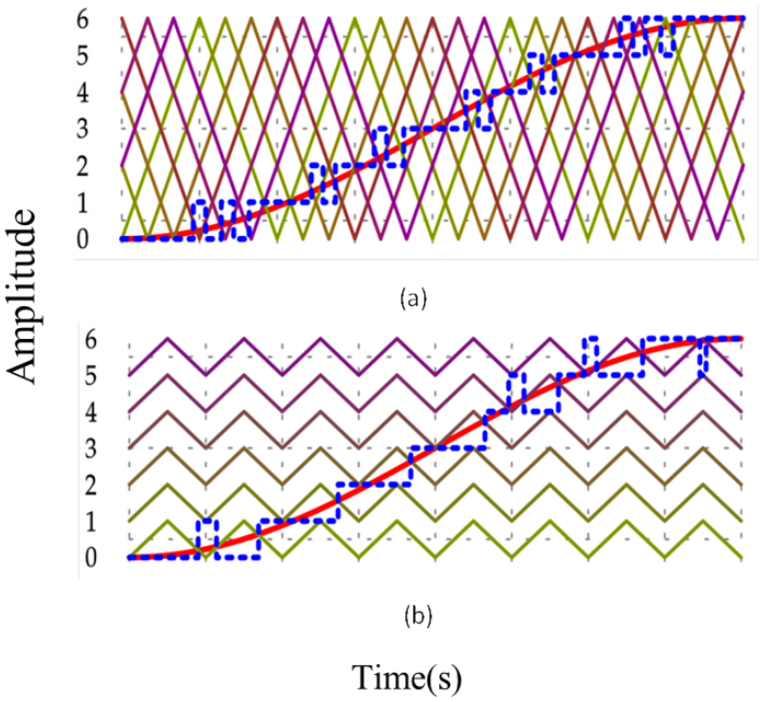

FIGURE 2.9: SPWM for multilevel Inverters
(a) PSPWM (b) LSPWM [37]

Figure 2.9 (b) shows LSPWM technique and it can be visualized that is quite similar to that of PSPWM with the only difference that its carriers are level shifted i.e. each carrier is shifted by some offset value from the zero reference level [40].

LSPWM is not considered a better option for the switching of MMC because the power losses among submodules are unevenly distributed [41]. It also causes large circulating currents in the MMC arms due to uneven distribution of capacitor voltage ripple in each submodule [42, 43].

2.6.2 Low Switching Frequency Modulation

The modulation technique which uses low frequency modulation ($100 < f_s w < 1000$), falls under this category [7]. It has two categories; 1) sampled average modulation (SAM) and 2) space vector modulation (SVM) as shown in Figure 2.8.

SAM directly controls the output phase voltages while the line voltages are controlled indirectly. Conversely, SVM allows the direct control of line voltages whereas the phase voltages are controlled indirectly. The three phase equivalent of both techniques is almost similar with the only difference of SAM distributes the zero vectors unequally at the start and end of switching sequence [7].

Hence it generates highest levels of harmonic distortion in the output voltage. It can be easily expandable for MMC with any number of converter arm submodules. Figure 2.10 (a) shows the operation of sampled average modulation.

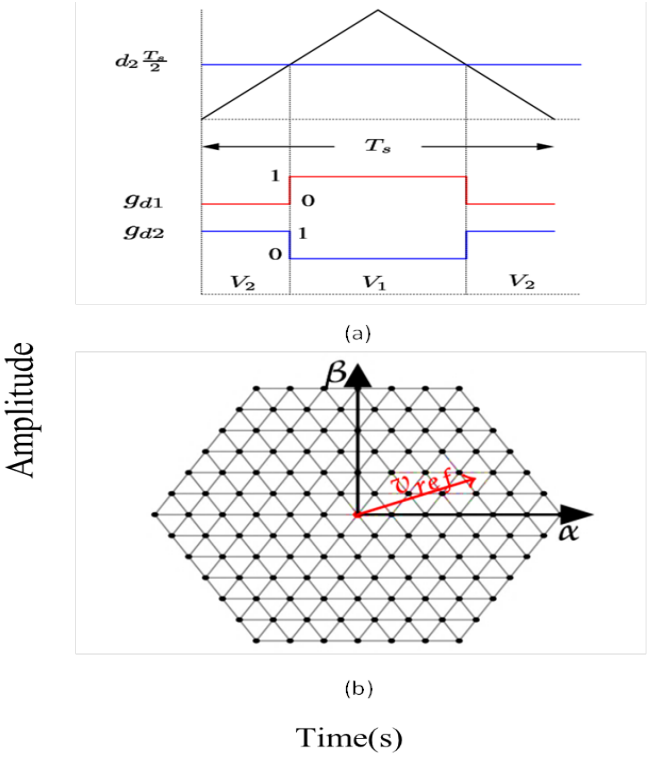

FIGURE 2.10: Low frequency modulation for multilevel Inverters (a) SAM (b) SVM [37]

On the other hand, SVM which can be shown in Figure 2.10 (b), shows flexibility to choose best vectors for switching of submodules in order to enhance output voltage harmonics, better utilization of DC bus, regulation of magnitudes of common mode voltages [7] etc.

However, despite of the fact that it provides so many advantages it cannot be easily extend able to any number of submodules in MMC. For an m-level MMC,

m^3 vectors are needed for the switching of submodules therefore MMC with higher number of submodules ($N > 20$) restricts the use of SVM [29].

The computational complexity at modulation stage due to alpha beta transformations, use of look up tables and trigonometric functions makes its use complicated for higher voltage levels in order to operate in high voltage high power applications [37, 44].

2.6.3 Fundamental Switching Frequency Modulation

Staircase modulation or commonly known as nearest level modulation (NLM) and simple harmonic elimination (SHE) use fundamental frequency for the switching of submodules, therefore these technique fall under the category of fundamental switching frequency modulation [7].

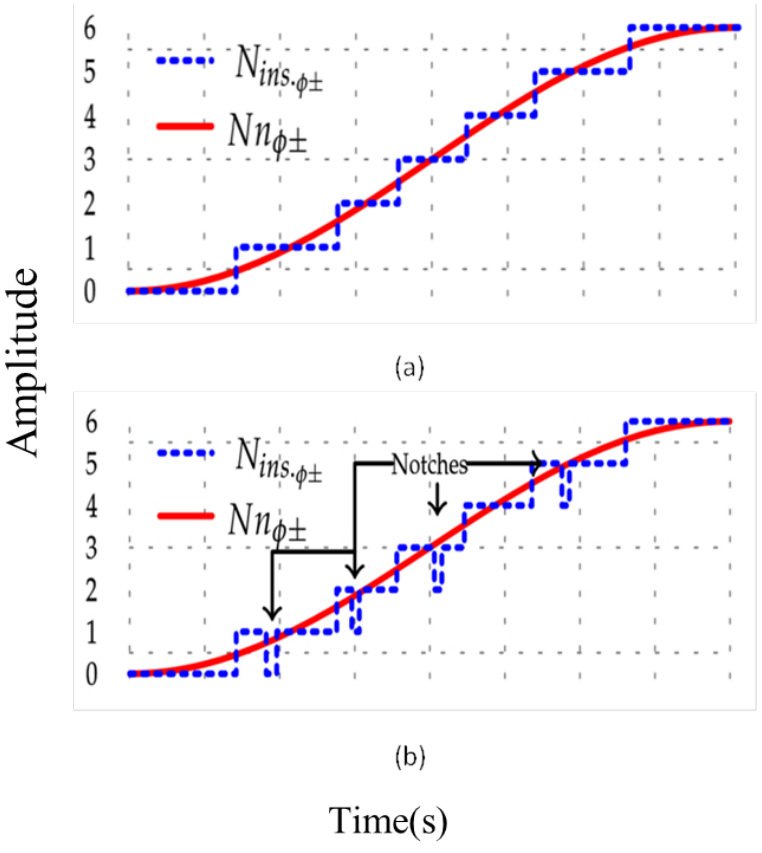

FIGURE 2.11: Fundamental frequency modulation for multilevel Inverters (a) NLM (b) SHE [37]

NLM uses a single staircase signal and compares it with the reference to generate the switching signal for each submodule in MMC as shown in Figure 2.11 (a) [37]. The drawback of NLM is that it demands high sampling frequency and generates poor quality waveforms when used for MMC with lower number of submodules.

Generally, for better quality output voltages, NLM should be used with MMC having submodules greater than 100 or 200 [7, 45, 46].

SHE offers amazing quality of output voltage by having tight control over output voltage harmonics while keeping the switching frequency equal to line frequency [15]. Its drawback includes the off line manipulation of switching angles for which large nonlinear equations are supposed to be solved [40].

The number of angles required for switching, drastically increases as the number of levels in the MMC output voltage increases and thus making it difficult to attain solution for such a large figure of switching angles [7]. The basic structural overview of SHE that how it works is presented in Figure 2.10 (b).

2.7 Comparative Analysis of Conventional VSC and Multilevel-VSC in Literature

[47] is only oriented towards total harmonic distortion analysis of conventional VSC and three level neutral point clamped converter in an HVDC based environment.

In [48], the comparative analysis of 2-level VSC and MMC is presented in HVDC with grid frequency support, The discussion is more tilted to provide the comparison of control of MMC and two-level VSC based HVDC system in the presence of frequency support provided by wind power plants during disturbances in grid frequency. However it does not provide the output voltage quality comparison.

In [49], the comparative analysis between two-level VSC and three level multiple topologies like NPC, FC and CHB and concludes that the 3-level converter topology, having more sinusoidal output voltage waveform is, more efficient than the

conventional 2-level VSC. The author also touches the cost, efficiency and filtration requirements. But this study does not provide any idea regarding their use in high power high voltage applications.

In [50], the author provides mathematical model and control structure design for conventional VSC and MMC but does not addresses the output power quality of both systems.

In [17], different multilevel converter topologies are compared to analyze their suitability with regards to be utilized in a specific 10MW, 100kV transformer less wind generator setup. It does not provide analysis of control structure for modular multilevel converters

[16] provides the comparison of different converter topologies on the basis of converter output voltage quality while using two different modulation schemes. This paper does not touch the control and modeling side of converters.

2.8 Gap Analysis

Thyristor based LCC technology is quite mature, it is even currently being used in HVDC projects for the transmission of large power over long distances, however due to the limitations offered by LCC, 1990's VSC technology got popularity with the arrival of IGBTs i.e. self commutating devices which was first commercialized in 1997. Since then two level VSC is taking part in the race of HVDC commercialized projects to transmit high power over long distances but still it is running through developmental changes to meet higher power demands.

Due to higher control flexibility of VSC technology, it is greatly used in HVDC applications but it always made to make a compromise on bulky, expensive filters and endured the additional complexities resulting in response to series connection of IGBTs to reach high power high voltage operating ratings in HVDC system.Along side to achieve good quality output voltage and current waveforms conventional VSC uses high switching frequencies which endures additional converter losses

upto 1.7% which were only 0.2% in LLC technology [27]. Therefore there was always a need for a converter which not only provides higher control flexibility but inherently provides high quality output voltage with low switching frequencies which in turn reduces the demand for voluminous and expensive filters and incorporates lower converter losses as well.

Modular multilevel, being modular and scalable to achieve any power level theoretically has been used in different medium to low power applications. In 2010 when it was first commercialized by Siemens, since then it is becoming an outmanoeuvre and being casted in many commercialized HVDC projects which can be pictured through Table.2.3.

This work is subjected towards the detailed and comprehensive analysis of modular multilevel converter on the basis of output power quality, active and reactive power control performance and complexity, filter requirements, losses, costs and design feasibility by comparing it standard high power conventional 2-level VSC which is being used in HVDC projects commercially since 1997.

Although lots of work is done on the performance investigation of newly developing modular multilevel converter topology by making comparative analysis with conventional VSC but there is not even a single literature found which addresses all the performance aspects of MMC with respect to its use in high power high voltage applications. This work is an attempt to fill this gap by providing comprehensive details on the basis of comparative analysis between MMC and conventional VSC when used in high voltage high power applications.

2.9 Problem Statement

To design an efficient modular multilevel converter model which abstains the limitations and performance hindrances offered by standard high power conventional VSC, by providing high quality output voltage waveform with reduced filtration

requirements, losses, costs and maintained control flexibility towards the independent control of active and reactive power at Pcc in a grid connected HVDC converter station environment.

2.10 Chapter Summary

This chapter investigated the details regarding the problems of high power conventional VSC and fundamental multilevel VSC topologies with respect to their use in HVDC from literature. Different literature work is skimmed through for analyzing the modulation techniques , control design and performance comparison of conventional VSC and modular multilevel converter VSC. In the end the gap of this work with the previously done work, which is identified through literature, is provided and based on the Gap the problem statement for this thesis is described.

Chapter 3

System Modeling

3.1 Introduction

This chapter gives comprehensive details involving the mathematical modeling of AC side dynamics of conventional VSC and MMC when tied to a grid and later the simulation models for both converter topologies are presented in Matlab/Simulink 2016b environment. In the end section of this chapter the model designed for the grid is also presented and discussed.

3.2 Conventional Two-Level VSC

3.2.1 Introduction

The conventional two-level three phase VSC as its name indicates, produces an output voltage having two levels i.e. $+Vdc/2$ and $-Vdc/2$ at its output phases a, b and c with respect to the supply mid-point having 0V voltage [15, 51].

Figure 3.1 represents the general configuration of three-phase two-level VSC which comprises three single phase half bridge converters connected parallel to each other [26]. Each phase leg constitutes two arms and every arm has a switching device i.e.

integrated gate bipolar transistor (IGBT) with anti parallel freewheeling diodes served to allow the passage of reversed current [15, 51].

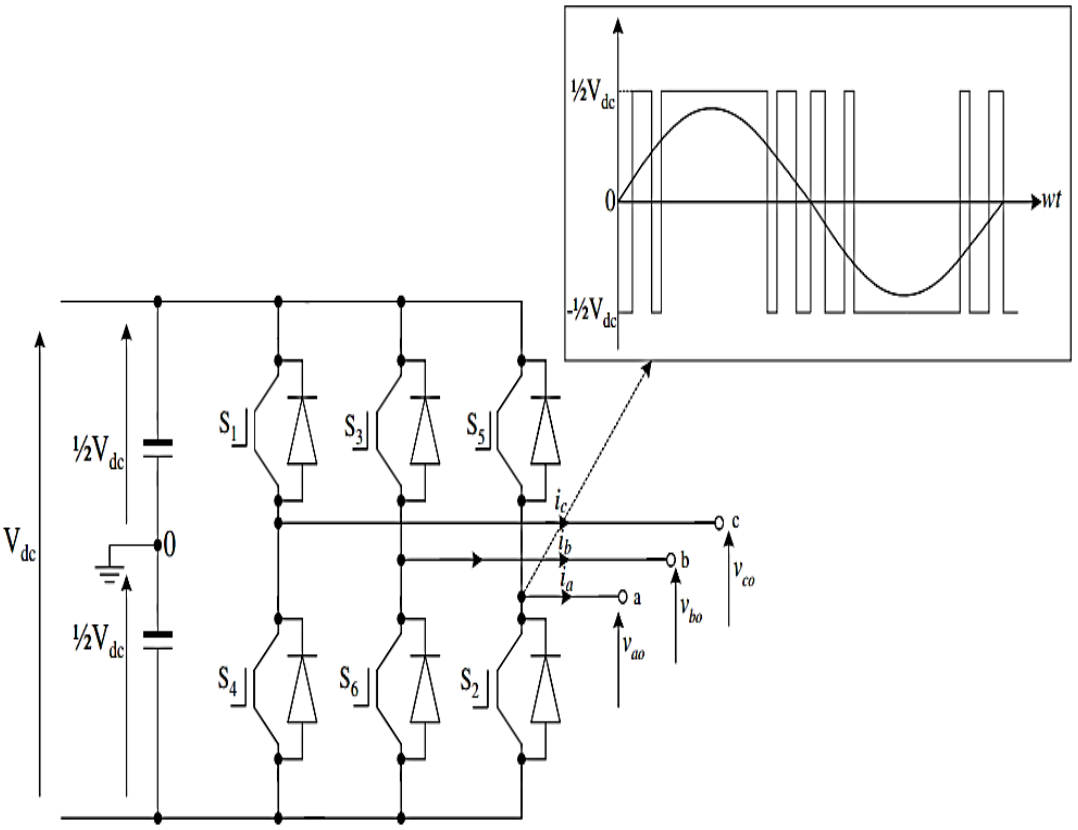

FIGURE 3.1: Three Phase two-level VSC with output phase voltage [15].

3.2.2 Fundamentals of Two-Level VSC

As the single phase half bridge converter is the fundamental structure for three-phase two-level VSC system therefore for the sake of simplicity this section considers single phase half bridge converter topology to understand the working of conventional VSC and development of mathematical model [26].

Later the equations are extended for three-phase full bridge VSC. Figure 3.2 shows the basic structure for the single phase half bridge converter connected to the grid through a coupling impedance. It comprises two switches namely 1 for upper and 4 for lower arm respectively.

Each switch cell contains semiconductor switching devices Q_1 and Q_4 and an anti parallel freewheeling diode D_1 and D_4 respectively. The positive current flows through collector to emitter in a transistor whereas the current flowing from anode to cathode is assumed positive in the diode. The currentsi_p and i_n represent the current through the upper and lower switches respectively.

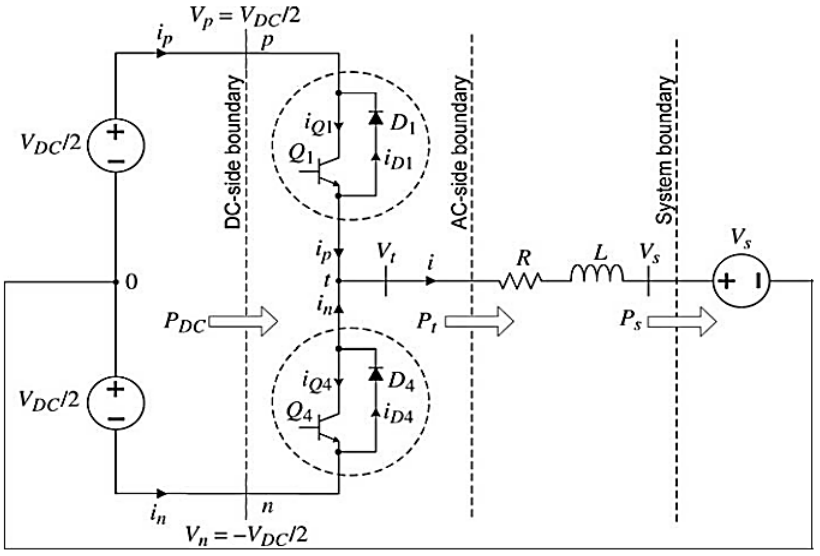

FIGURE 3.2: Single phase half bridge converter tied to a grid through phase reactance[26].

The point p and n represent the dc-side boundary where the DC Power P_{dc} is delivered to the converter. The terminal t represents the AC side boundary where the DC power is being converted into the AC power P_t. The terminal s represents the system boundary where the AC power is being transferred to the grid or some other system.

V_s represents the source voltage of grid, whereas R and L represent the equivalent reactance offered by the converter, line impedance and coupling transformer(if used), which provides an interface between converter and grid.

Two DC voltage sources, $Vdc/2$ are split by a common mid-point with zero voltage, providing reference for the electrical circuit, supply DC power to the converter station. The negative terminal of V_s is connected to the mid-point of DC voltage sources to complete the circuit [26].

3.2.3 Working Principles

Pulse width modulation (PWM) is used for the switching of the half bridge converter switches. There are number of different techniques (with further variations) used for the switching purposes in two-level VSC but the basic techniques follow space vector modulation, selective harmonic elimination and sinusoidal pulse width modulation [15].

This thesis uses sinusoidal pulse width modulation for its ease and simplicity for use [51]. It uses a high frequency carrier and compares it to the low frequency modulation signal, the instants where modulating signal crosses the carrier signal defines the switching instants for the switching devices.

Those instants where the amplitude of carrier is higher than the modulating signal a switch off command is issued for Q_1 whereas when the modulating signal gets higher amplitude than the carrier wave, switch on command is issued for Q_1 [26]. The lower switch Q_4 switches in a complementary fashion to that of upper switch cell Q_1.The amplitude of carrier fluctuates between 1 and -1 over the time period of T_s.

The switching function is defined as follows [26];

$$S(t) = \{1; if the switch is in conduction mode$$

$$0; if the switch is in blocking mode\}$$

This implies that

$$S_1(t) + S_4(t) = 1$$

Where $S_1(t)$ defines the switching function for Q_1 and $S_4(t)$ defines the switching function for Q_4.

Figure 3.3 shows the basic operation of pulse width modulation which is used to carry out the commutation of switching devices in conventional VSC.

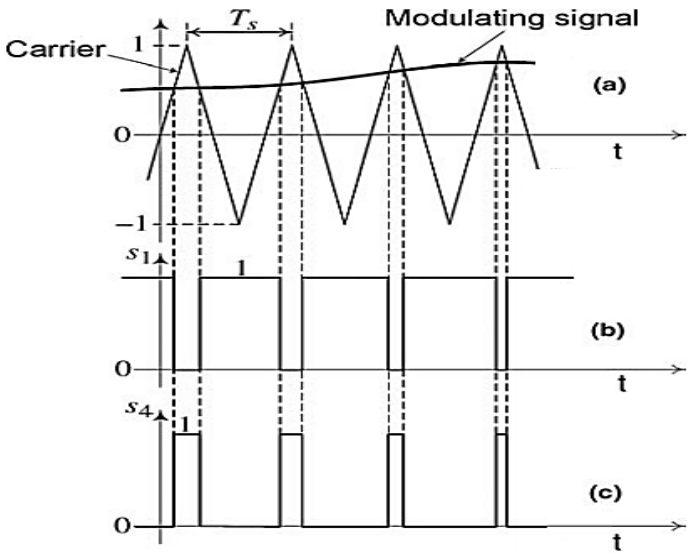

FIGURE 3.3: Fundamental operation of pulse width modulation used for the switching of converter switching devices.[26].

3.2.4 Mathematical Modeling of AC Dynamics Of Two-Level VSC

In order to develop the converter switched model and construct the waveforms for the two-level VSC, some streamline assumptions are made as follows [26].

1. Every switch behaves as a short circuit during conduction state
2. Each switch behaves as an open circuit in blocking state.
3. The transistors do not possess turn-off tailing current.
4. The diodes do not possess turn-off reverse recovery current.
5. Transitions from on state to off state, and vice versa, occur immediately

The switching sequences and another factor which greatly influence the converter operation is the direction of the converter output current i_t. Therefore the converter performs in a different manner for the different directions of current. For instance, for $i > 0$ assume that the switching sequence is $S_1 = 0$ and $S_4 = 1$ therefore Q_1 is off and Q_4 is on.

In this condition i can neither pass through D_1 nor from Q_4 for being positive in direction therefore its passage becomes possible through D_4 and thus the terminal voltage V_t becomes equal to -$Vdc/2$. Now if $S_1 = 1$ and $S_4 = 0$, this surely implies that Q_1 is on and Q_4 is off thus the positive current flows through Q_1 and $V_t = Vdc/2$. Therefore Q_4 and D_1 play no role in the operation of the converter [26].

Now if $i < 0$ and suppose the switching sequence is $S_1 = 0$ and $S_4 = 1$ than Q_1 is off and Q_4 is on then the current passes through Q_4 and V_t =-$Vdc/2$ and when $S_1 = 1$ and $S_4 = 0$ than Q_1 is on and Q_4 is off and current being negative flows through D_1. Therefore it shows that Q_1 and D_4 plays no role in the converter operation during negative direction of current.

The duration when the Q_1 or Q_4 is on, is called the switch's respective duty cycle and it is represented by d. Figure 3.4 shows that the operation of converter is greatly affected by the direction of current but the converter output voltage and current does not rely on current's direction either it is positive or negative.

For example when $S_1 = 1$, Q_1 is on and Q_4 is off thus $V_t = Vdc/2$, the current through upper switch $i_p = i$, and current through lower switch$i_n = 0$. Alternatively, when $S_4 = 1$, Q_4 is on and Q_4 is off consequently V_t =-$Vdc/2$ and $i_n = i$ and $i_p = 0$ and this condition holds true for both directions of current either positive or negative.

The entire above mentioned discussion is summed up in Figure 3.4. Relying on the foregoing discussion, the two level half bridge converter operation can be mathematically summed up by the following set of equations [26].

$$S_1(t) + S_2(t) = 1 \tag{3.1}$$

$$V_t(t) = \frac{V_{dc}}{2} \times S_1(t) - \frac{V_{dc}}{2} \times S_4(t) \tag{3.2}$$

$$I_p(t) = i \times S_1(t) \tag{3.3}$$

$$I_n(t) = i \times S_4(t) \tag{3.4}$$

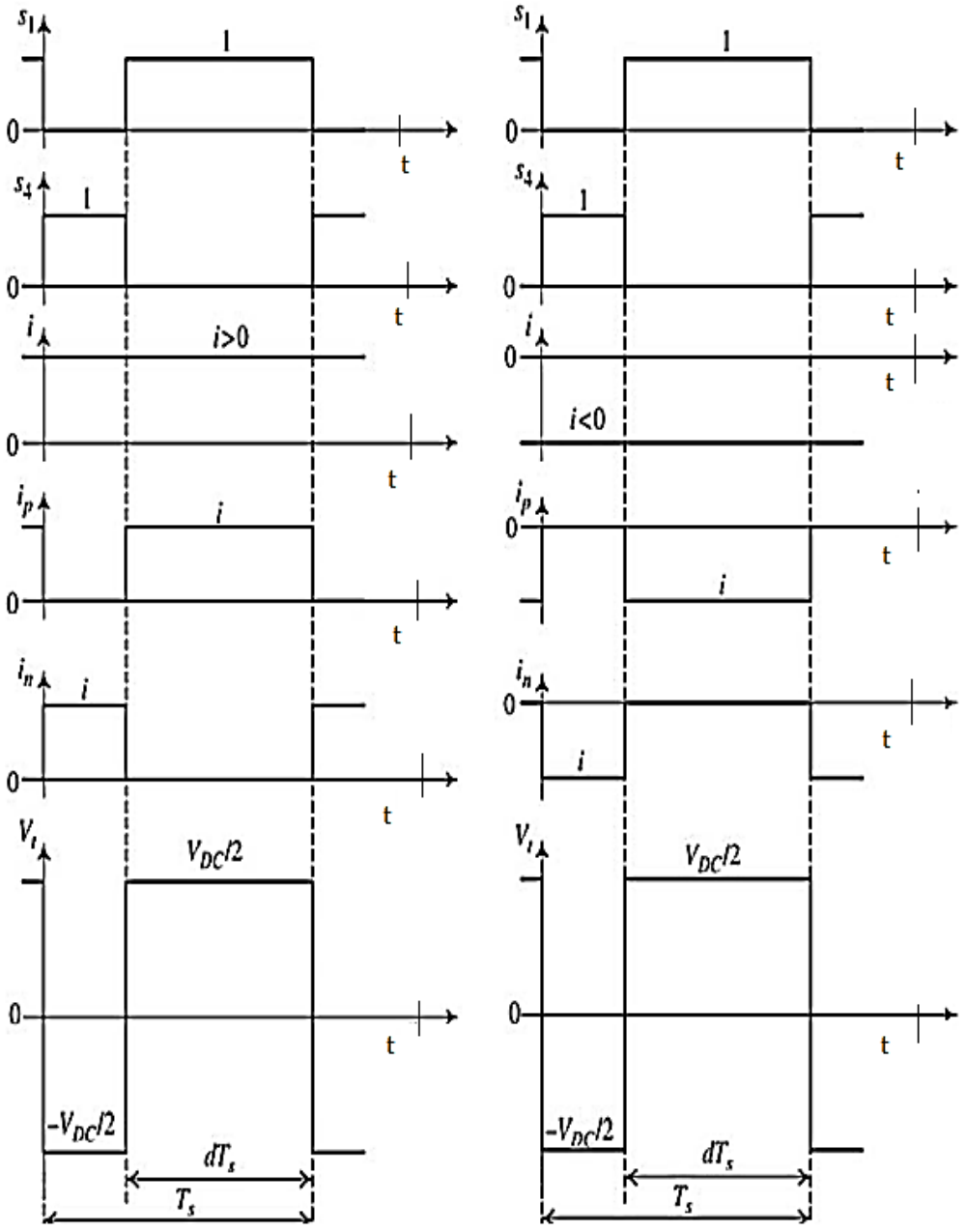

FIGURE 3.4: Waveforms for Half bridge converter for positive direction and negative direction of AC current respectively [26]

The equations from 3.1 to 3.4 represent the switched model of half bridge converter where $V_t(t)$ is the converter output terminal voltage and it is a continuous periodic signal. The half bridge converter switched model is represented in Figure 3.5.

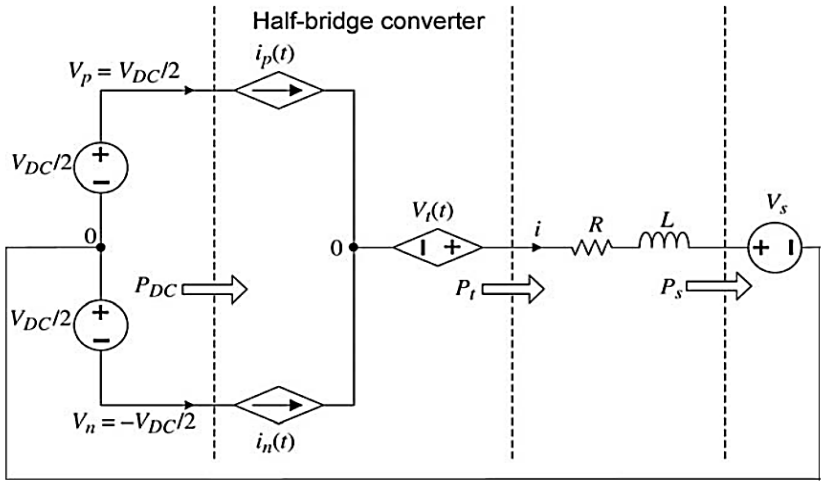

FIGURE 3.5: Switched equivalent model of half bridge converter [26]

From Figure 3.5 the AC side dynamics of two-level grid tied VSC are given in 3.5

$$L\frac{d}{dt}i(t) + Ri(t) = V_t(t) - V_s \tag{3.5}$$

The switched models are good to analyze the instantaneous current and voltage values provided the switching functions but they result into high frequency values of the instantaneous output current and voltages which are not desirable in control systems, because controllers are low pass filters and they are responsive towards the low frequency averaged values of the variables [26]. Therefore an averaging operator is applied on the switched model which is defined as

$$\overline{\mathrm{x}}(t) = \frac{1}{T_s}\int_{t-T_s}^{t} x(t) \tag{3.6}$$

In 3.6 $x(t)$ represents the variable and $\overline{\mathrm{x}}(t)$ represents the average of that specific variable and if this operator is applied to 3.3 and 3.4 we get

$$\overline{\mathrm{S}_1}(t) = d \tag{3.7}$$

$$\overline{\mathrm{S}_4}(t) = (1-d) \tag{3.8}$$

If the carrier frequency is chosen very high as compared to the modulating signal, the average values of current $\bar{\mathrm{i}}$ and DC voltage $\overline{\mathrm{V}}_dc/2$ are considered constant for

one switching cycle [26]. Thus taking averages on both sides from equation 3.2 to 3.4 and substituting 3.7 and 3.8 we get

$$\overline{\mathrm{V}}_(t) = \frac{V_{dc}}{2}(2d-1) \tag{3.9}$$

$$\bar{\mathrm{i}}_p = id \tag{3.10}$$

$$\bar{\mathrm{i}}_n = (1-d)i \tag{3.11}$$

The duty cycle d can vary between 0 and 1, and if sinusoidal pulse width modulation is used the term $2d-1$ is replaced by m where m is the reference modulation signal. When d varies from 0 to 1, m varies from -1 to 1 [40]. The equations 3.9 to 3.11 can be rewritten as

$$\overline{\mathrm{V}}_(t) = \frac{V_{dc}}{2}m \tag{3.12}$$

$$\bar{\mathrm{i}}_p = i\frac{(1+m)}{2} \tag{3.13}$$

$$\bar{\mathrm{i}}_n = i\frac{(1-m)}{2} \tag{3.14}$$

As m changes from -1 to 1 the terminal voltage V_t changes from $V_{dc}/2$to $+V_{dc}/2$. The equation 3.5 can be extended from single phase half bridge converter to three phase full bridge converter while taking the AC side dynamics into consideration. The three phase switched average model of two-level VSC is represented by 3.15 to 3.17 as follows [7, 26].

$$L\frac{d}{dt}i_{abc}(t) + Ri_{abc}(t) = V_{tabc}(t) - V_{sabc} \tag{3.15}$$

$$V_{tabc} = \frac{V_{dc}}{2}m_{abc}(t) \tag{3.16}$$

$$m_{abc}(t) = \hat{m}\cos((\omega t + \theta) + \phi) \tag{3.17}$$

Where $\hat{m}$ is the modulation index and its value varies from 0 to 1 [51], ω is the fundamental line frequency in radians, θ is some initial phase angle and ϕ is the angle between each phase in a three phase AC system [26].

3.3 Matlab/Simulink Model for Three Phase Two-Level Grid Tied VSC

The Simulink model developed for the analysis of conventional two-level three phase grid tied VSC is based on the mathematical model developed in the equations 3.15 to 3.17.

The Matlab/Simulink model for two-level three phase grid tied VSC is presented in Figure 3.6. It comprises two split DC voltage sources $V_{dc}/2$ of 50kV having a common grounded mid-point taken as reference. Thus the total DC link voltage at the input is V_{dc} =100kV.

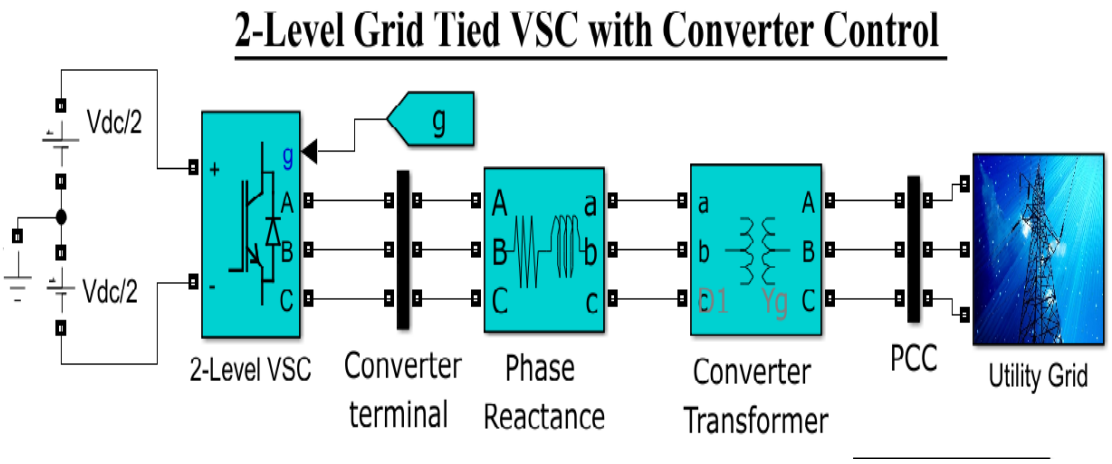

FIGURE 3.6: Simulation Model of two-level Grid tied VSC in Simulink

The two-level three phase grid tied VSC model is simulated on the basis of mathematical model developed in section 3.2.4. For software based modeling Matlab/Simulink 2016b environment was chosen.

The block under the title "Universal Bridge" was chosen from Simscape Simpower library for realization of simulation model of two level three phase VSC and its picture is shown in Figure 3.7. The option of IGBTs/Diodes is chosen to be used as the switching devices.

The Universal Bridge has three input terminals; the two of the input terminals are connected to the two DC voltage sources respectively which are equal to half of

the full DC link voltage having a ground connected at the midpoint. The midpoint is chosen as a reference for the entire electrical circuit model.

The third input terminal is specified for the gating signals used to control the semiconductor switching devices i.e. the IGBTs. At output it provides three phase two-level voltage waveforms whose magnitude varies from -50kV to +50kV as the switching signal varies from -1 to +1.

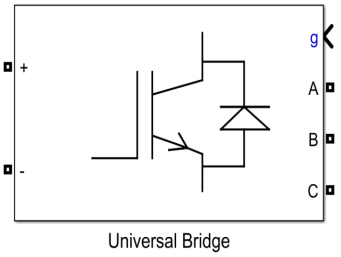

FIGURE 3.7: Universal Bridge for two-level VSC Simulation model in Matlab/Simulink 2016b

The parameters chosen for two-level VSC are represented in Table 3.1

TABLE 3.1: Specifications of two-level Three-Phase VSC [52]

Description	Symbol	Value
Full Dc link Voltage	V_{dc}	$100kV$
Fundamental frequency	f	$50Hz$
Switching frequency	f_{sw}	$1650Hz$
Output phase voltage	V_a	$50kV$
Modulation Index	$\hat{m}$	0.85
Frequency modulation ratio	m_f	33
Number of Levels in V_a	N	2

From Figure 3.6 the converter output terminal t represents the VI-measurement block where the converter three-phase output voltages and currents are measured.

The phase reactor block is used to control the flow of active and reactive power by regulating the current passage through them. It is also used as AC harmonic filter which filters out the high frequency harmonics from the converter output current.

The equivalent resistance R offered by the phase reactor is chosen 0.04Ω whereas the reactance L is chosen equal to $1.29H$. Next to the phase reactor, the Simulink model uses a coupling transformer connected between the converter and AC grid. It provides coupling interface between the converter station and grid by transforming the high grid voltages to the lower voltage levels which are suitable for the converter operation.

This simulation model uses $Y_g\Delta$ transformer configuration to provide interface between converter and AC grid. The Δ configuration allows the circulation of third harmonic currents with in the transformer and does not allow its flow to the supply line, it is not suitable to be used on high voltage transmission sides because it requires higher insulation costs therefore it is used on secondary side or on converter side [53].

The converter switching frequency is chosen to be 33×50 =1650Hz because for hard switched converters it is limited to below 1kHz whereas those topologies which are soft switched they can be switched as high as 2kHz however it renders more switching losses along with more power losses due to additional equipments to slow down the switching speed [23].

Therefore, this thesis considers the switching frequency f_{sw} =1650Hz as high switching frequency by considering the limitations of hard and soft switched converters especially for conventional VSC which is being switched at full DC-link voltage of 100kV.

The Y/star configuration has an important feature that it requires less insulation inside the transformer which makes it highly suitable to be used on high voltages therefore it is used on the primary side [54].

The AC system is modeled using a three phase balanced voltage source having nominal AC voltage (V_{sabc}) of $220kV(r.m.s)$ and $50Hz$ nominal AC frequency f. The transmission parameters of the AC system are provided in Table 3.2.

TABLE 3.2: Specifications of Simulink Model for two-level Three-Phase VSC [52]

Description	Symbol	Vlue
Phase reactance	$R + jL$	$0.04\Omega + j1.29H$
Transformer primary voltage	V_{pri}	$220kV$
Transformer secondary voltage	V_{sec}	$52kV$
Transformer leakage reactance	$R_x + jL_x$	$0.0048\Omega + 0.03H$
Transformer turn ratio	K	0.85
Ac source voltage	V_s	$220kV$
Nominal AC source frequency	f	$50Hz$
Sampling time for power GUI	T_s	$6.06e^{-6}$s
Sampling frequency	f_s	3300Hz

3.4 Modular Multilevel Converter

3.4.1 Introduction

The basic configuration of single phase $N + 1$ level modular multilevel converter (MMC) is presented in Figure 3.8. MMC as its name indicates that it is a multilevel converter topology which comprises two arms i.e. an upper arm and a lower arm per leg/phase. Each arm consists of N series connected submodules (SM) which corresponds to $N + 1$ voltage levels or steps in the output line to neutral voltage waveform [7].

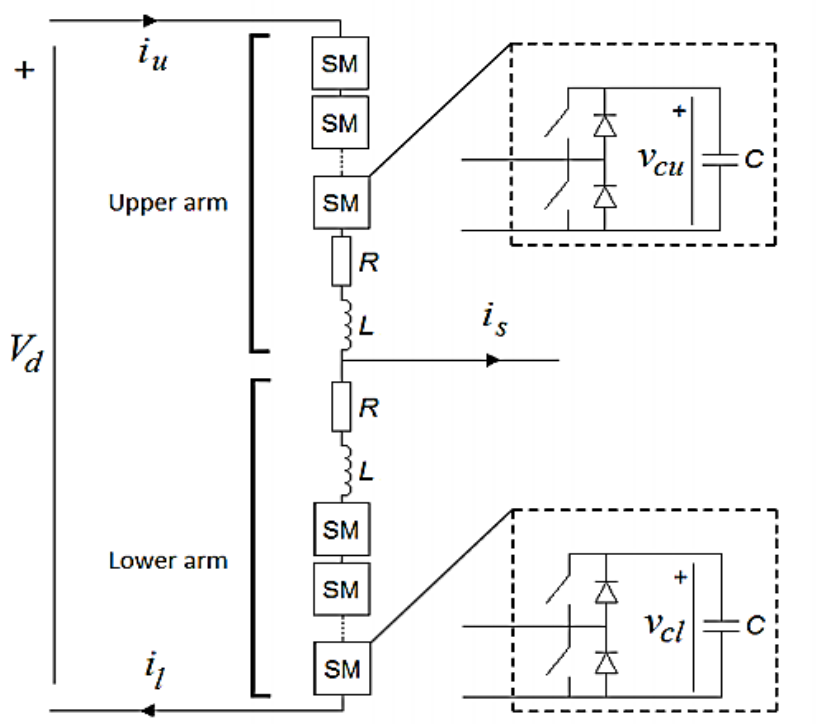

FIGURE 3.8: Basic Configuration of Modular multilevel converter

MMC uses an arm reactor (L) in its each arm to suppress the circulating currents which arise due to the difference between the phase leg and DC voltages [33]. Arm inductance is also used to minimize the fault currents during dc short circuits [33].

Every SM in MMC commonly uses half bridge converter topology which is shown in Figure 3.8 and 3.9 [10]. It mainly comprises a cell capacitor (C) and two integrated gate bipolar transistors (IGBTs) each with an anti parallel diode [15].

3.4.2 Operational Principles

The half bridge submodule is shown in Figure 3.9, since the IGBTs are controllable devices, the gating signals G_1 and G_2 are used to control the switches S_1 and S_2. Both switches perform in complementary fashion i.e. $S_1 = 0 \Rightarrow S_2 = 1$ and vice versa. The half bridge SM can have three possible states during MMC operation which are given below [10, 55, 56];

1. On State: when SM is on it is said to be in inserted or on state. The gating pulse G_1 is high and G_2 is low while the output voltage of SM (V_sm) will be equal to the voltage across capacitor (V_C). The charging or discharging of capacitor is depending on current direction for $i > 0$ capacitor charges and for $i < 0$ the capacitor discharges.

2. Off State: when SM is off it is said to be bypassed or in off state. The gating pulse G_1 is low and G_2 is high while $V_sm = 0$ as$V_C = 0$ and it would remain zero i.e. constant, no matter what the current direction is.

3. Blocked State: when both SMs are off it is said to be in blocked state, hence $G_1$and G_2 both are low whereas current will be conducted through the freewheeling diodes. For $i > 0$ the capacitor will charge but ideally it cannot be discharged.

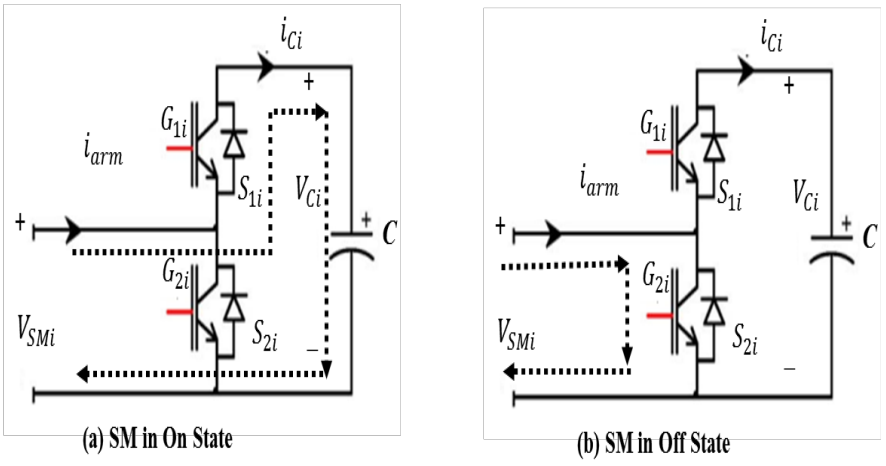

FIGURE 3.9: Half Bridge Circuit for i^{th} submodule(SM) [10]

The capacitor in each submodule is a vital element for making MMC a multilevel converter as it holds the voltage of $V_C = V_{dc}/N$ across it and manages to make $N + 1$ voltage levels at the output voltage waveform [7].

Each arm has the capability to withstand the full DC link voltage by sharing it among each submodule where each submodule withstands voltage equals to V_{dc}/N, thus MMC has the capability to block twice the Dc-link voltage per phase [55].

A single phase 5-level MMC with 4 submodules in each arm are shown in Figure 3.10, it provides the clear view of upper and lower arm voltages where each waveform comprises voltage equals to $+V_{dc}$ whereas the line to neutral voltage waveform comprises the peak voltage of $V_{dc}/2$.

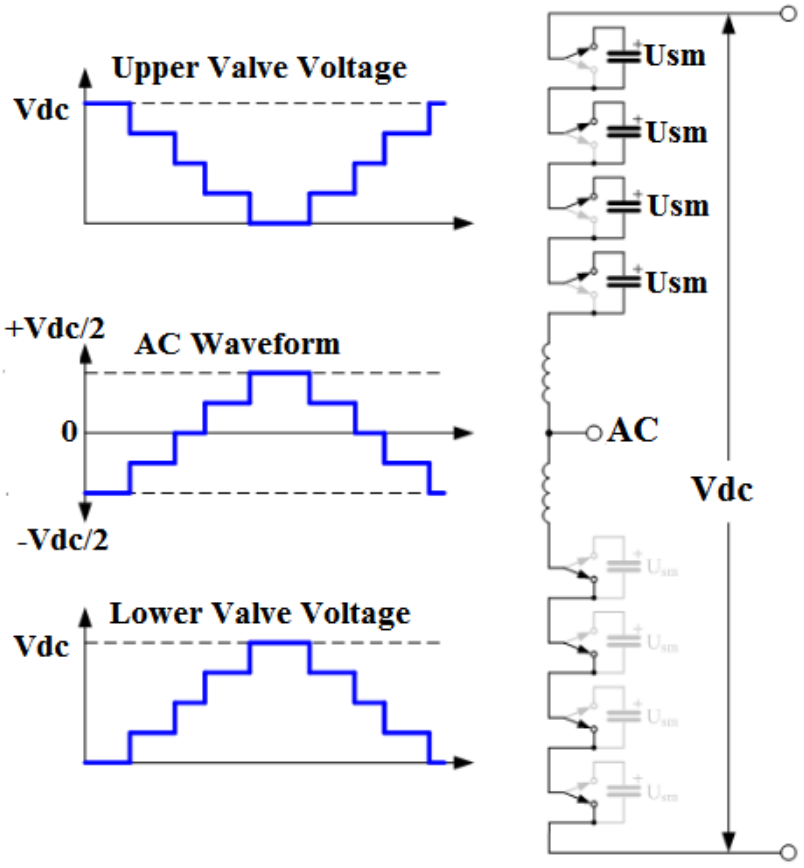

FIGURE 3.10: Operating principle of 5-level modular multilevel converter [57]

3.4.3 Mathematical Modeling of Modular Multilevel Converter

The basic single phase grid tied MMC configuration is shown in Figure 3.11 and it is used for the mathematical modeling under this section. In Figure 3.11 the sum of voltages across each capacitor in upper and lower series connected submodules are replaced by equivalent variable DC voltage sources separately in both arms whose voltages [55].

Arm inductance is represented by $L_{arm}$and the equivalent resistance offered by the arm reactor is represented by R_{arm}. The DC link voltage V_{dc} is split in to two equal halves $V_{dc}/2$ with a separating 0 voltage point. The upper and lower arm currents are represented by $i_U$and i_L respectively.

The phase reactor is represented by R_g+jL_g to mitigate the AC side high frequency harmonics and improve the quality of output current waveforms. The grid side voltage is represented byV_s, V_t and i_t are converter output terminal voltage and current respectively.

The circuit modeling is done on the basis of the assumption that the number of series connected submodules and the switching frequency used for the switching of the semiconductor devices is considered infinitive. These assumptions help to develop a continuous model of MMC [55]. Applying Kirchoff's current law (KCL) in Figure 3.11.

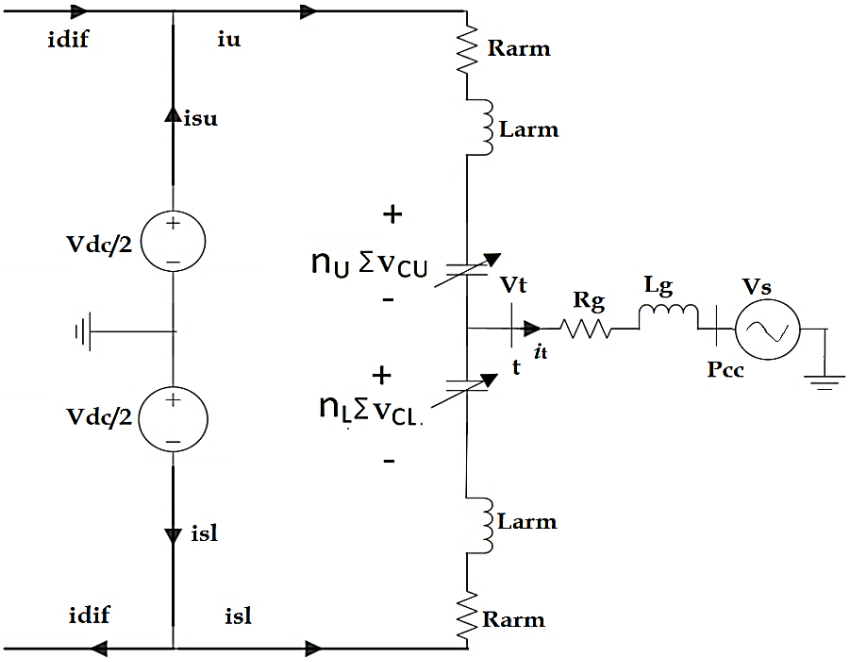

FIGURE 3.11: Equivalent continuous model of single phase MMC [55]

$$i_U + i_L = i_t \tag{3.18}$$

$$i_U = i_{su} + i_{dif} \tag{3.19}$$

$$i_L = i_{sl} - i_{dif} \tag{3.20}$$

Substituting 3.20 and 3.19 in 3.18 we get,

$$i_t = i_{su} + i_{sl} \tag{3.21}$$

The difference between the upper and lower arm currents is,

$$i_U - i_L = i_{su} - i_{sl} + 2i_{dif} \tag{3.22}$$

Let N is the total number of series connected submodules per arm of MMC and n_k is the insertion index for the submodules inserted in the arm where $k = U$ and L. Then the capacitor voltage across each submodule v_{ck} and the total voltage per arm V_{ck} which is the sum of the individual capacitors per submodules is represented as [10, 55]

$$V_{ck} = n_k \sum v_{ck} \tag{3.23}$$

If $n_k = 0 \implies$ all the submodules in the converter leg are bypassed and if$n_k = 1 \implies$ all the submodules in the converter leg are inserted. Asn_k ranges from 0 to 1 therefore the number of inserted submodules in the one arm means the bypassing of submodules in the other arm. Hence, it is expressed as

$$n_U + n_L = 1 \tag{3.24}$$

Applying Kirchoff's Voltage Law (KVL) in the upper and lower leg in Figure **??**.

$$\frac{V_{dc}}{2} - n_U \sum v_{sk} - V_s(R_{arm} i_{dif} + L_{arm} \frac{d}{dt} i_{dif}) - (L_g \frac{d}{dt} + R_g i_t) = R_{arm} i_{su} + L_{arm} \frac{d}{dt} i_{su} \tag{3.25}$$

$$\frac{V_{dc}}{2} + n_L \sum v_{sk} + V_s(R_{arm} i_{dif} + L_{arm} \frac{d}{dt} i_{dif}) - (L_g \frac{d}{dt} + R_g i_t) = R_{arm} i_{sl} + L_{arm} \frac{d}{dt} i_{sl} \tag{3.26}$$

Suppose the source current in upper and lower arm are are equal i.e.

$$i_{su} = i_{sl} \tag{3.27}$$

Therefore combining the fact that$V_s = V_s$ with the assumption made in 3.25 and using in 3.23 and 3.24 which gives,

$$V_s - n_U \sum v_{sk} + n_L \sum v_{sk} = 2(R_{arm} i_{dif} + L_{arm} \frac{d}{dt} i_{dif}) \tag{3.28}$$

From 3.28 $\sum V_{cu} = \sum V_{cl} = V_{dc}$ is a case where the upper and lower arm capacitor voltages are perfectly balanced. This condition implies that the circulating current produces only when there is imbalance between the converter arm voltages. The circulating current becomes zero in steady state if the deviancy of sum of capacitor voltages from the DC link voltage $V_{dc}$is zero [55]. Substituting the supposition made in 3.27 in 3.21 and later in 3.22 then we get,

$$i_{su} = i_{lU} = \frac{i_t}{2} \tag{3.29}$$

and

$$i_{dif} = \frac{i_U - i_L}{2} \tag{3.30}$$

Substituting 3.29 and 3.30 in 3.25 and 3.26 and then adding gives,

$$n_L \sum V_{cu} - n_u \sum V_{cl} = 2V_s + 2R_g i_t + 2L_g \frac{d}{dt} i_t + R_{arm} i_t + L_{arm} \frac{d}{dt} i_t \tag{3.31}$$

The output terminal voltage of the converter V_t, the equivalent resistance R_{eq} and the equivalent inductance L_{eq} is shown in 3.32, 3.33 and 3.34 respectively

$$V_t = \frac{n_L \sum V_{cu} - n_u \sum V_{cl}}{2} \tag{3.32}$$

$$R_{eq} = \frac{R_{arm}}{2} + R_g \tag{3.33}$$

$$L_{eq} = \frac{L_{arm}}{2} + L_g \tag{3.34}$$

Therefore equation 3.31 can be rewritten as

$$V_t = L_{eq} \frac{d}{dt} i_t + R_{eq} i_t + V_s \tag{3.35}$$

Equation 3.35 presents the mathematical model for the AC side dynamics of single phase grid tied MMC. This model is extended to the mathematical model of three phase grid tied MMC in equation 3.36

$$V_{tabc}(t) - V_{sabc}(t) = L_{eq}\frac{d}{dt}i_{tabc} + R_{eq}i_{tabc}(t) \tag{3.36}$$

$$V_{tabc}(t) = \frac{V_{dc}}{2}m_{abc}(t) \tag{3.37}$$

Equation 3.37 represents the three phase output terminal voltages V_{tabc} in terms of three phase reference modulating signals m_{abc} for three phase inverter modular multilevel converter [10, 55, 56, 58]. The modulating signals are the control signals that are responsible for synthesizing a controlled $N+1$ level output voltage waveform [40]. As the modulating signal $m(t)$ changes from -1 to 1, in response, the output terminal voltage changes from -V_{dc}/2 to V_{dc}/2. Equation 3.38 represents the relation for three phase modulating signals [40] as

$$m_{abc}(t) = \hat{m}\cos((\omega t + \theta) + \phi) \tag{3.38}$$

$\hat{m}$ is the modulation index and it ranges from 0 to 1, θ is the initial phase angle, ω is the fundamental frequency in radians and ϕ is the angle for three phase AC signals and can take values $\{0, \frac{2\pi}{3}, \frac{-2\pi}{3}\}$ for the respective phases [40].

3.5 Matlab/Simulink Model of Three Phase Grid Tied MMC

Under this section, the simulation model for 21-level grid tied MMC is presented on the basis of mathematical model developed in the foregoing section. This model is developed in Matlab/Simulink 2016b environment and shown in 3.12. The number of series connected submodules (N) is chosen twenty to build MMC converter simulation model, as a result the output voltage waveform of the MMC comprises $(N+1)$ levels i.e. twenty one.

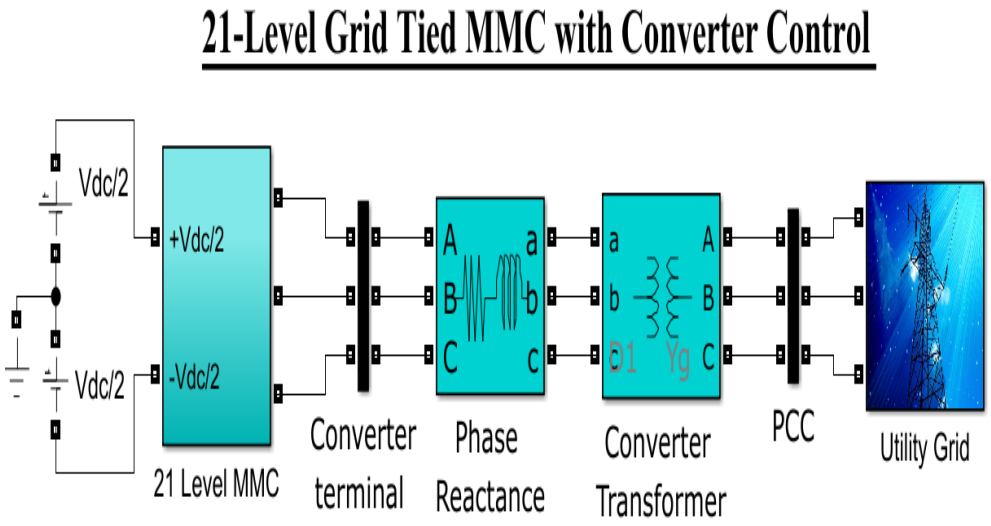

FIGURE 3.12: Simulation Model for 21-level Grid tied MMC in Matlab Simulink 2016b Environment

The different blocks of the simulation model are discussed in this section. The input Dc voltage source V_{dc}=100kV is divided into two equal halves of the DC voltage $V_{dc}/2$ =50kV, split by a supply mid-point having 0V voltage as reference for the entire simulation model.

The three phase 21-level MMC Simulink model is shown in Figure 3.13. It comprises three phase legs each comprising two arms, an upper one and a lower one.

The arm inductance L_{kU} for upper arm is equal to the arm inductance L_{kL} has the value of 3mH. Therefore the equivalent resistance offered by the arm reactor is also same in upper and lower arm i.e. R_{kU}=R_{kl} and it is chosen 1Ω.

The voltage across each capacitor V_C in a submodule is 2mF. The upper and lower arm in each phase leg comprises twenty series connected half bridge submodules.

These series connected submodules are collectively represented by a block named as U_k for upper arm and L_k for lower arm where k represent the three phases $\{a, b, c\}$ respectively.

The parameters used for the design of Simulation model of 21-level MMC in Simulink are provided in Table 3.3.

TABLE 3.3: Design Parameters for 21-Level MMC Simulation Model [15]

Description	Symbol	Values
Sub Module Capacitor	C	0.002F
Arm Inductance	L_{arm}	0.003H
Arm Resistance	R_{arm}	1 Ω
Number of submodules per arm	N	20
Number of levels in output voltage	$N+1$	21
Output peak voltage	V_p	50kV
Voltage across each capacitor	V_c	5kV

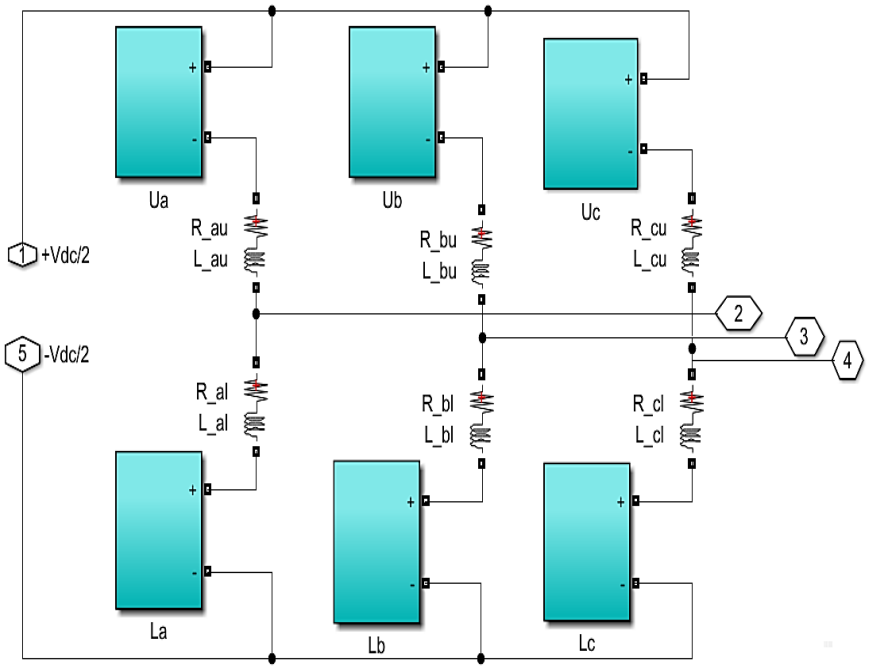

FIGURE 3.13: Simulation model of three phase 21-level MMC

The simulation model for half bridge submodule is shown in Figure 3.14. The gating pulses are provided in a complementary fashion to both of the IGBTs in the half bridge Submodule. Not gate logical operator is used to complement the gating pulses for the IGBT named SMbar to that of the IGBT titled SM, thus ensuring that both switches are not turned on at the same time.

SM in on state implies SMbar in off state and vice versa. These half bridge sub modules are connected in series in the each arm of the converter where each submodule corresponds to a discrete voltage step in the converter output voltage. The 21-level MMC uses twenty submodules per arm to output twenty one level voltage waveform.

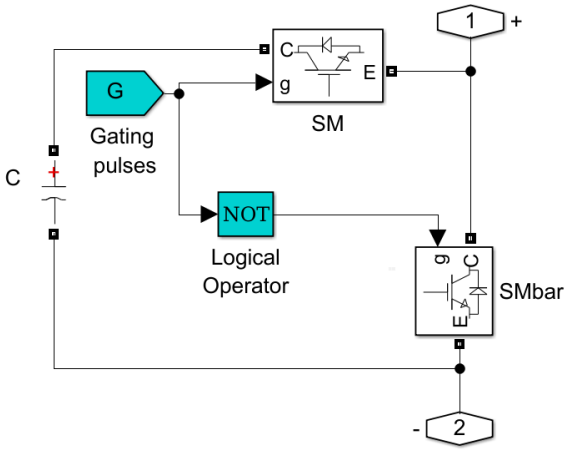

FIGURE 3.14: Simulation model of three phase 21-level MMC

The upper arm of 21-level MMC for phase A, uses twenty series connected half bridge submodules is shown in Figure 3.15

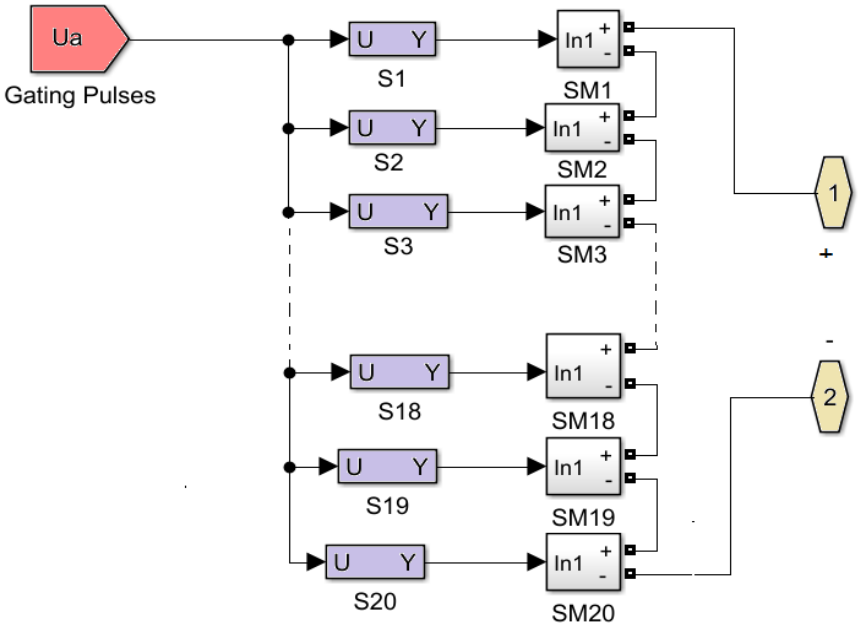

FIGURE 3.15: Three phase 21-level MMC single phase arm Model in Simulink.

3.6 AC Grid Modeling

This section involves the modeling of three phase AC grid, by simply using a three phase symmetrical balanced voltage source. In order to realize a practical grid, a three phase transmission line joins the AC grid through the grid side bus and connects three phase load.

This load is connected to another three phase load through another three phase transmission line which in turn joins with point of common coupling PCC. The single line diagram of the Grid is shown in Figure.3.16.

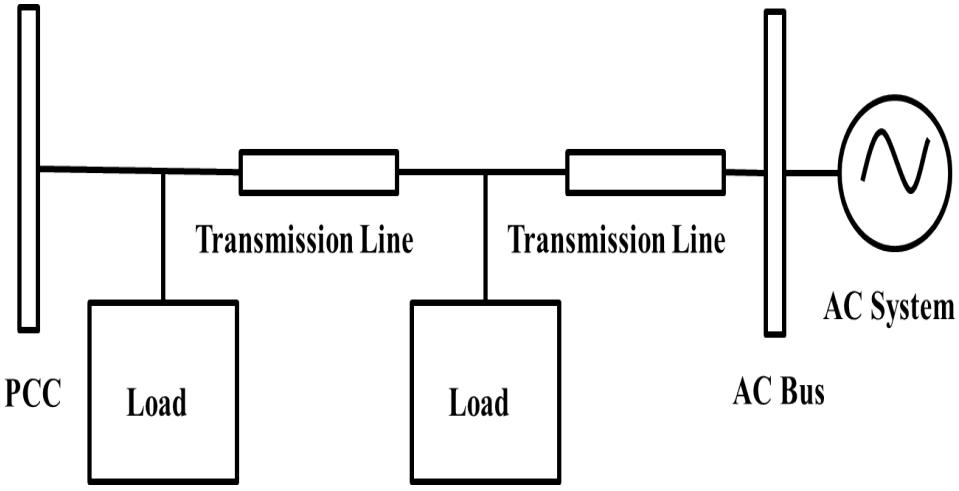

FIGURE 3.16: The single Line Diagram of Designed Grid

3.6.1 Simulink Based Model of Grid

The simulation model of grid is designed on the basis of single line diagram presented in Figure 3.17. The model uses three phase balanced AC source at $220kV$ nominal voltage and 50Hz nominal frequency.

The grid side bus is used to provide connection between the three-phase transmission lines and the grid whereas it also provides the measurement ports for measuring the three phase grid voltages and currents.

An active three-phase 50MW load with wye-grounded configuration is connected to the grid through a transmission line of 10km. This load is connected to another

load with similar specifications by means of a another 10km transmission line, which in turn connects the load with the point of common coupling PCC.

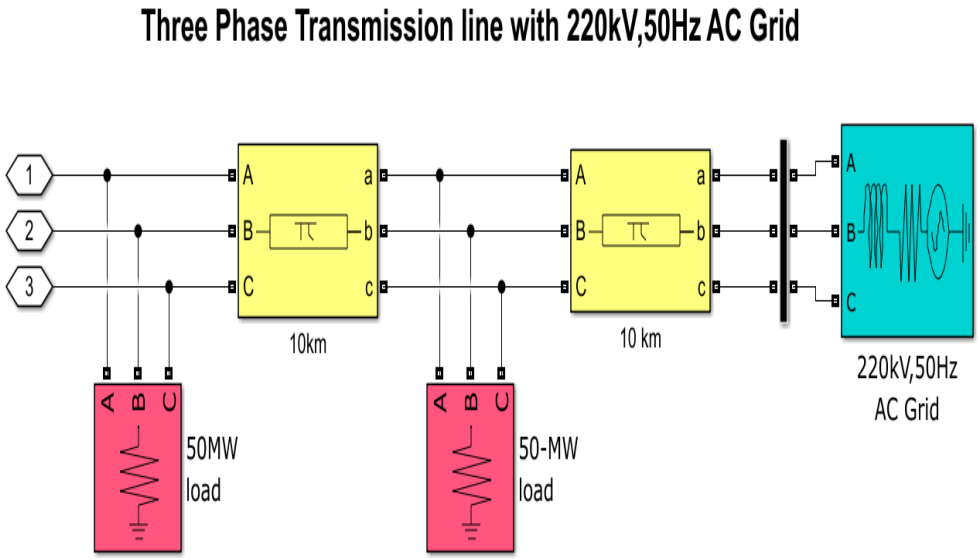

FIGURE 3.17: The simulation model of three-phase AC Grid in Simulink

The parameters used for the design of grid model are represented by table 3.4

TABLE 3.4: text

Description	Symbol	Values
AC Grid Voltage	V_s	220kV(r.m.s)
Ac Grid Current	I_s	347A (r.m.s)
Nominal Grid Frequency	f	50Hz
Transmission Line	$2\times\pi$	2×10km
Load	$2 \times L$	2×50MW

The instantaneous active power P_g of 150 MW is flowing through the circuit when the converter is in stand-alone mode of operation and it can be is shown in Figure 3.18.

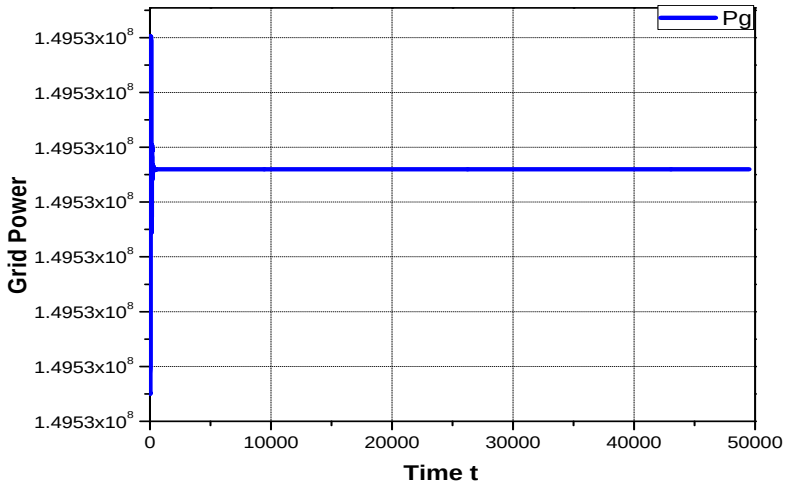

FIGURE 3.18: Grid Power in standalone mode of operation

The three phase grid voltages and current waveforms obtained from the grid side bus and the simulation results are presented in Figure 3.19

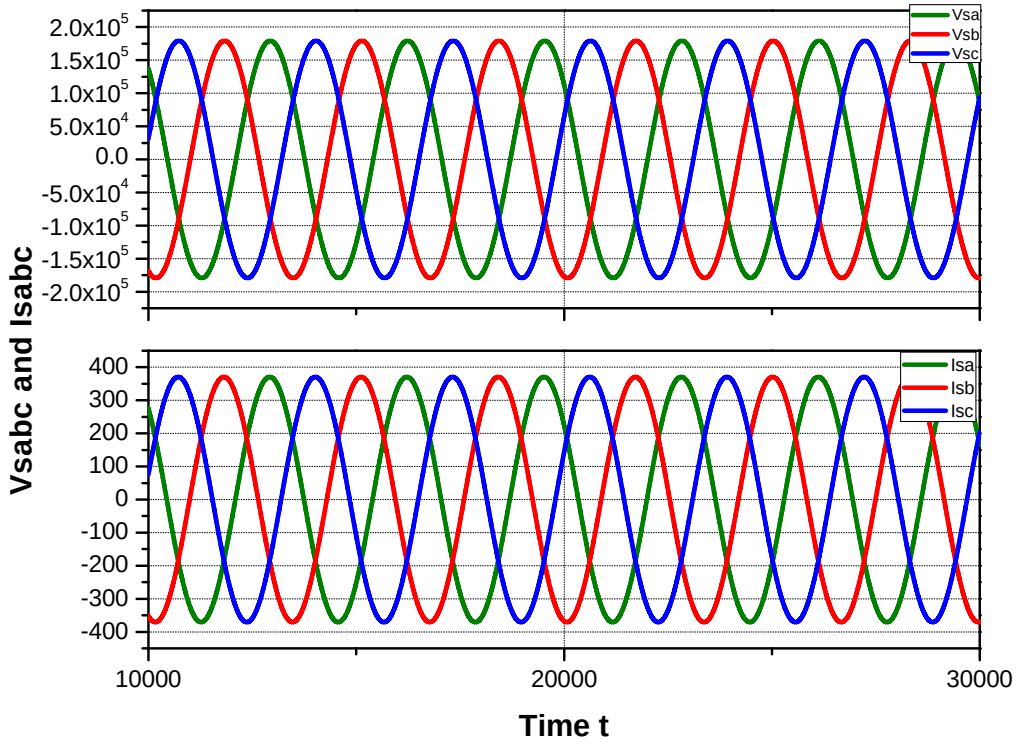

FIGURE 3.19: Three phase Grid voltages and currents measured at Grid side Bus.

3.7 Chapter Summary

This chapter presented the detailed discussion about the structure, working principle, mathematical modeling and development of simulation model on the basis of mathematical modeling developed previously for both 2-level grid tied VSC and 21-level grid tied MMC. In the end the modeling of AC grid was also presented.

Chapter 4

Control of Voltage Source Converters

4.1 Introduction

In this chapter the strategy developed for the design of control structure is discussed for VSC based HVDC systems. As this work is focused on the inverter side dynamics of the VSC which are same for both of the converter topologies i.e. conventional two-level VSC and modular multilevel converter MMC. Therefore the same control strategy is developed for both grid tied converter topologies. This control strategy involves the DQ0 transformations, Modeling of three grid connected converters in DQ0 reference frame, Design of PLL, PI compensator design by using Modulus optimum tuning criteria, Transfer function extraction and control of switching devices. The simulation models of whole control system is also presented by the end of this chapter.

4.2 Grid Tied VSC System

The ABC reference frame model for a grid tied VSC system is shown in Figure 4.1.

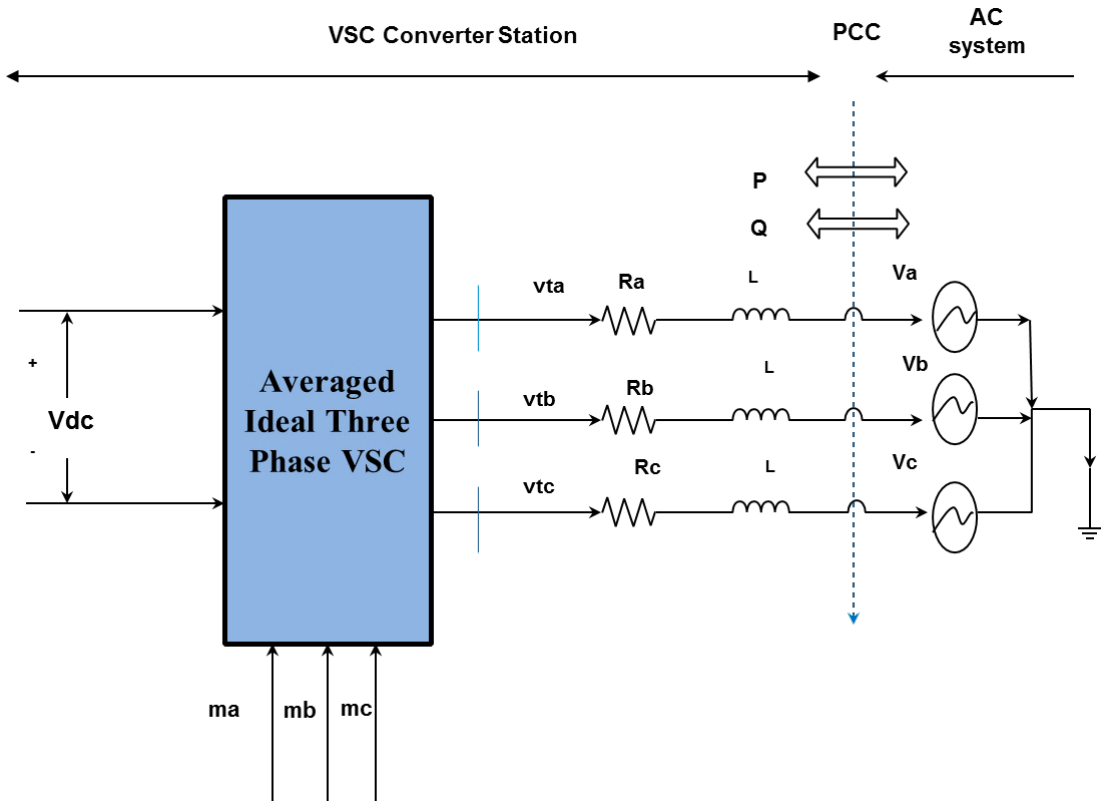

FIGURE 4.1: Reference model for the grid tied VSC System [26]

The reference model for a grid tied voltage source converter presented in Figure 4.1 can be mathematically expressed by the following expression,

$$L_d \frac{\vec{i}_{abc}}{dt} = -R\vec{i}_{abc} + \vec{V}_{abc} - \vec{V}_{sabc} \tag{4.1}$$

Where $\vec{i}_{abc}$ represents three phase output current signals of VSC system,$\vec{V}_{tabc}$ is converter three phase output terminal voltage and $\vec{V}_{sabc}$ represents the three-phase AC grid voltages in ABC reference frame.

L represents the line reactor and R represents the equivalent resistance offered by the line reactor [26]. As the three phase system models are very complex for the analysis therefore their control structures are not easy to develop [59].

This thesis transforms the three phase alternating (AC) signals from stationary frame of reference to a rotating reference frame where the vector quantities (signals) are reduced to two constant (DC) vectors [60]. Such a transformation is

known as dq0 or simply dq transformation and it is explained in the section below.

4.3 Dq0 Transformations

The direct quadrature or commonly known dq0 transformation is a mathematical transformation which is used for the dynamic analysis of three-phase electrical systems because it reduces the complexity and simplifies the system parameters by making them purely dc values.

The dq0 transformation also known as Park Transformation was first proposed by Robert H. Park in 1929 for the simplified study of electrical machines [61]. The idea of using this transformation was adopted in order to simplify the analysis of electrical machines and nowadays it is most commonly used technique for the development of simplified control techniques with zero steady state error because of the fact that it transforms the three AC signals from stationary reference frame to two phase DC signals in rotating reference frame.

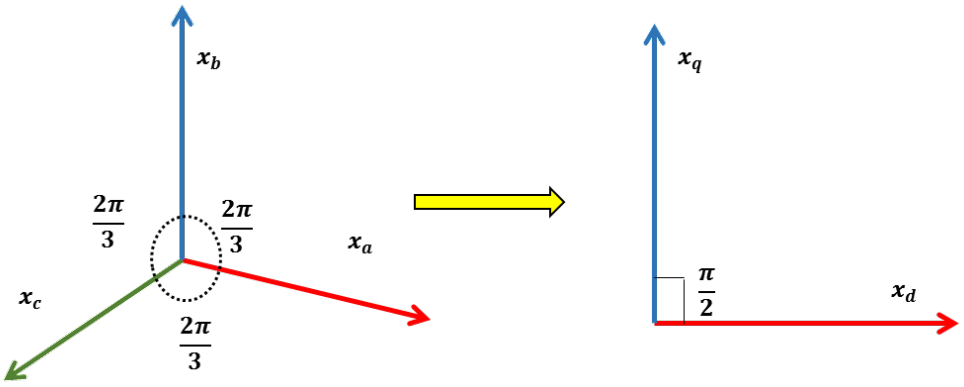

FIGURE 4.2: Axis transformation from abc to dqo reference frame [60]

Figure 4.2 represents the transformation of abc-stationary frame to dq0-rotating frame. The stationary frame, comprising three phase rotating signals where each signal is apart from the other by an angle of 120 deg, is transformed to a rotating frame having non varying dc vectors which are orthogonal to each other [61, 62].

4.4 Mathematical Expression for Park's Transformation

The mathematical relation expressing Park's Transformation is given by equation 4.4.

$$x_{dq0} = \mathbf{T} x_{abc} \tag{4.2}$$

The transformation matrix **T** used to perform Parks Transformation is related in 4.3 [62].

$$\begin{bmatrix} x_d \\ x_q \\ x_o \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \sin(\theta) & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3} \\ \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{4.3}$$

Equation 4.3 shows the transformation of three phase sinusoidal electrical signals $\begin{bmatrix} x_a & x_b & x_c \end{bmatrix}^T$ to two dimensional dq-vectors $\begin{bmatrix} x_d & x_q & x_0 \end{bmatrix}^T$ by using transformation defined by **T**. This feature of dq0 transformation makes it really attractive to be used in the control applications of complex three-phase AC systems.

As it simplifies the analysis and allows the use of simple PI controllers to get zero steady state errors with the simple DC quantities in order to achieve fast and stable output dynamic and steady state response [26, 59, 60].

Therefore to further proceed with control of three phase grid tied inverters there is a need to develop the three phase equivalent mathematical model in dq reference frame. This job is done and details are provided below.

4.5 DQ0 Modeling of Three-Phase VSC System

The dq0 modeling of three-phase VSC system based on the model presented in Figure 4.1 is shown in Figure 4.3 [26]. In order to simplify the control structure design, the three phase mathematical models are transformed to dq0 mathematical

model and can be expressed by the set of subsequently provided equations

$$L\frac{d}{dt}i_d = L\omega(t)i_q - Ri_d + V_{td} - V_{sd} \tag{4.4}$$

$$L\frac{d}{dt}i_q = -L\omega(t)i_d - Ri_q + V_{tq} - V_{sq} \tag{4.5}$$

$$\frac{d\rho}{dt} = \omega(t) \tag{4.6}$$

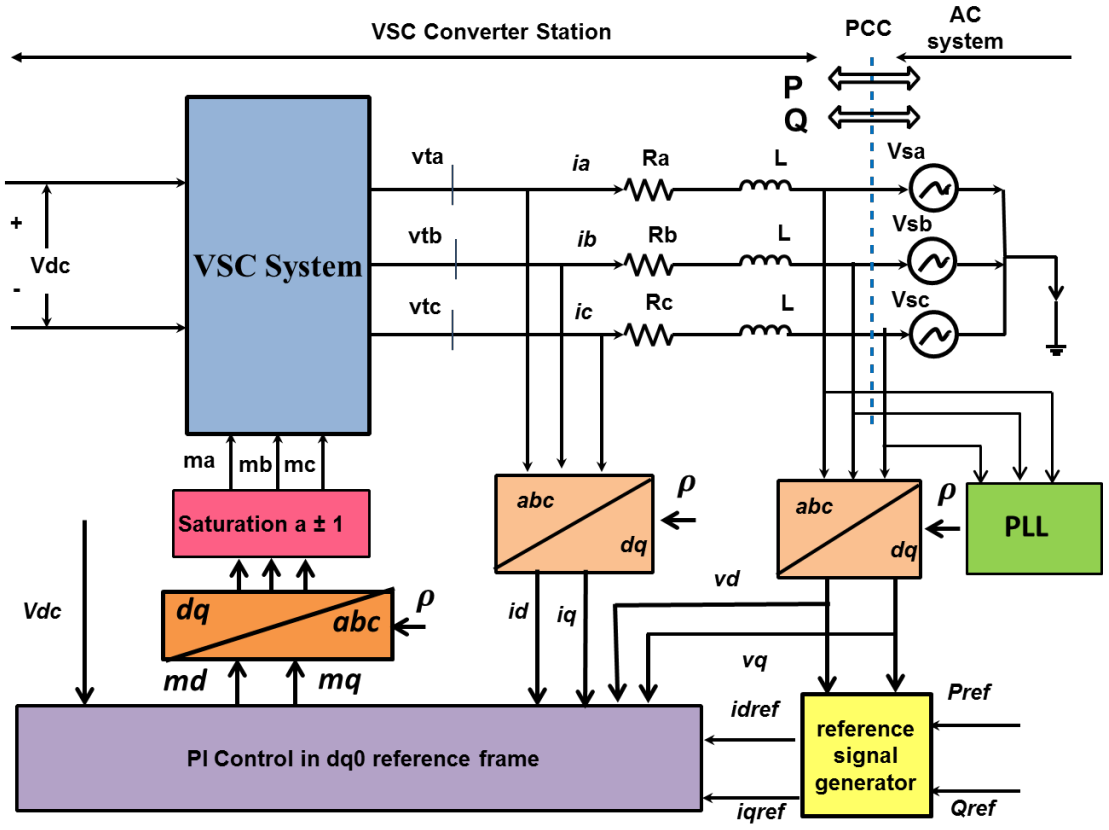

FIGURE 4.3: Schematic for the active/reactive control of VSC in dqo frame [26, 40]

The set of equations 4.4 to 4.6 present the dq model of three phase AC system which is mathematical equivalent for models expressed in 3.15 to 3.17 and 3.36 3.38 respectively [26]. In dq0 model i_d and i_q represent the d and q components of converter output current , V_{td} and V_{tq} represent the d and q components of converter output terminal voltage and V_{sd} and V_{sq} are d and q components of AC grid side voltages respectively.

Here ρ is the angle between the ABC stationary frame and dq0 rotating frame of reference and ω is the angular speed with which the dq0 frame is rotating [40]. The expressions for active power $P_s(t)$ and reactive power $Q_s(t)$ at point of common coupling are found in equation 4.7 and 4.8 respectively.

$$P_s(t) = \frac{3}{2}(V_{sd}(t)i_d(t) + V_{sq}(t)i_q(t)) \tag{4.7}$$

$$Q_s(t) = \frac{3}{2}(-V_{sd}(t)i_q(t) + V_{sq}(t)i_d(t)) \tag{4.8}$$

From 4.4 to 4.8 it can be clearly observed that the grid tied VSC system is strongly coupled system due to the coupling states i_d and i_q therefore the independent control of active and reactive current or the independent control of active and reactive power is not possible until or unless the term V_{sq} does not become equal to zero [40]. When V_{sq}=0 than 4.7 and 4.8 can be rewritten as follows

$$P_s(t) = \frac{3}{2}(V_{sd}(t)i_d(t) \tag{4.9}$$

$$Q_s(t) = \frac{3}{2}(-V_{sd}(t)i_q(t) \tag{4.10}$$

Hence it is evident from 4.10 and 4.11 that the active power $P_s(t)$ and reactive power $Q_s(t)$ can be independently controlled by the respective active current i_d and reactive current i_q, when the q-component of grid voltage V_{sq} is forced to make equal to zero [26, 40]. The references for the active and reactive power can be acquired by using equation 4.12 and 4.13.

$$P_{sref} = \frac{3}{2}[v_{sd}i_{dref}] \tag{4.11}$$

$$Q_{sref} = \frac{3}{2}[-v_{sd}i_{qref}] \tag{4.12}$$

The foregoing discussion concludes that $V_{sq} = 0$ is the only and necessary condition, which allows synchronization of grid with the converter which enables to make the grid voltages in phase with the converter current and power flow become realizable either from grid to converter ar from converter to grid [40].

Once the grid is synchronized, the active/reactive currents or active/reactive power can be independently controlled at point of common coupling (PCC) as long as the above mentioned condition is held true.

For this purpose the services of phase locked loop are brought under practice due to its ability to lock the grid phase angle to regulate the system on the grid frequency [60]. This thesis performs grid synchronization in dq frame with the help of phase locked loop (PLL).

4.6 Phase Locked Loop (PLL)

The space phaser $\vec{V_s}(t)$ equivalent of three phase AC grid voltage can be represented in dq0 reference frame as follows [26]

$$V_{sd}(t) = \hat{V}_s \cos(\omega_0 t + \theta_0 - \rho) \tag{4.13}$$

$$V_{sq}(t) = \hat{V}_s \sin(\omega_0 t + \theta_0 - \rho) \tag{4.14}$$

Where ω_0 is the grid initial frequency, θ_0 is the grid initial phase angle and ρ is the angle between the three phase reference frame and dq reference frame and $\hat{V}_s$ is some constant. From 4.14 it is evident that if the phase angle of grid voltage ω_0 t+ θ_0= ρ than V_{sq} becomes equal to zero therefore a mechanism devised in [26] is used to regulate V_{sq} at zero and can be expressed by the following feedback law

$$\omega(t) = H(s)V_{sq}(t) \tag{4.15}$$

Where ω(t) is the grid frequency and $H(s)$ is the transfer function of the compensator substituting 4.7 and 4.14 in 4.15 we get 4.16 represents the nonlinear dynamic behavior of the system and it is well-defined as Phase locked loop PLL [26].

$$\frac{d}{dt}\rho = V_s H(s)(\omega_0 t + \theta_0 + \rho) \tag{4.16}$$

If PLL tracks $\omega_0 t + \theta_0$ than the term $\omega_0 t + \theta_0$-$\rho \approx 0 \implies \sin(\omega_0 t + \theta_0 - \rho) \approx \omega_0 t + \theta_0$- ρ.

These all assumptions are used in 4.16 and rewritten as follows in 4.17 and the operation of 4.17 is represented in the form of a control block in Figure 4.4.

$$\frac{d}{dt}\rho = \hat{V}_s H(s)(\omega_0 t + \theta_0 - \rho) \tag{4.17}$$

Figure 4.4 shows that PLL takes the initial angle of grid ω_0 t+θ_0 as the reference signal, ρ is the output of PLL and $\hat{V}_s H(s)$ is the transfer function of the compensator. PLL regulates V_{sq} at zero by adjusting the rotational speed of dqo reference frame.

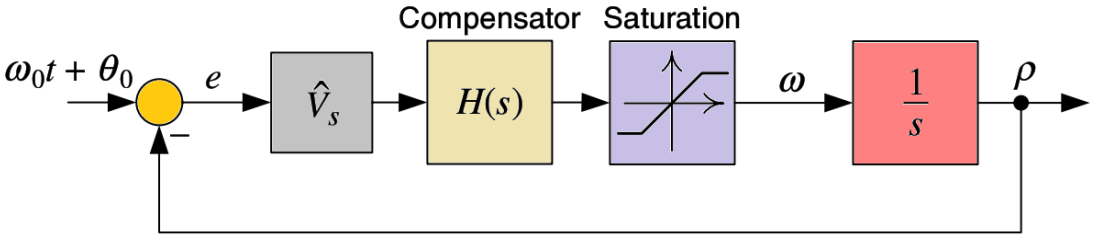

FIGURE 4.4: control block diagram of phase locked loop [26]

The integrator in Figure 4.4 is realized by resettable voltage controlled oscillator (VCO) which is shown in Figure 4.5 whose output ρ is reset to zero once it reaches 2π. The saturater or limiter is used to limit the frequency of grid between maximum and minimum point to avoid unwanted nonlinear dynamics of the PLL in worst case scenario [26].

The schematic diagram of PLL is shown in Figure 4.5 and explains its role in the transformation of three phase grid voltages to two dimensional dq frame vectors. It provides the angle to the dq transformations which aligns both of the frames by making difference of angles equal to zero. When both of the frames get aligned with each other, the reactive component of grid voltage is forced to become equal to zero. The physical implementation of this phenomenon is realized by grid synchronization i.e. the converter is synchronized with the grid.

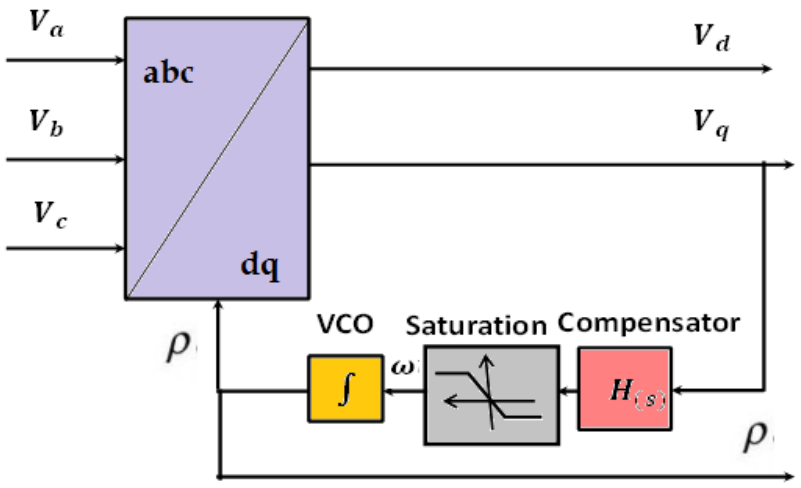

FIGURE 4.5: The schematic Diagram of Phase Locked Loop [26]

The vectorial picture of the operation of PLL for grid synchronization is shown in Figure 4.6. It shows that when the dq reference frame moves ahead of the ABC frame space phasor than $V_{sq} < 0$ therefore PLL slows down the speed of rotation of the dq frame as shown in Figure 4.6 (a) [40].

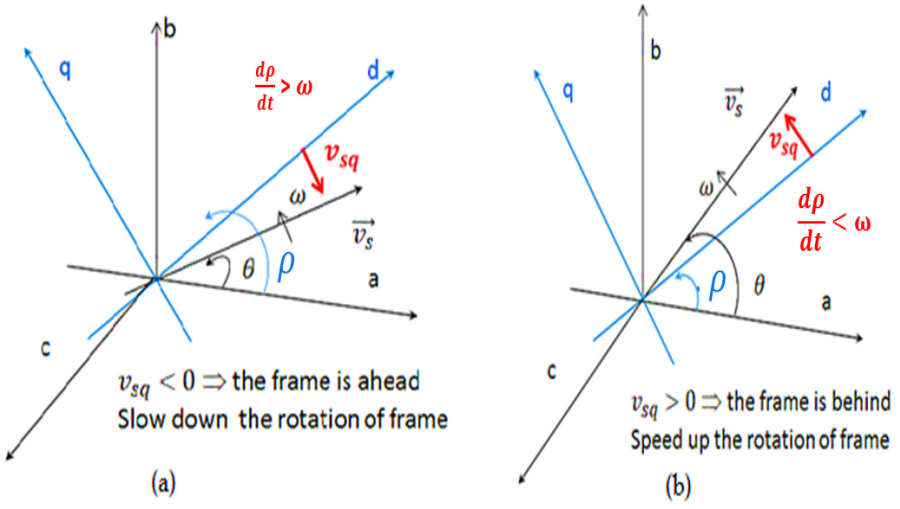

FIGURE 4.6: Operation of phase locked loop [40]

But if the dq frame moves behind the ABC frame space phasor than $V_{sq} > 0$ therefore PLL speeds up the rotation of the dq frame to ensure the alignment of

both frames [40].

Hence the frequency of dq frame follows the frequency of grid. Whereas ρ represents the angle with which the PLL controls the speed of rotation of dq frame.

The alignment of ABC reference space phasor and dq reference frame ensures the grid synchronization, proper transformation of ABC frame signals to dq frame signals (dc quantities) thus enabling the independent control of active and reactive power by regulating the q component of grid voltage i.e. V_{sq} at zer0.

This foregoing discussion is all about the dq transformations and phase locked loop, the next section discusses the development of control structure in dq reference frame.

4.7 Inner Current Control of VSC System

In order to design a control structure it is mandatory to extract the transfer functions of that system which could explain characteristic behavior of the system. Therefore the subsequent section deals with the extraction of transfer functions in dq frame for a grid tied VSC system which uses pulse width modulation (PWM) for the switching of devices.

4.7.1 System Transfer Functions

Figure 4.7 shows the most general form of the inner current control loop of a VSC system which uses PWM for the control of switching devices. It mainly comprises two proportional Integrator (PI) regulator blocks for the control of d and q components of current respectively.

The PI regulators process the error between the reference and measured value of dq currents and transform the error into the voltages. The detailed overview of the control block diagram with their transfer functions is presented in the subsequent

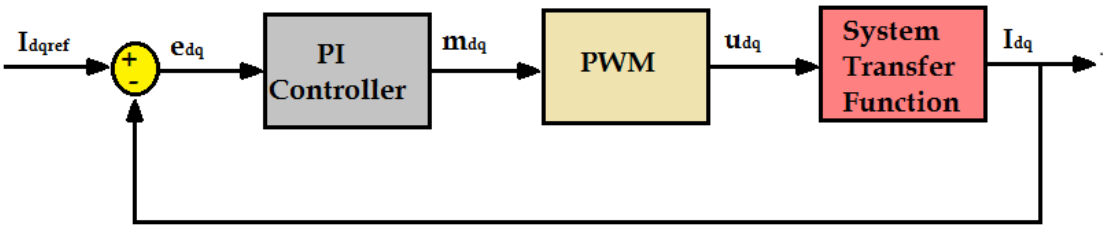

FIGURE 4.7: General Illustration of Inner current Controller in dq frame [63, 64]

4.7.2 PI Controller

The PI control is represented by the equation below [65]

$$K(s) = K_p + \frac{K_i}{s} = K_p \left(\frac{1 + T_i s}{T_i s} \right) \tag{4.18}$$

Where K_p is the proportional gain and T_i is the integral time constant and its value is $\frac{K_p}{K_i}$.

4.7.3 Pulse Width Modulation Converter

It is assumed that the converter output voltage follows the reference voltage signal by an average delay of half of the switching period due to the switching of VSC. Therefore general expression for the PWM is given below [63]

$$R(s) = \left(\frac{1}{1 + T_a s} \right) \tag{4.19}$$

Where $T_a = \frac{T_{switch}}{2}$

4.7.4 Decoupled Control

In order to ensure the decoupled control of the system, dq model is expressed in 4.4 and 4.5 where a new control input u_d and u_q is defined which cancels out the cross coupled terms. Therefore defining 4.4and 4.5 in steady state follows ω(t)=ω_0

and expressed as [26].

$$\frac{di_d}{dt} = L\omega_0 i_q - Ri_d + V_{td} - Vsd \tag{4.20}$$

$$\frac{di_q}{dt} = L\omega_0 i_q - Ri_d + V_{tq} - Vsq \tag{4.21}$$

$$V_{td}(t) = \frac{V_{dc}}{2} m_d(t) \tag{4.22}$$

$$V_{tq}(t) = \frac{V_{dc}}{2} m_q(t) \tag{4.23}$$

$$m_d = \frac{2}{V_{dc}}(u_d - L\omega_0 i_q + V_{sd}) \tag{4.24}$$

$$m_q = \frac{2}{V_{dc}}(u_q + L\omega_0 i_d + V_{sq}) \tag{4.25}$$

By equating 4.24 and 4.25 in 4.22 and 4.23 respectively and substituting the corresponding outcomes in 4.20 and 4.21 accordingly, then the decoupled system model is expressed in 4.26 and and 4.27.

The new control input is represented by u_d and u_q whereas -L$\omega_0 i_q + V_{sd}$ and -L$\omega_0 i_d + V_{sq}$ are the feed forward terms which allow the decoupling of both state variables i.e. i_d and i_q respectively. The decoupled VSC system is represented by following equations with new defined control input [26]

$$L\frac{d}{dt} i_d + Ri_d = u_d \tag{4.26}$$

$$L\frac{d}{dt} i_q + Ri_q = u_q \tag{4.27}$$

From 4.26 and 4.27 it can be seen that the new control input successfully decouples the system and makes it first order differential equation which enables the independent control of active and reactive currents in a simplified manner.

4.26 and 4.27 provide the same dynamics for d and q variables therefore for further analysis only d axis variables are used in this thesis which are equally applicable to q-axis dynamics, consequently the q-axis controller will have the same parameters [26]. Taking Laplace transform of 4.26 we get;

$$
\begin{aligned}
Lsi_d(s) + Ri_d(s) &= u_d(s) \\
i_d(s) &= \left(\frac{1}{sL+R}\right) u_d(s) \\
\implies G(s) &= \frac{1}{R}\left(\frac{1}{1+\tau.s}\right)
\end{aligned} \tag{4.28}
$$

4.28 represents the system transfer function of grid tied VSC system where τ is the time constant and it is equal to L/R [26, 63, 64].

4.7.5 Compensator Design

The detailed block diagram of the inner current controller of Figure 4.4 in dq reference frame using PI control is presented in Figure 4.8 [26, 40] .

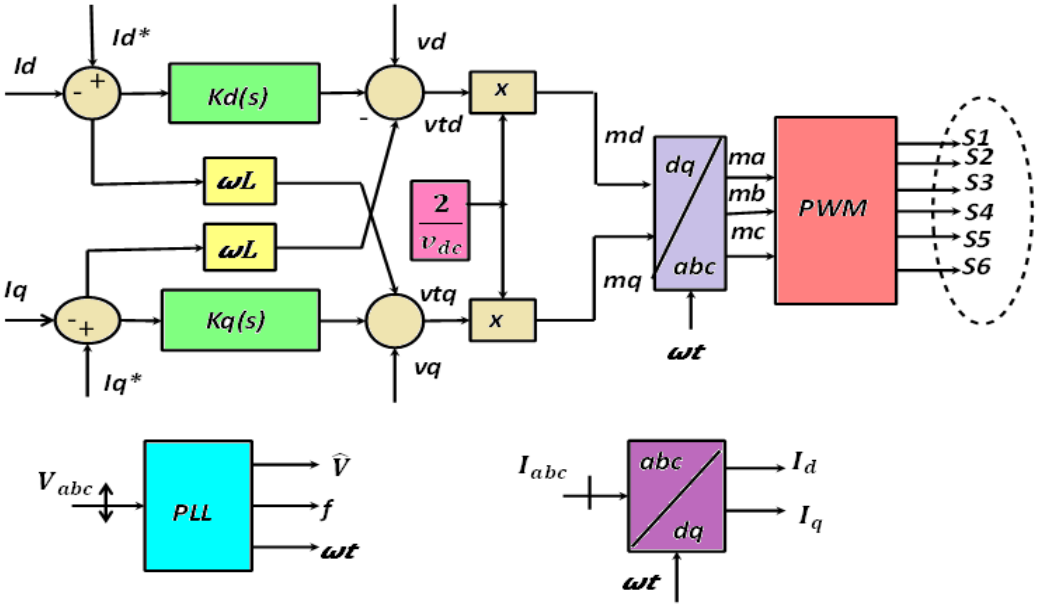

FIGURE 4.8: Block Diagram of Inner current control loop [26, 40, 58]

The references for d-axis i_d and q-axis currents i_q are represented by $i_{dref}(t)$ and $i_{qref}(t)$ respectively and are expressed by 4.29 and 4.30 [26, 66].

$$
i_{dref}(t) = \frac{2}{3V_{sd}} P_{sref}(t) \tag{4.29}
$$

$$i_{qref}(t) = \frac{2}{3V_{sq}} Q_{sref}(t) \tag{4.30}$$

The feed forward terms in the compensator cancel out the cross coupling terms making the decoupled control possible in d and q axis [26, 67]. The converter output voltage in dq reference frame is amplified by the term $2/v_{dc}$ thus producing reference voltages in dq frame [67]. Using inverse dq0 transformation the dq axis vectors are transformed to three phase ABC reference frame.

Later these three reference signals are used as modulating signals to perform pulse width modulation in order to produce the gating signals for the converter switches [40]. The compensator design involves the use of Modulus Optimum tuning criteria [65] to tune the gains of PI controller. It is further discussed with detail in the subsequent section.

4.8 Modulus Optimum Tuning Criteria

When the system transfer function has two poles out of which one pole is dominant or slow so that it mainly affects the system dynamics and the other pole being fast decays quickly than such systems can be controlled by tuning the control loops using a famous technique called as "Modulus Optimum Tuning Criteria "[63, 65, 68, 69]. It cancels the slow pole by the controller zero closed loop gain of the system should be kept higher for large frequencies [70].

4.8.1 Tuning of Current Controller

The simplified block diagram representation of Figure 4.8 is shown below

Figure 4.9 shows that at input the compensator takes error between the desired and measured current values in dq reference frame. The compensator block is presented by the controller transfer function expressed in 4.18. The controller generates the dq-axis modulating signals which are fed to the PWM generator block whose transfer function is expressed in 4.19.

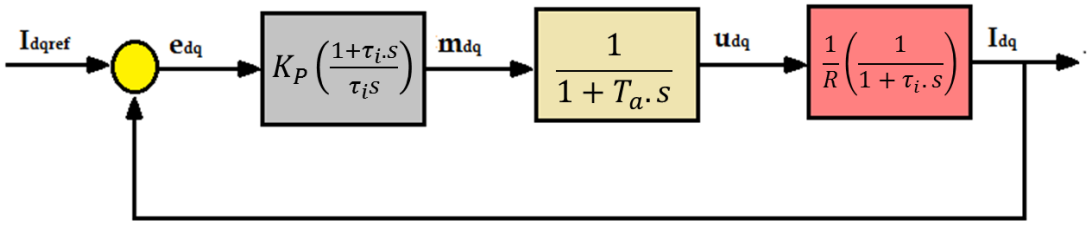

FIGURE 4.9: Simplified block diagram of closed loop control of VSC in dq frame [63]

It eventually generates new control signals which are fed to the converter for the switching of the devices where as the converter transfer function is expressed in 4.28. At the output the measured values of dq current are obtained and again fed to the compensator to regulate the measured values to desired values of current in accordance with the error signals. The open loop transfer function for the entire system can be written as follows

$$G_{OL}(s) = K_p\left(\frac{1+T_i s}{T_i s}\right).\left(\frac{1}{1+T_a s}\right).\frac{1}{R}.\left(\frac{1}{1+\tau s}\right) \tag{4.31}$$

Canceling the slow pole of the plant by the zero of the controller [63, 68]
$\implies T_i = \tau$. The open loop transfer function then becomes

$$G_{OL}(S) = \frac{K_p}{\tau R}.\frac{1}{s(1+T_a s)} \tag{4.32}$$

Based on 4.32 the closed loop transfer function can be found out as

$$\frac{GK}{1+GK} = \frac{\frac{K_p}{\tau.R.T_a}}{s^2 + \frac{1}{T_a}s + \frac{K_p}{\tau.R.T_a}} \tag{4.33}$$

4.8.2 Transfer Function Analysis

Under this section the transfer functions are extracted for both of the converter topologies i.e two-level grid tied VSC (GTVSC) and 21-level grid tied MMC i.e (GTMMC), using Modulus Optimum tuning criteria.

The parameters used for the extraction of transfer function for inner current loop of two-level GTVSC include Line reactance $L + jR$ of 0.04Ω+0.129H, transformer leakage reactance $R_x + jL_x$ of 0.003Ω+0.0048H, the fundamental frequency f of 50Hz and converter switching frequency f_{sw} of 1650Hz [52].

The average converter switching delay which can be represented by $T_a = T_{sw}/2 = 1/2 \times f_{sw}$ and its value is chosen to be 0.0003s. The sampling time for the converter control T_s is equals to $6.06e^{-5}$s. The 21-level grid tied MMC based Simulink model uses same parameters with an additional parameter of MMC Arm reactance $R_{arm}/2 + jL_{arm}/2$ equals to 0.0006Ω+0.0006H which gets added up with the line reactance and gives equivalent series reactance $R_{eq} + jL_{eq}$=0.0406Ω +0.1296H. These parameters are summarized in Table 4.1.

TABLE 4.1: Transfer function Parameters [52]

Description	Symbol	Value
Line Reactance 2-Level	$R + jL$	0.04Ω+0.129H
Line Reactance 21-Level	$R_{eq} + jL_{eq}$	0.0406Ω+0.1296H
Transformer Reactance	$R_x + jL_x$	0.003Ω+0.0048H
Converter Switching Frequency	f_{sw}	1650Hz
Average Converter Switching delay	T_a	0.0003s
Sampling time for converter control	T_s	$6.06e^{-6}$s
angular frequency	ω	314rad
Frequency	f	50Hz

4.8.2.1 Transfer Function for 2-Level Grid Tied VSC Using Modulus Optimum

The transfer function for the inner current control of 2-level GTVSC is evaluated using equation 4.33 and Table 4.1. Before that the optimal gains are calculated at which the current closed loop is tuned. According to Modulus optimum tuning

criteria the optimal gains are calculated as following equations [64]

The proportional gain $K_p = \tau \times R/2T_a = 0.68$,

The integral time constant $T_i = \tau = L/\omega \times R = 0.0102s$,

Integral gain $K_i = K_p/\tau = 66$.

Thus the open loop transfer function based on 4.33 is evaluated to be

$$G(s).K(s) = 1666.67/0.00067s^2 + s$$

And closed loop transfer function is expressed as

$$G(s)K(s)/1 + G(s)K(s) = 1666.67/0.0006s^2 + s + 16666.7$$

The inner current control loop parameters for 2-level GTVSC are summarized in Table 4.2

TABLE 4.2: Current control parameters in 2-level GTVSC

Description	Symbol	Value
Proportional Gain	K_p	0.68
Integral Time constant	T_i	0.0102s
Integral Gain	K_i	66

4.8.2.2 Transfer Function For 21-Level Grid Tied MMC using Modulus Optimum

Similarly, the transfer function of inner current control loop of 21-level GTMMC is also evaluated using parameters described in Table 4.1. The optimal gains are

obtained using Modulus Optimum tuning technique for grid connected modular multilevel inverters [68]. This is similar to the way adopted for the tuning of control loops for conventional VSC as discussed in [63–65].

Therefore the gains for inner current control loop of GTMMC are evaluated as given below and subsequently used to extract the open loop and closed loop transfer functions based on 4.33 and 4.34 respectively

The proportional gain $K_p = \tau \times R/2T_a = 0.683$

The integral time constant $T_i = \tau = L/\omega \times R = 0.0101s$

Integral gain $K_i = K_p/\tau = 67.23$

Thus the open loop transfer function for 21-level MMC inner current control loop based on 4.33 is evaluated to be

$$G(s).K(s) = 1658.29/0.0006s^2 + s$$

And closed loop transfer function is expressed as

$$G(s)K(s)/1 + G(s)K(s) = 1658.29/0.0006s^2 + s + 16658.29$$

The inner current control loop parameters for 21-level GTVSC are summarized in Table 4.3

TABLE 4.3: Current control parameters for 21-level GTMMC

Description	Symbol	Value
Proportional Gain	K_p	0.683
Integral Time constant	T_i	0.0101s
Integral Gain	K_i	67.623

4.9 Control of Switching Devices

After that modulation signals are generated by the current control loop and transformed back to the three phase AC signals from the dq frame, a methodology must be developed to generate the gating pulses which can control the switching devices of converter. As this thesis is dealing with the comparative analysis of 2-level VSC and 21-level MMC therefore a modulation technique which can be equally applicable to both converter topologies is opted for the converter switching purposes.

Therefore a most commonly used approach i.e. Sinusoidal Pulse Width Modulation technique is used to control the converter switching devices. The subsequent section discusses sinusoidal pulse width modulation (SPWM) for conventional VSC and the later section discussed phase shifted carrier pulse width modulation (PSPWM) which is the extension of SPWM for multilevel converter topologies.

4.9.1 Sinusoidal Pulse Width Modulation (SPWM)

Sinusoidal pulse width modulation is used for the switching of semiconductor devices in two-level VSC [15]. A triangular or saw tooth signal V_c with very high frequency f_c is used as a carrier wave [15, 51].

The reference signal m with fundamental frequency f less than carrier frequency f_c is used as a modulation signal [51]. During modulation, the modulation and the carrier signals are compared by a comparator as shown in Figure 4.10.

For a three-phase 2-level VSC, three phase reference signals are compared with the carrier frequency generating the gating signals for the switching devices S_1S_2,S_3S_4,S_5S_6 in each phase [51].

As for each phase only one modulation signal is used therefore bipolar SPWM is utilized which provides simultaneous switching of each pair of switches in opposite phase legs as given shown in Figure 4.1 [51].

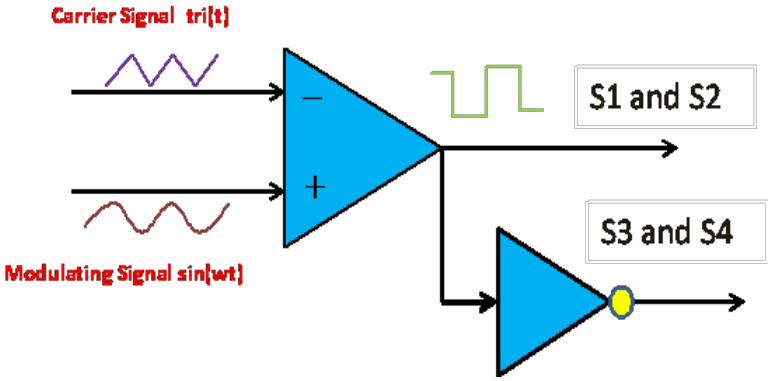

FIGURE 4.10: Operation of Sinusoidal PWM for the generation of Switching Signals [51]

However it is ensured that no two switching devices in the lower and upper arm of the same leg are turned on simultaneously which can short circuit the DC-link capacitors [15]. Equation 3.17 represents the three phase modulation signals where the modulation index $\hat{m}$ is the ratio of amplitudes of modulating and carrier signal [51]. The expression 4.34 represents the relation for modulation index as follows

$$\hat{m} = \frac{A_m}{A_c} \tag{4.34}$$

Where A_m is the amplitude of modulating signal and A_c represents the amplitude of carrier wave which ranges from 1 to -1 . The modulation of switching devices must be performed in the linear region of modulation range i.e. $0 < m < 1$ **??**. The frequency of the switching signals is realized by the frequency of the carrier signal which is integer multiple of the fundamental frequency and it is defined as frequency modulation index m_f , the expression for m_f is given in 4.35 [51].

$$m_f = \frac{f_c}{f} \tag{4.35}$$

Higher m_f implies higher switching frequency which helps to shift the low frequency harmonic content to high frequency harmonics in 2-level VSC thus ensuring less expensive and reduced size AC harmonic filters by smoothing out the output voltage and current waveforms. The next section discusses the control methodology for the switching of semiconductor devices in 21-level MMC.

4.9.2 Phase Shifted Pulse Width Modulation

Phase shifted pulse width modulation (PSPWM) is used for the generation of switching/gating signals in multilevel converter topologies. This modulation scheme uses the comparison of N (where N corresponds to number of submodules per arm and can vary from case to case) carrier waveforms and a reference modulating signal to produce the switching signals for each switching device [7, 71].

PSPWM has certain advantages over other modulation techniques when the switching of multilevel converters is main concern, due to which it is used in the current thesis for the switching of submodules in the upper and lower arms of MMC topology. A few of its advantages are listed below

- It naturally provides the capacitor voltage balancing across in each submodule at higher switching frequencies [7, 71].
- The stress on each switching device and power handling capability is evenly distributed across each submodule [7].

Thus PSPWM is used due to its advantages that it does not require the extra capacitor voltage balancing algorithms hence reducing control complexity [7]. The mechanism involves the generation of N carrier waveforms where each carrier is phase displaced by a phase angle ϕ for half bridge submodule and given in 4.36.

$$\phi = \frac{360^0}{N} \tag{4.36}$$

Each phase displaced carrier is compared with the modulation signal to generate the switching signals for the series connected submodules [7, 36]. As each half bridge submodule contains two IGBTs connected in a leg so both switches are turned on in a complementary operation however the first carrier is zero phase displaced. The theory for generation of modulation signals, amplitude modulation index and frequency modulation index is same as discussed for the case of 2-level VSC.

4.10 Matlab/Simulink Model for VSC Control

This section is dedicated towards discussion of the software based simulation model designed for the control of grid tied VSC system based on the mathematical model developed in the foregoing sections. The converter output voltage is controlled by the converter inner current control loop and the entire methodology used for the development of Simulink based model of converter control is illustrated in the following sections.

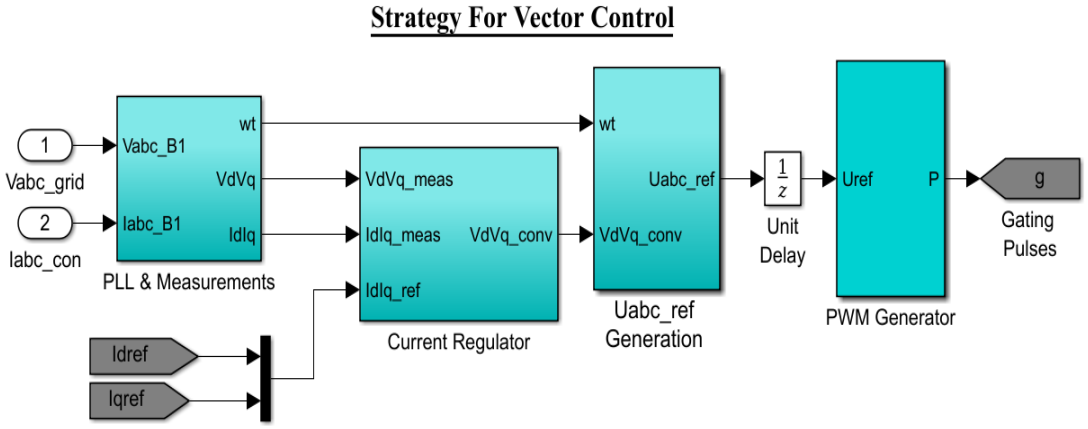

FIGURE 4.11: Strategy developed for the Control of VSC in Matlab/Simulink 2016b

Figure 4.11 shows that the grid voltages and converter currents are given to the PLL and measurements block which provides the synchronizing angle ωt and dq transformed grid voltages and currents. The current regulator block is given the measured dq frame grid voltages and currents as well as their references respectively.

The current regulator block outputs the dq frame converter output terminal voltages in dq frame which are fed along the grid angle ωt, to the $Uabc_{ref}$ generation block. This block generates the reference modulation signals in *abc* frame. The unit delay is used to compensate the delay during the control system sampling and processing.

After that the PWM generator takes the three phase modulating signals as input and produces gating signals for the switching of the semiconductor devices in each arm of the Inverter. Each block in Figure 4.11 is explained with its detailed simulation model and working principles subsequently.

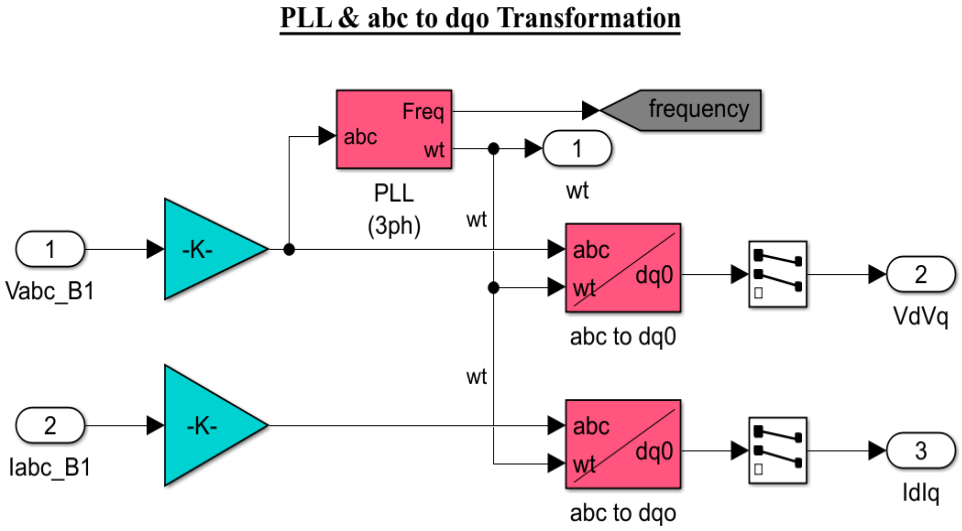

FIGURE 4.12: phase locked loop and DQ0 transformations

PLL and Measurements block represents the model designed for the dq transformation of converter three phase output currents and grid three phase output voltages. Three-phase PLL block is used to track the angle of the grid which is given to dqo transformation blocks to synchronize the dq frame.

This synchronization helps to transform the three phase currents and voltages to dq frame constant vectors. The output of this PLL and Measurement block are; grid angle ωt, dq frame grid voltage and currents v_d and v_q and I_d and I_q respectively. Figure 4.12 shows this block.

Phase locked loop performs in accordance with the discussion made in section 4.6. The angle with which PLL synchronizes the grid space phasor and dq reference frame is shown in Figure 4.13 (a), Figure 4.13 (b) represents grid frequency tracked by PLL thus showing a fast and smooth response by the PLL compensator. The grid is synchronized with the converter as the converter current and grid voltage for phase A are in phase with each other which can be shown in Figure 4.13 (c).

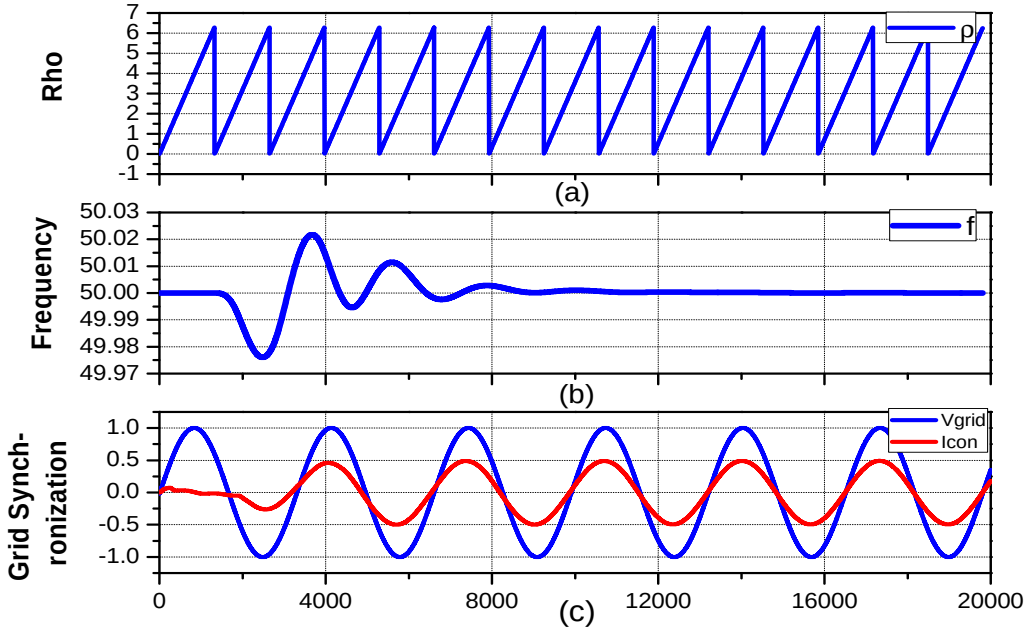

FIGURE 4.13: (a) Grid angle (b) PLL grid frequency tracking (c) Synchronization of Grid voltages and converter currents

The Specifications of PLL block that are utilized in Simulink block are provided in the Table 4.4.

TABLE 4.4: Specifications of Phase Locked Loop [52]

Description	Symbol	Value
Proportional Gain	K_p	180
Integral Gain	K_i	3200
Differential Gain	K_d	1
Minimum Frequency	f_0	50 Hz
Sampling time	T_s	$6.06e^{-5}$s
Sampling frequency	f_s	3300Hz

The three phase AC signals are normalized before these signals are fed into the transformation block. Figure 4.14 (a) and 4.14 (c) represent the normalized three phase grid voltages and converter output currents respectively. The grid voltages are normalized by a factor of $1/(V_{nompri} * sqrt(2)/sqrt(3))$ whereas converter three phase currents are normalized by the factor of $(V_{nompri} * sqrt(3)/P_{nom}/sqrt(2))$.

These normalized values are fed to dq0 transformation blocks along with the grid tracking angle tracked by phase locked loop which ensures the alignment of dq reference frame with grid voltage phasor. As a result the dq transformed grid voltages are presented in Figure 4.14 (b) and dq transformed converter currents are presented in Figure 4.14 (d). It can be seen that both dq0 transformed currents and voltages are pure DC vectors.

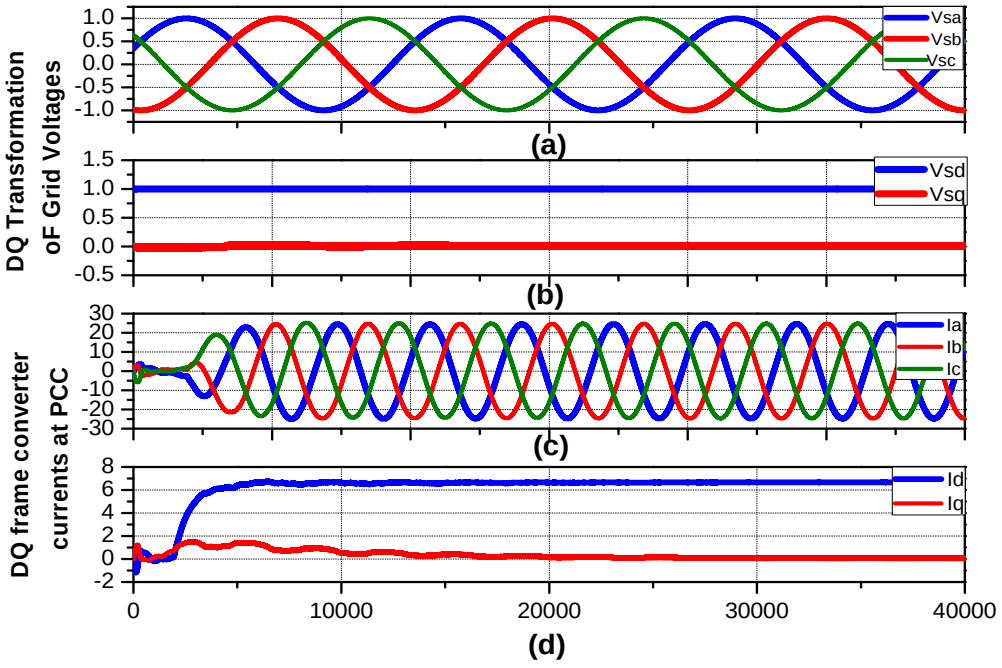

FIGURE 4.14: (a) Three phase grid voltages, (b) DQ frame grid voltages, (c) three phase converter terminal currents (d) DQ converter currents.

The parameters that are utilized for DQ0 transformations are presented in Table 4.4 with their specifications

TABLE 4.5: Specifications of Parameters used in Dq0 Transformations

Description	Symbol	Value
Nominal Base Power	P_{nom}	1MVA
Nominal Primary voltage	$V_{nomprim}$	220kV
Nominal Secondary voltage	V_{nomsec}	52.051kV
3 phase normalized grid voltages	V_{abc}	2
3 phase normalized converter voltages	I_{abc}	14.03
D-axis grid voltage	V_d	1
Q-axis grid voltage	V_q	0
D-axis converter current	I_d	7
Q-axis converter current	I_q	0
sampling frequency	f_s	3300Hz

Now after that we achieved the pure DC signals in DQ0 reference frame, these signals are provided to the inner current control loop where the active and reactive power are independently controlled by their respective active and reactive current components.

The structure of inner control loop developed for the decoupled control of active and reactive current on the basis of dq0 model of three phase VSC system [66, 67] is presented in Figure 4.15. It constitutes two PI controllers, one for d-axis current and the other for q-axis current.

At input the error e_d/e_q between the reference I_d^*/I_q^* and measured I_{dmeas}/I_{qmeas} and then these corresponding d/q errors are fed to the compensator as input.

The error e_d/e_q is processed by the controller $K_d(s)/K_q(s)$ and at output produces the converter output voltages V_{td}/V_{tq} in the d/q reference frame. The feed forward

terms are added at the controller output on the basis of 4.24 and 4.25 to ensure the decoupled control in dq reference frame .

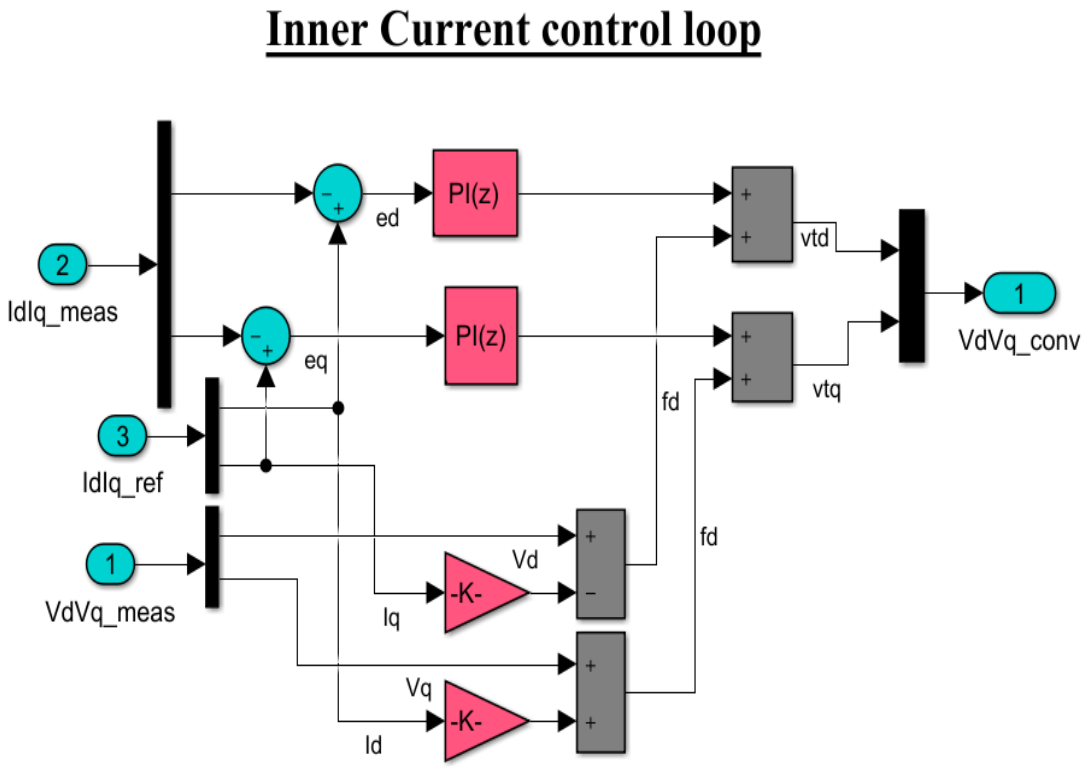

FIGURE 4.15: Inner Current Control of VSC in DQ reference Frame

The schematic that has been used to generate the reference values of active and reactive power follows the use of Signal builder blocks in Simulink. Two signla builders are used, one for active power and the other for the reactive power. However the reactive power is kept at zero reference value to regulate the converter reactive at 0VAR throughout the simulation which employs that converter neither absorbs nor generates reactive power. Whereas active power signal is generated by using a square wave signal in which various changes are subjected to the active power control loop.

Figure 4.16 shows the generation of reference signals for the d/q component of current based on 4.11 and 4.12 and presented in the form of simulation model. As we have discussed earlier, the independent control implies that the change in reference for the active and reactive power corresponds to the change in reference values of active and reactive currents.

Thus by controlling the d and q components of current we can independently control the active and reactive power at point of common coupling (PCC). This control strategy is known as Direct Power Control DPC at PCC [66, 67].

The half nominal DC link voltage is divided by the nominal secondary voltage, this normalizes dc link voltage $V_{dc}/2$ [1]. When the converter output voltages V_{td}/V_{tq} are divided by normalized $V_{dc}/2$ we get reference modulation signals m_d/m_q in dq reference frame. Where m_d corresponds to the amplitude and m_q corresponds to the phase angle of the converter output voltage in dq-frame.

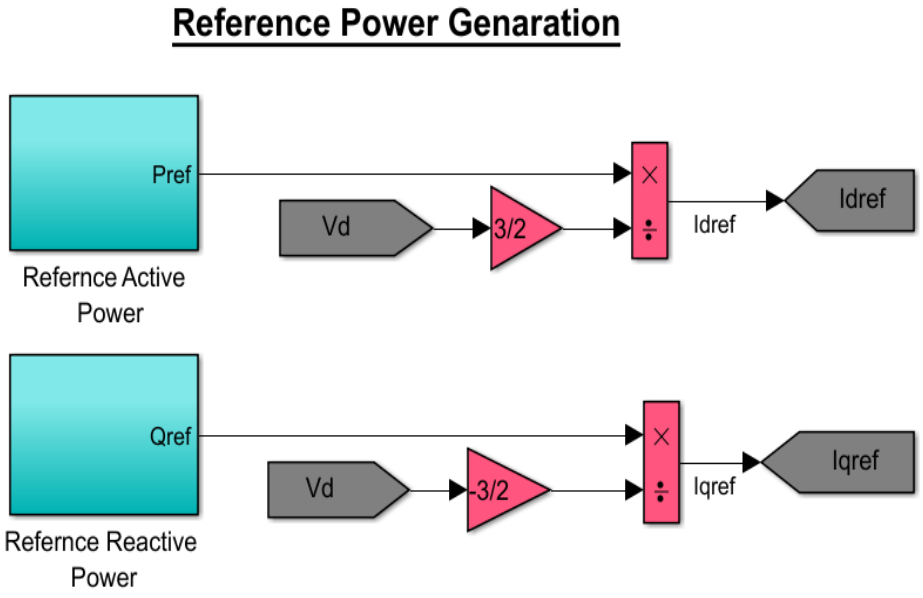

FIGURE 4.16: Simulation Model for the generation of Active and Reactive Power References.

The dq frame modulation signals are then transformed to three phase reference modulation signals $m_{abc}(t)$, which are phase displaced by 120^0 by using dq0 to *abc* frame transformation block from Simulink Simscape library.

The three phase reference modulation signals are later used by PWM block to generate gating pulses for the control of semiconductor switching devices in corresponding 2-level grid tied VSC and 21-level grid tied MMC. Figure 4.17 represents the transformation of dq frame modulation signals to three phase modulation signals.

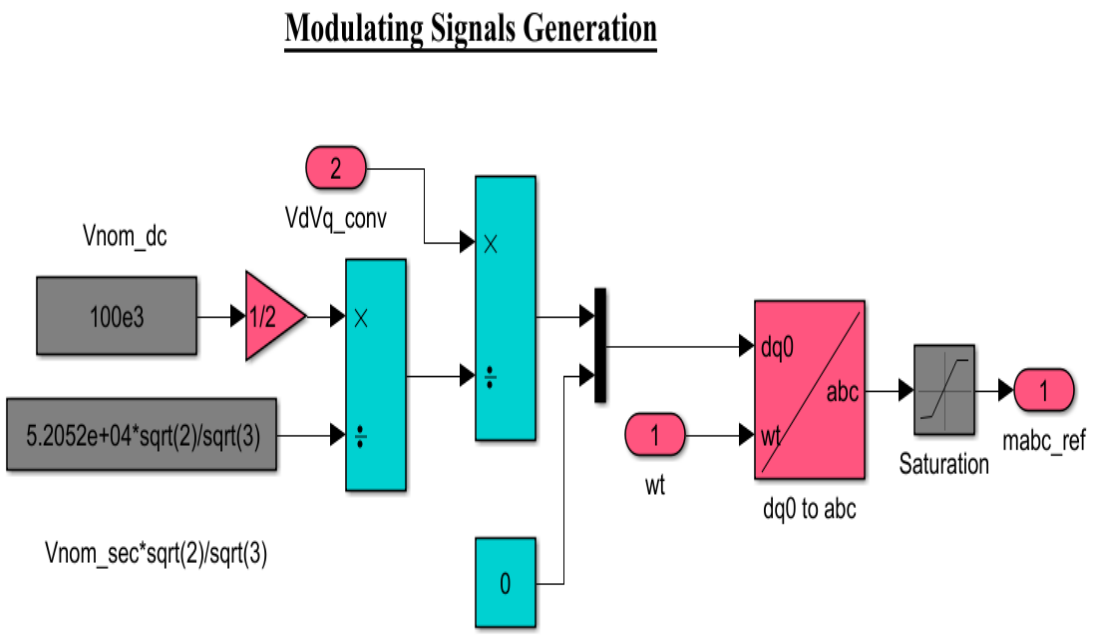

FIGURE 4.17: The transformation of DQ0 signals to ABC reference frame for generation of modulation signals

As long as signals stay inside the control loop both systems methodology towards control was same but after we have got the modulation signals than both systems adopt their own methodology for the generation of switching signals.

The three phase modulation signals for two-level VSC are represented in Figure 4.18 (a) whereas Figure 4.18 (b) represents the three phase modulation signals for 21-level MMC.

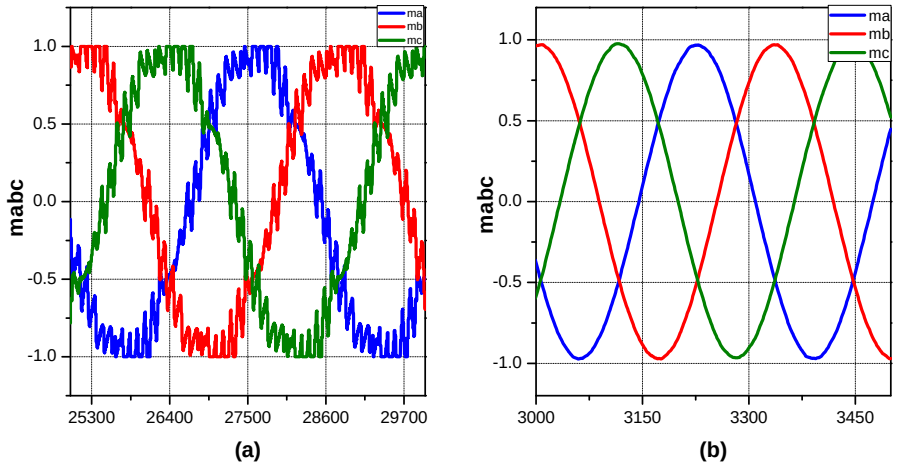

FIGURE 4.18: Modulating Signals (a) 2-Level VSC (b) 21-Level MMC.

The gating pulses for two-level three-phase VSC are generated by using the PWM generator block (two-level) from Simscape Simpower library and it is shown in Figure 4.19.

It takes the three phase modulation signals as reference signal which is generated by the control system and compares them with the high frequency carrier waves to generate the six switching pulses for the control of six switching devices in a conventional three phase VSC.

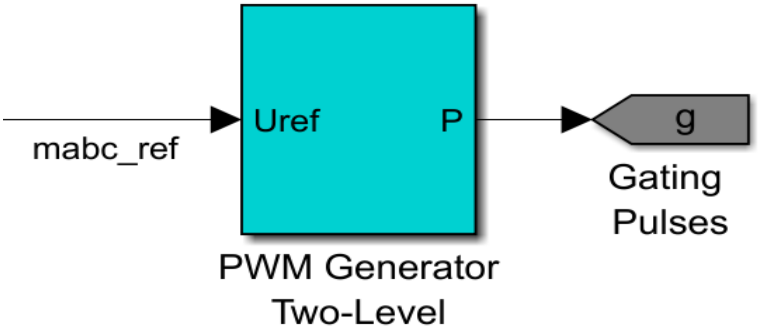

FIGURE 4.19: PWM generator model for 2-level VSC in Simulink

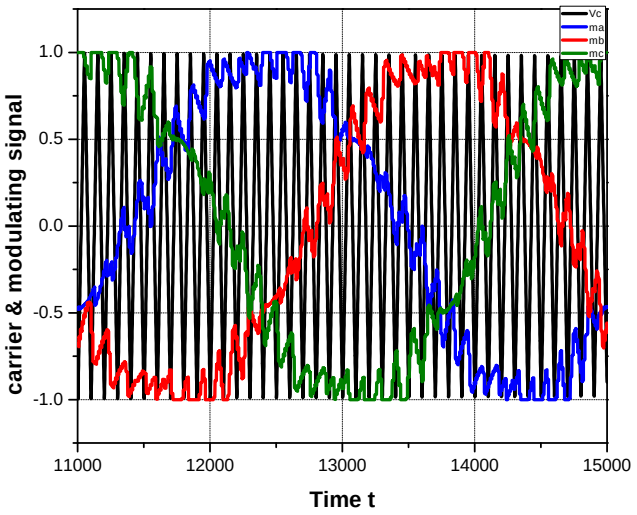

FIGURE 4.20: Three-phase modulation signals with a triangular carrier wave 2-level VSC PWM

The three phase reference modulation signals $m_{abc}(t)$, having fundamental frequency 50Hz and amplitude varying between 1 and -1, are compared to the carrier waves, with frequency 1650Hz and amplitude swinging between 1 and -1, by the PWM generator which is shown in Figure 4.20

As a result switching pulses are generated for the control of each IGBT in each phase. Each phase comprises two IGBTs in each submodule, therefore for the switching of each IGBT in a single phase, two switching or gating pulses are required.

These gating signals are generated in a complementary manner to avoid the short circuit of DC sources . The switching pulses are shown in Figure 4.21 where S_1S_{1bar}, S_3S_{3bar} and S_5S_{5bar} are the switching pulses for three phase two-level VSC.

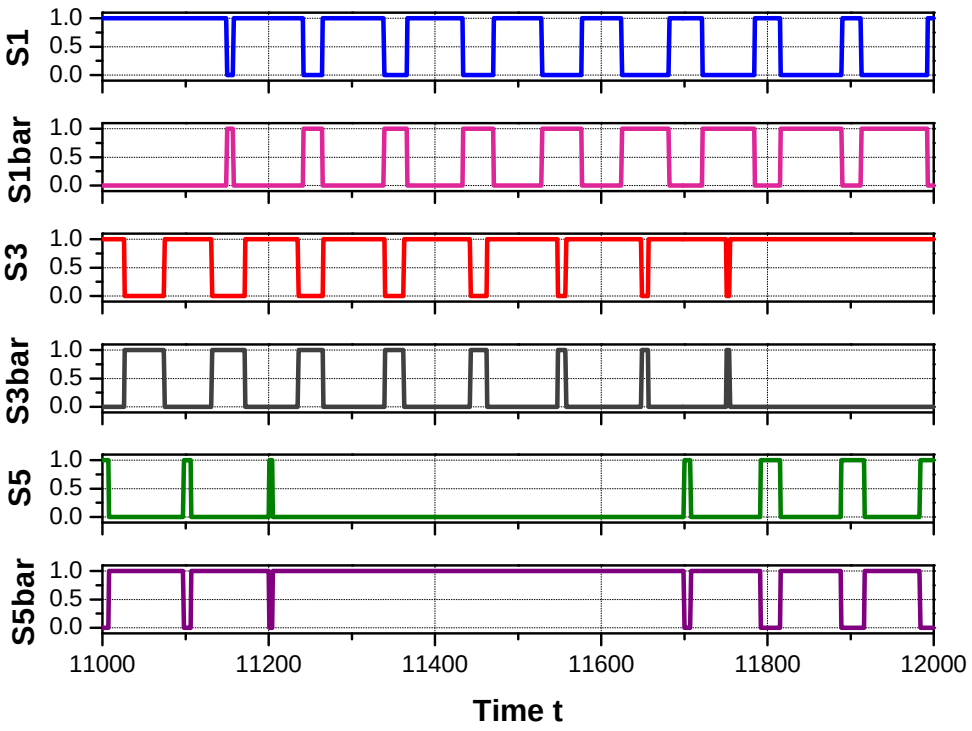

FIGURE 4.21: Gating signals generated by PWM generator block for 2-level three-phase VSC

The parameters used for the generation of switching signals by using sinusoidal pulse width modulation for two-level three phase VSC are specified in Table 4.6.

TABLE 4.6: Specifications for SPWM for VSC

Description	Symbol	Value
Modulation frequency	f	50Hz
Amplitude Modulation Index	$\hat{m}$	0.85
Carrier frequency	f_c	1650Hz
Frequency Modulation Index	m_f	33
Total switching signals per phase	N_s	2
Total switching signals in 3 phase	N_{st}	6
Sampling Time	T_s	$6.06e^{-6}$s
Sampling frequency	f_s	3300Hz

The switching signals for 21-level MMC are generated by using PWM generator (multilevel) block from Simscape Simpower library. These signal generator blocks generate switching pulses on the pattern of phase shifted pulse width modulation PSPWM where twenty half bridge submodules are switched at the switching frequency of 1650Hz.

Each PWM signal generator takes the single phase reference modulation signal and produces carrier waves equal to twice the number of submodules that are provided to the signal generator block. For three phase 21-level modular multilevel converter the Matlab/Simulink block uses three PWM generator blocks as shown in Figure 4.22.

For 21-level MMC the PWM generator block uses twenty carrier waves which are phase displaced by 18^0 calculated on the basis of 4.36. The amplitude of modulation signal, being a sinusoidal signal, varies between 1 and -1 having 50Hz frequency.s

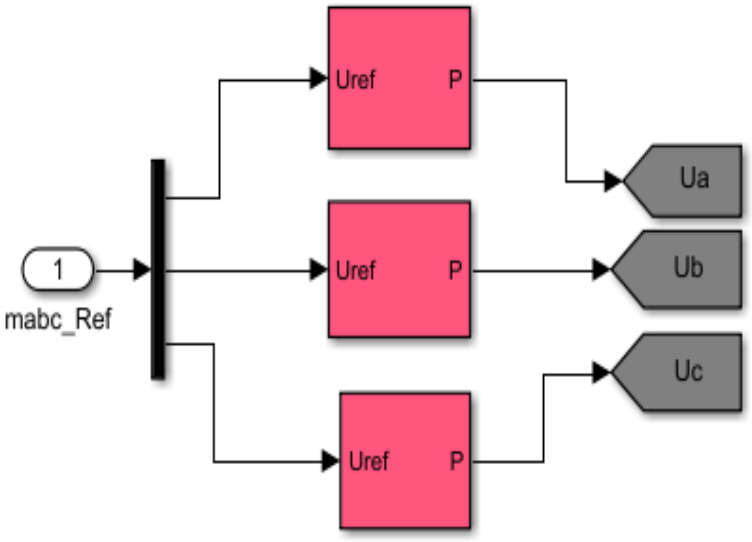

FIGURE 4.22: PSC-PWM generator model for Modular Multilevel Converter in Simulink

Whereas each carrier signal swings between 1 and -1 having 1650Hz frequency. Each carrier waveform with the reference modulation signal for phase A 21-level modular multilevel converter are shown in Figure 4.23.

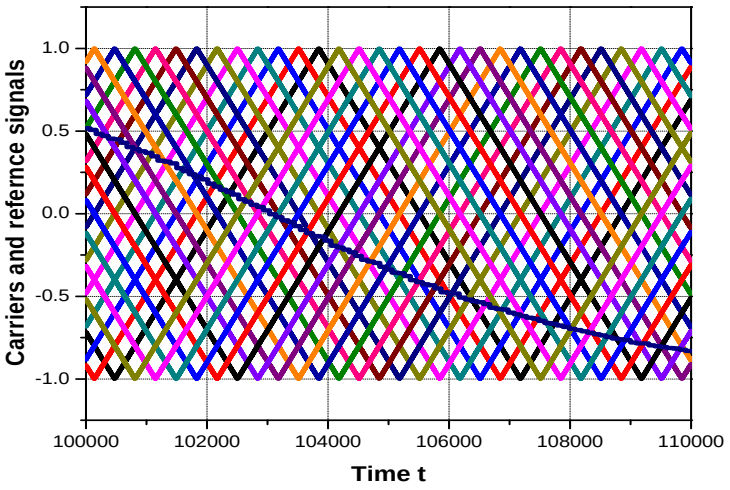

FIGURE 4.23: PSC-PWM with reference modulation signal and carrier waves

The parameters for the generation of switching signals by using phase shifted pulse width modulation in 21-level three phase MMC are specified in Table 4.4

TABLE 4.7: Specifications of the parameters of PSC-PWM for 21-level MMC

Description	Symbol	Value
Number of carriers	N	20
Phase displacement per carrier	ϕ	18^0
Total switching signals per phase	N_s	40
Total switching signals in 3 phase	N_{st}	240
Modulation frequency	f	50Hz
Amplitude Modulation Index	$\hat{m}$	0.85
Carrier frequency	f_c	1650Hz
Frequency Modulation Index	m_f	33
Sampling Time	T_s	$6.06e^{-6}$s

The modular multilevel converter uses series connected half bridge submodules where each submodule comprises two switching cells in its single phase leg, both of which operate in complementary manner therefore each submodule requires two switching signals which are opposite to each other.

As the single arm of the 21-level MMC comprises twenty series connected half bridge submodules therefore the model generates forty switching pulses for each arm in a three phase MMC. The forty switching signals for one arm are inverted to be used for the switching of other arm in the same converter phase leg.

Figure 4.24 shows first ten switching signals generated for the switching of first ten series connected Submodules in MMC upper arm phase leg A, where each switching signal is phase displaced by 18^0 due to which each submodule switches by the delay angle of 18^0 during phase shifted pulse width modulation in 21-level MMC

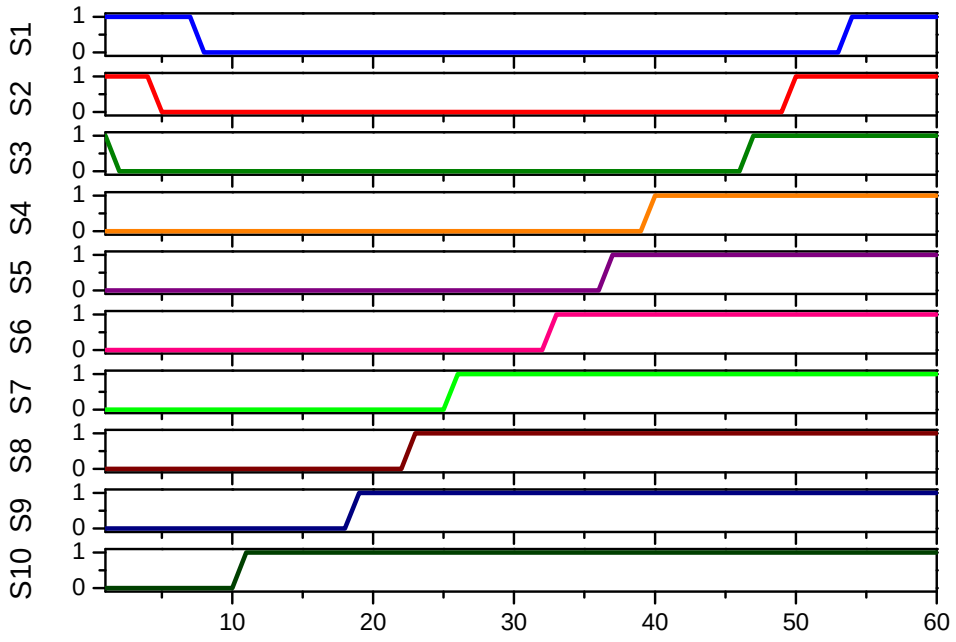

FIGURE 4.24: First ten switching signals for the switching of first ten series connected submodules in 21-level MMC upper arm phase leg A.

4.11 Chapter Summary

This chapter discusses all the control aspects of both converter topologies including the dq-modeling, design of inner current control loop and control of switching devices. Later the models discussed in earlier sections in this chapter, are presented towards by simulation models developed in Matlab/simulink 2016b for each converter topology.

Chapter 5

Simulations and Results

5.1 Introduction

This chapter involves the discussion of the results evaluated by the comparison of conventional two-level grid tied VSC (GTVSC) and 21-level (GTMMC). The results are produced using Matlab/Simulink 2016b environment where a case study is developed to test both converters regarding their performance towards reference command tracking and output power quality. To simplify the analysis, two cases are defined; Case A and Case B, where Case A corresponds to the comparative analysis of 2-level GTVSC and 21-level GTMMC on the basis of converter output power quality and Case B corresponds to the analysis of stability and dynamic performance of control loops.

5.2 Case Description: Matlab/Simulink Model

For the analysis of conventional two-level GTVSC and 21-level GTMMC a case is developed by using the HVDC converter station operating in inverter mode of operation. To make analysis more practical and realistic, this thesis develops a 220kV, 50Hz AC grid interfaced with the converter through a phase reactor and a coupling transformer. Two split DC voltage sources $V_{dc}/2$ of 50kV are used

to provide the full DC link voltage V_{dc} of 100kV at the input of the converter. The Phase reactor R+jL = 0.04Ω+0.129H is used to provide the interface for the converter and the transformer. It also smooths out the harmonics from the converter output voltage and current waveforms [20].

The coupling transformer with Wye grounded Delta ($Y_g\triangle$) configuration is used between phase reactor and point of common coupling (PCC) as an interface between converter and grid to provide suitable voltage levels for the converter [54]. The primary side voltage V_{nompri} equals 220kV is stepped down by the transformer secondary at voltage V_{nomsec} equal to 52kV [1].

The AC grid is designed by using a three phase symmetrical voltage source with 220kV (r.m.s) voltage and 50Hz nominal frequency. Initially the power circulating in grid is 150MW when the converter is in standalone mode.

Two loads with equal power rating of 50 MW are used in parallel connection with two transmission lines of 10km distance in between and from Grid. Both converter topologies i.e. 2-level GTVSC and 21-level GTMMC are used and tested through the developed methodology.

A carrier wave with high frequency f_{sw} of 1650Hz is used for the switching of both converter topologies therefore the sampling frequency f_s of 100×1650Hz is chosen for the sampling of the entire system signals. The sampling time T_{spower} is thus chosen to be $6.06e^{-6}$s for the sampling of power signals whereas T_{scon} =$6.06e^{-5}$s is chosen for the sampling of control signals.

The bus B_1 represents the converter station output bus where converter output voltages and currents are measured, bus B_2 represents the point of common coupling (PCC) which is conjunction between converter and grid. Bus B_3 represents the grid side bus where grid voltages and currents are measured. The single line diagram of the described case is presented in Figure 5.1. The specifications of the entire system are summed up into Table 5.1.

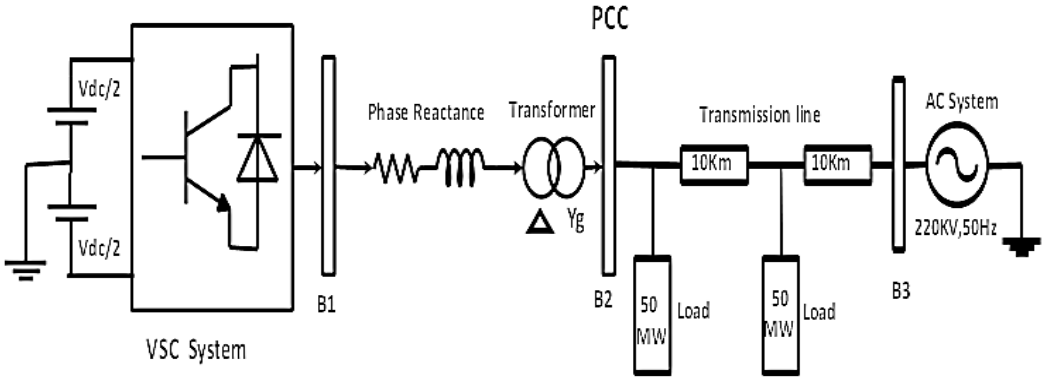

FIGURE 5.1: Single Line Diagram of the developed case study.

TABLE 5.1: System Specifications used to develop the Matlab/Simulink model

Description	Symbol	Value
Nominal Dc Link Voltage	V_{dc}	100kV
ConverterTerminal Voltage	V_t	50kV (V_{peak})
Phase Reactance	$R + jL$	0.04Ω+0.129H
Transformer primary Voltage	$V_{nomprim}$	220kV
Transformer secondary voltage	V_{nomsec}	52kV
Transformer Turns Ratio	$V_{nomprim}/V_{nomsec}$	0.85
Converter Switching Frequency	f_{sw}	1650Hz
Sampling time for power gui	T_{spower}	$6.06e^{-6}$s
Ac voltage	V_s	220kV
Transmission Line	$2 \times L$	2×10km
Parallel Connected Load	$2 \times L$	2×50MW
Grid Power in Stand Alone Mode	P_g	150MW
Ac system nominal frequency	f	50Hz

5.3 Simulation Model in Matlab/Simulink Environment

Under this section, simulation models for 2-level GTVSC and 21-Level GTMMC are presented which are designed in Matlab/Simulink environment using Simscape Simpower library. The Power GUI is used with sampling time $T_s = 6.06e^{-6}$s for the both of the entire Simulink models. The simulation run time for both of the models is t_{run}=1s. Figure 5.2 and Figure 5.3 represents the corresponding Simulink model for 2-Level GTVSC and 21-Level GTMMC respectively along with inner current control block and the scope section block. The converter control block presents the inner current control implemented by using PI compensator in dq reference frame as discussed in chapter 4 whereas scope section block is used to analyze the behavior of model parameters during the entire simulation period.

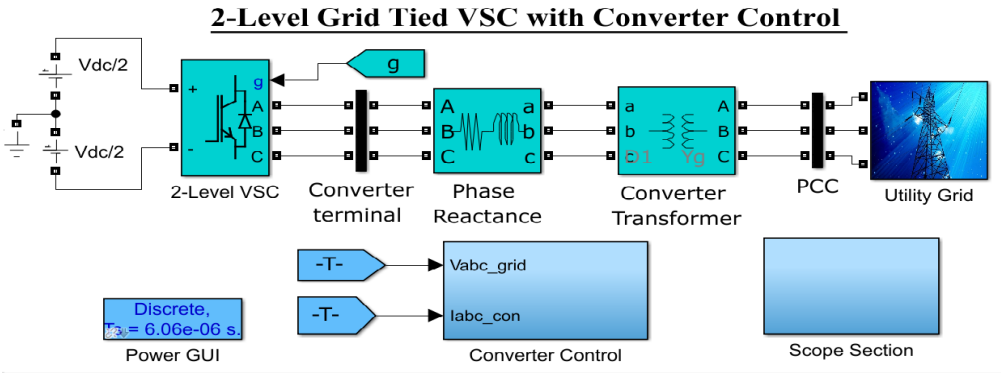

FIGURE 5.2: Simulink model of 2-Level GTVSC with inner control and scope section block

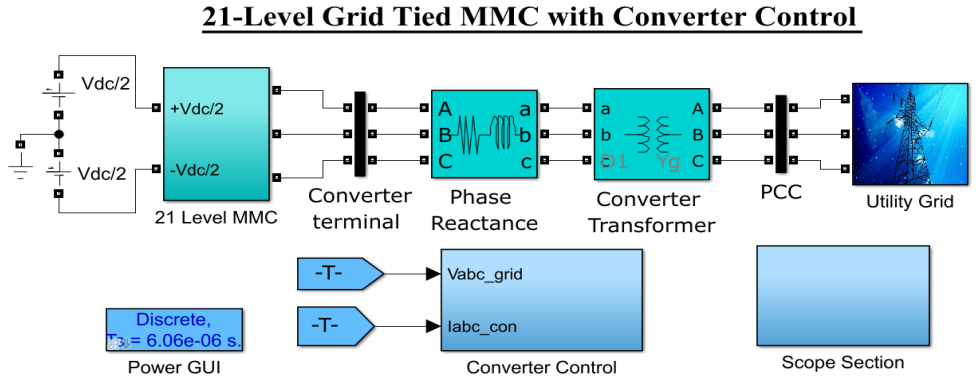

FIGURE 5.3: Simulink model of 21-Level GTMMC with inner control and scope section block.

5.4 Case A: Comparative Analysis of Converter Output Voltage Quality

The concept of power quality is versatile and it does not have any standard definition but in the current thesis the definition under consideration is, "Power Quality includes all those aspects of events due to which the performance of the system deviates from the normal operation" [72].

Case A is dedicated towards the comparison of quality of output voltage and current waveforms for both 21-level GTMMC and 2-level GTVSC where both topologies interfaced with grid are examined to make a comparative analysis.

This Case defines certain parameters in order to make a comparison between 2-level GTVSC and 21-level GTMMC, these parameters are; shape (measure of smoothness) of converter output phase voltage and current waveforms, harmonic spectrum, the respective harmonics with their order, total harmonic distortion (THD) in the output phase current and voltage waveforms, converter switching losses, costs and filter requirements by considering IEEE standard 519^{TM} [73].

5.4.1 Converter Output Voltage Shape

Figure 5.4(a) and Figure 5.4(b) represent the three phase output voltage waveforms for conventional 2-level GTVSC and 21-level GTMMC respectively, comprising peak to peak voltage $V_{(p-p)}$ of 100kV where V_p is the peak phase voltage and its value is 50kV. As it can be seen from Figure 5.4(a) that the three phase output voltage waveform for conventional GTVSC is crude having only two voltage levels i.e. $+50$kV & -50kV and if it is compared to a pure sinusoidal waveform, it is only providing high and low voltage levels of full DC-link voltage.

Figure 5.4(b) shows that the three phase output voltage waveform of 21-level GTMMC is smooth and almost sinusoidal, comprising twenty one voltage steps

each. In 21-level GTMMC each voltage step takes its equal share of 5kV which is equal to the 20^{th} part of full DC link voltage of 100kV.

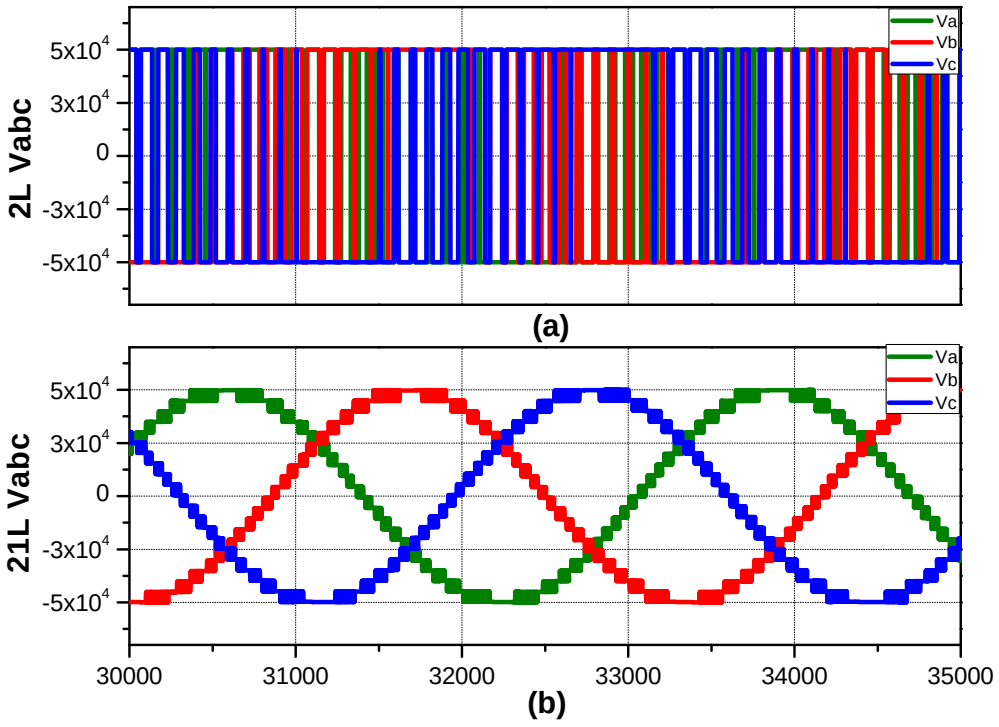

FIGURE 5.4: Three phase converter output voltages (a) 2-level GTVSC (b) 21-level GTMMC

Figure 5.5(a) and Figure 5.5(b) shows a more clear view of converter output voltage by presenting single phase output voltage waveform over one complete cycle for two-level GTVSC and 21-level GTMMC respectively. The output voltage of two level GTVSC shows that the converter is hard switched i.e. the converter output switches at full DC-link voltage of 100kV whereas the 21-level GTMMC is comparatively soft switched where each submodule switches according to its share i.e. at 5kV.

Hard switching renders high switching losses, higher values of dv/dt which in turn at higher switching frequencies generate enormous amount of electromagnetic interference (EMI) noise in two-level VSC. In 21-level MMC, switching at lower

voltage levels reduces switching losses and renders lower values of dv/dt which is in huge interest to produce a high quality output voltage waveform .

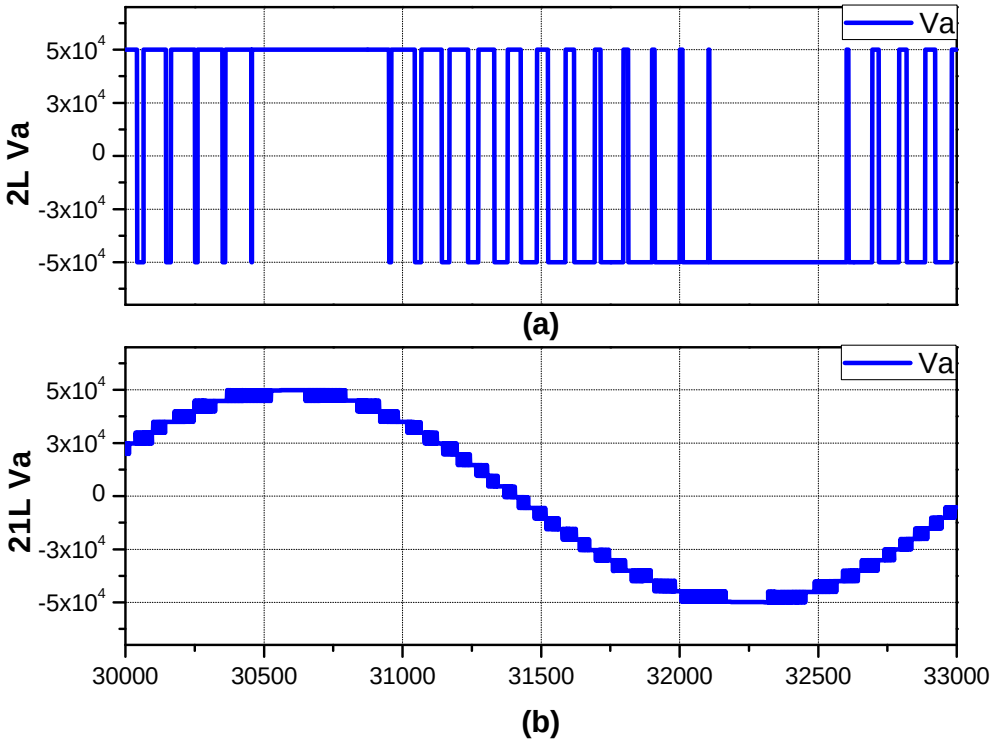

FIGURE 5.5: 1-cycle of output phase A voltage (a) 2-level GTVSC (b) 21-level GTMMC

Figure 5.6 shows the single phase output voltage waveform of 21-level GTMMC, it can be noticed that every single step comprises 5kV voltage, giving peak to peak voltage (V_{p-p}) of 100kV and peak voltage V_p = 50kV at the output of 21-level MMC. The equal voltage of 5kV in each step indicates that the voltages across all capacitors in the series connected submodules are well balanced.

Phase shift pulse width modulation (PSPWM) using high carrier frequency f_{sw} of 33× fundamental frequency provides natural voltage balancing across each capacitor in all series connected submodules. Therefore even without using complex capacitor voltage balancing algorithms, capacitor voltages did not come across the trouble of voltage imbalance where each capacitor maintains its respective voltage level efficiently.

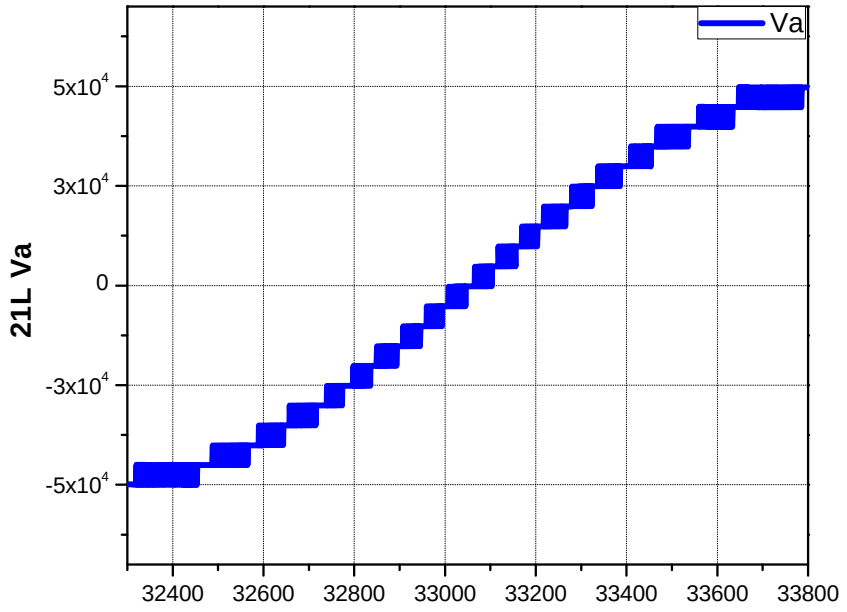

FIGURE 5.6: Magnified view of levels of output voltage of 21-level GTMMC

5.4.2 Voltage Harmonic Spectrum

In this section the output phase voltages and currents for 2-level VSC and 21-level MMC respectively are analyzed and compared on the basis of the harmonic content present in the corresponding waveforms. The Fast Fourier Transform (FFT) Analysis tool in the Power GUI block is used to perform the FFT of both converters ′ waveforms in Simulink 2016b simulation model. The sampling time T_s equals $6.06e^{-6}s$ whereas the sampling frequency f_s of 3.3kHz are used by the FFT window to perform signal processing. FFT was performed on 1 cycle of output voltage and current waveforms for both converter topologies.

The converter output voltage and current waveforms are analyzed at full load conditions to better analyze the performance of both converters tied to the grid. Therefore keeping reactive power Q zero, active power P is changed from 0 to 10MW at 0.1s. When the system reached steady state than at 0.2sec the FFT analysis was performed.

The fundamental frequency f was chosen to be 50Hz. The harmonic spectrum expanded over the range of 0 to 10kHz frequency. The x-axis displays the harmonic order whereas y-axis displays the % magnitude of the fundamental component i.e. 50kV. The harmonic analysis was performed by ensuring that all the parameters are strictly same for both of the converter models in FFT window. All of these parameters are summarized in Table 5.2.

TABLE 5.2: Parameters used for FFT Analysis of phase voltages of 2-level VSC and 21-level MMC

Description	Symbol	Value
Fundamental frequency	f	50Hz
Fundamental component magnitude	V_p	50kV
Switching frequency	f_{sw}	1650Hz
frequency modulation Index	m_f	33
Sampling time	T_s	$6.606e^{-6}s$
Number of samples per cycle	f_s	3.3kHz
FFT over Number of Cycles	N_f	1cycle
FFT over time instant	T_f	0.2s
X-axis maximum harmonic order	h	200≈1k0Hz
Y-axis maximum magnitude	$\%mag$	100
Maximum load	L_m	10MW

The harmonic spectrum obtained by using FFT Analysis tool are presented in Figure 5.7 and Figure 5.8 for output phase voltage of two-level VSC and 21-level MMC respectively. As Both figures are produced on the same scale in order to make the clear comparison between harmonic spectrum of both converters' output phase voltage waveforms therefore this analysis provides with the vivid picture of how high the harmonic content is, which actually resides in the crude AC output voltage waveform of 2-level VSC.

However the harmonic spectrum of 21-level MMC did not show any significant amount of harmonic content whose amplitude could hardly get higher than 0.2% over the same range of frequencies on x-axis.

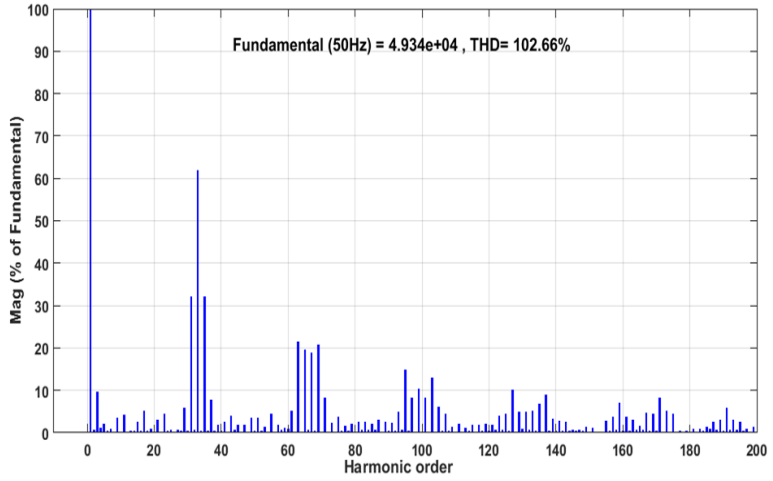

FIGURE 5.7: Voltage Harmonic spectrum of 2-level GTVSC

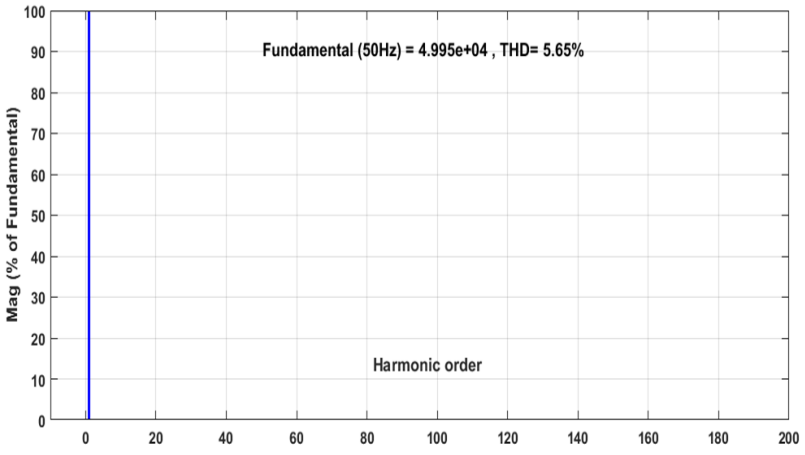

FIGURE 5.8: Voltage Harmonic spectrum of 21-level GTMMC

From Figure 5.7, it is clear that, in two level VSC the first harmonic component which contributes 61.98% of the fundamental component, is lying at $n \times m_f \pm k \approx 1 \times 33 \pm 2$ i.e. 33 ± 2. The second harmonic is present at $2 \times 33 \pm 3 \approx 66 \pm 3$ and its

magnitude decreases to 32% of fundamental component. The magnitude of higher order harmonics decreases with the increase in value of n with SPWM [40].

The harmonics in the output phase voltage of N+1 level MMC by using PSPWM modulation technique, are present at the order of $n \times N \times m_f$ where n is the integer and can take values from $\{1, 2, 3, ...\}$, N is the number of series connected submodules in converter arm and m_f is the frequency modulation index [7].

As in Figure 5.8 only fundamental component can be viewed therefore to further analyze the presence of harmonics in output voltage waveform of 21-level MMC, the range of frequencies on x-axis is broadened from 10k t0 40kHz. Figure 5.9 represents the harmonic spectrum of output phase voltage of 21-level MMC over a broader frequency range as compared to the range used in Figure 5.8.

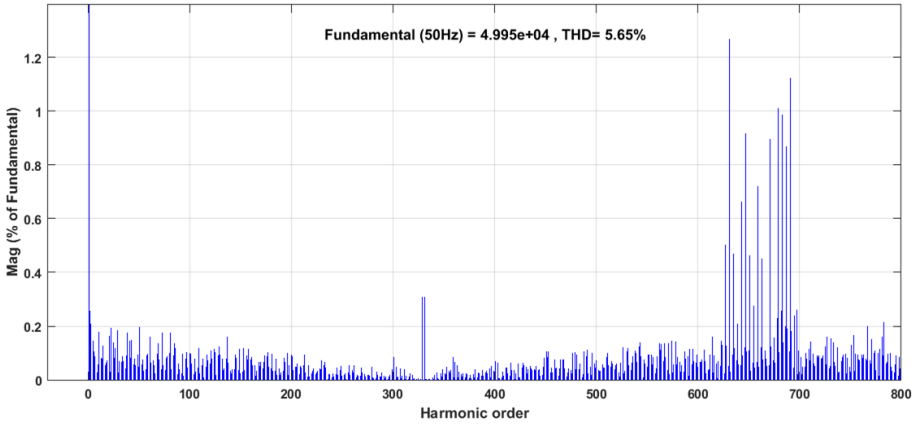

FIGURE 5.9: Harmonic spectrum of output voltage of 21-level GTMMC over a broad frequency range

From Figure 5.9, it can be clearly analyzed that the very first harmonic component present in the output phase voltage of 21-level MMC is residing at the harmonic order (h) of round about 660 i.e 33kHz and comprising 1.27% magnitude of the fundamental component which constitutes highest value among all the harmonics which are found present in 21-level MMC output voltage waveform.

These high order frequency harmonics comprising such a low level of magnitude goes in favor of 21-level modular multilevel converter to be utilized in high power high voltage applications because this converter has eradicated the need for bulky

and expensive filters required for the power quality improvement at point of common coupling in HVDC systems.

5.4.3 Harmonic Order in Converter Output Voltage

To further analyze the harmonic spectrum of output voltage for both converter topologies, the harmonics are analyzed statistically to verify that which of the harmonic orders dominate, and how much they contribute in the output voltage waveform for both converter topologies.

Figure 5.10 shows that the two-Level output voltage waveform is dominated by 75% of various different harmonics and 25% of the fundamental component. Using higher switching frequency even could not eliminate the low order harmonics among which the dominant low order harmonics are h_3, h_5, h_9, h_{11}, h_{15}, h_{17}, h_{19}, h_{21} and h_{23}. The contribution of these harmonics in the magnitude of output voltage can be clearly visualized in Figure.5.11.

On contrary, in 21-level MMC output voltage waveform the fundamental harmonic component contributes $\approx 95\%$ whereas the other harmonic components contribute only the $\approx 5\%$. According to **IEE standard** $519^{TM} - 2014$ [73], the recommended practice and obligation for the control of harmonics in electric power systems is provided in Table 5.3.

TABLE 5.3: IEEE Standard $519^{TM}2014$ [73]

PCC Bus Voltage	Single Harmonic	THD
V $\leqslant$ 1.0kV	5.0%	8%
1kV $\leqslant$ V $\leqslant$69kV	3.0%	5.0%
69kV $\leqslant$ V $\leqslant$ 161kV	1.5%	2.5%
161kV $\leqslant V$	1%	1.5%

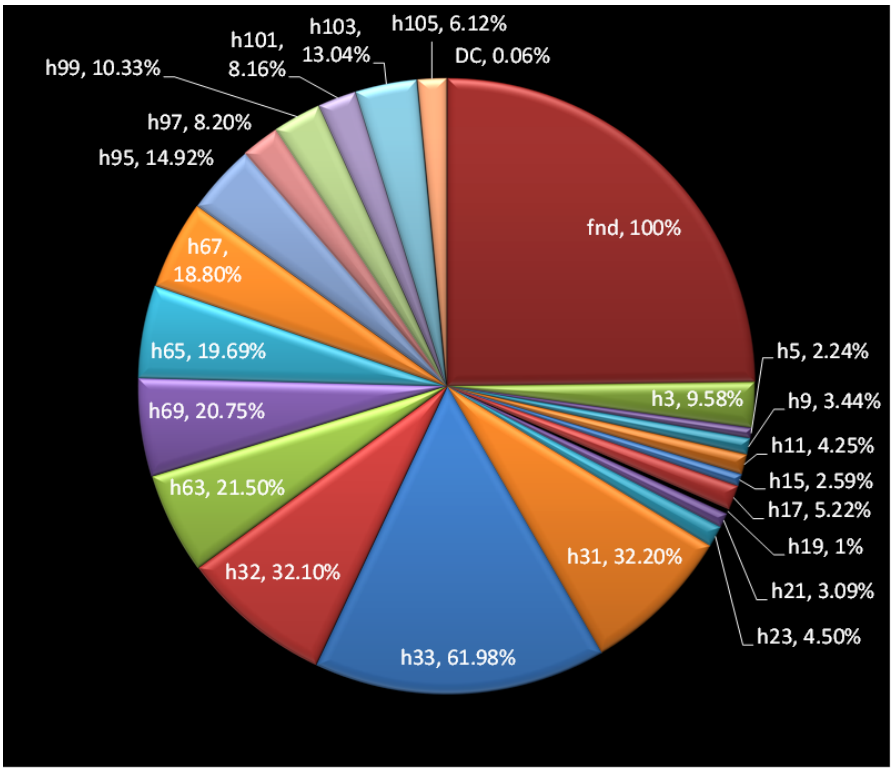

FIGURE 5.10: Two-level Voltage with individual harmonics and their magnitudes

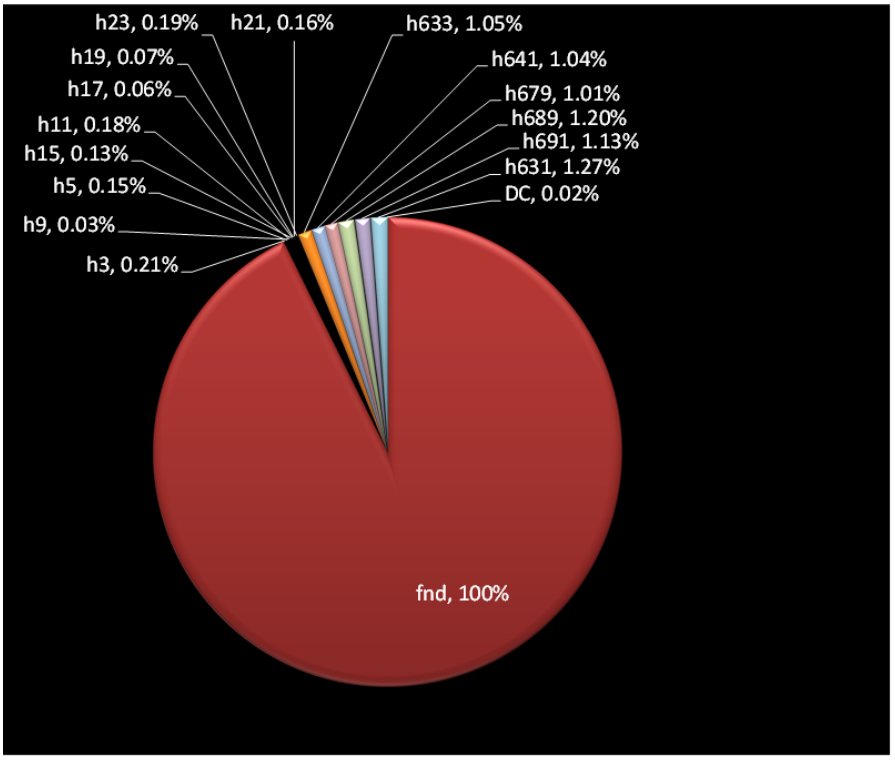

FIGURE 5.11: 21-level Voltage with individual harmonics and their magnitudes

For system voltages $\geq$ 161kV at PCC, the individual harmonic level must be $\leq$ 1% and the total harmonic distortion of the system must be $\leq$ 1.5% to avoid filter requirements. The two level VSC does not meet both requirements, as the maximum magnitude offered by the individual harmonic is 61.98% and the total harmonic distortion sums up to be 102% with the switching frequency of 1650Hz.

Figure 5.15 shows that 21-level MMC in a grid tied environment offers the maximum individual harmonic of 1.27% and total harmonic distortion of 5.68% in its output voltage.

The use of ΔY transformer configuration interestingly reduces the amount of total harmonic distortion up to 0.27% in case of conventional VSC and 0.02% in case of MMC. As Δ secondary transformer does not allow the passage of harmonics to Y primary hence these harmonics are dissipated as heat in the Δ winding.

Higher harmonics cause heating of transformer which in turn causes huge losses in transformers. Therefore to remove the huge harmonic content two-level output voltage the use of AC harmonic filters is indispensable for the improvement of power quality and for the safe operation of transformer also.

However, as the harmonic content in the output voltage waveform is quite low and meets the IEEE standard 519^{TM}2014 in case of single harmonic distortion therefore the transformer performance may not get bothered much with such a low level of total harmonic distortion present in MMC output voltage.

This analysis proposes that 21-level MMC tied to the grid through a phase reactor and ΔY transformer does not require AC harmonic filters at PCC as the power quality is with in the limits and in accordance with the IEEE standard 519^{TM}.

5.4.4 Converter Output Current Shape

In 21-level MMC, the soft switching of each submodule ends with a ripple free converter output phase currents. In contrast, the 2-level VSC uses high switching frequency of 1650Hz which switches each IGBT in converter arm 1650 times per

cycle at full DC-link voltage. This introduces large ripples in converter output current waveforms. The smooth and ripple free currents are desired on the utility side to avoid overheating and other losses in the electrical drives and processes.

Figure 5.12 (a) shows three phase output current of 2-level VSC and Figure 5.12 (b) shows the three phase output current waveforms of 21-level MMC where both converter topologies are analyzed and compared on the basis of smoothness and amount of ripple content present in the converter output current waveforms.

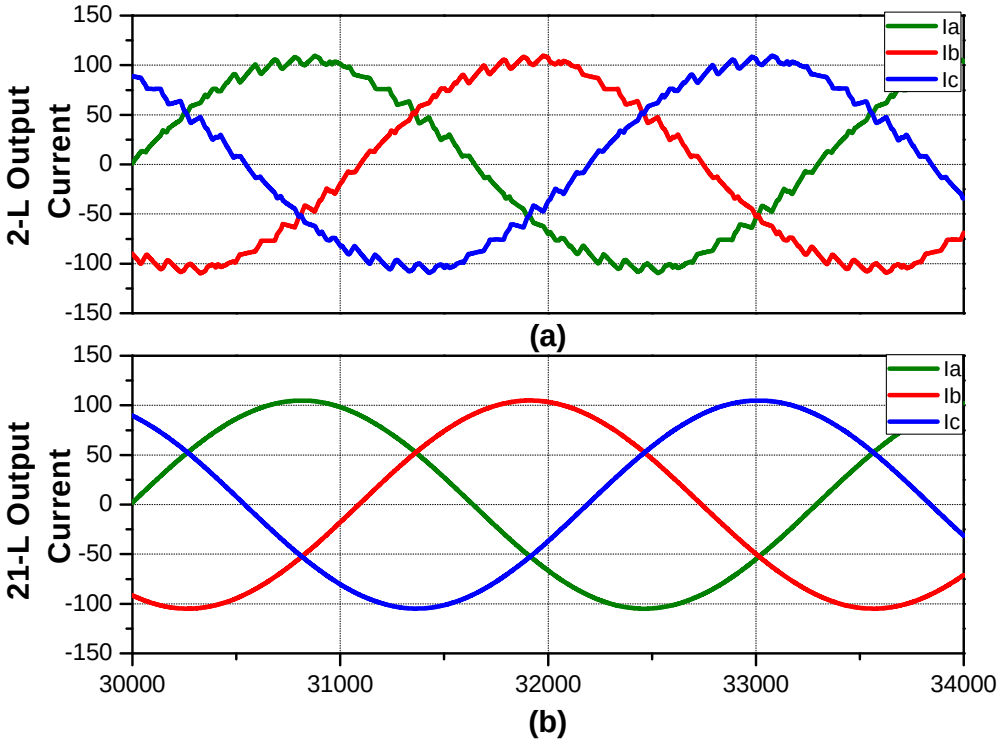

FIGURE 5.12: Three phase converter output currents (a) 2-level VSC (b) 21-level MMC

5.4.4.1 Converter Current at PCC

The quality of converter current for output " phase a " is analyzed at point of common coupling (PCC) for both converter topologies i.e. 2-level VSC and 21-level MMC and the graph is provided in Figure 5.13 (a) and Figure 5.13 (b). It can be clearly viewed that even after being passed through the line reactor and

coupling transformer which are meant to smooth out the current harmonics and ripple content, still the current waveform of 2-level VSC is unable to achieve a smoothness, showing a good amount of ripple content.

On the other hand, the output current waveform of 21-level MMC is smooth enough and ripple free therefore it does not require any further processing. It is proposed that 21-level MMC does not require filters to smooth out the output current waveform.

Whereas 2-level VSC, despite of using high switching frequency still requires AC harmonic filters between the phase reactor and coupling transformer to further smooth out the current waveforms so that the harmonics in current does not enter the AC system through PCC.

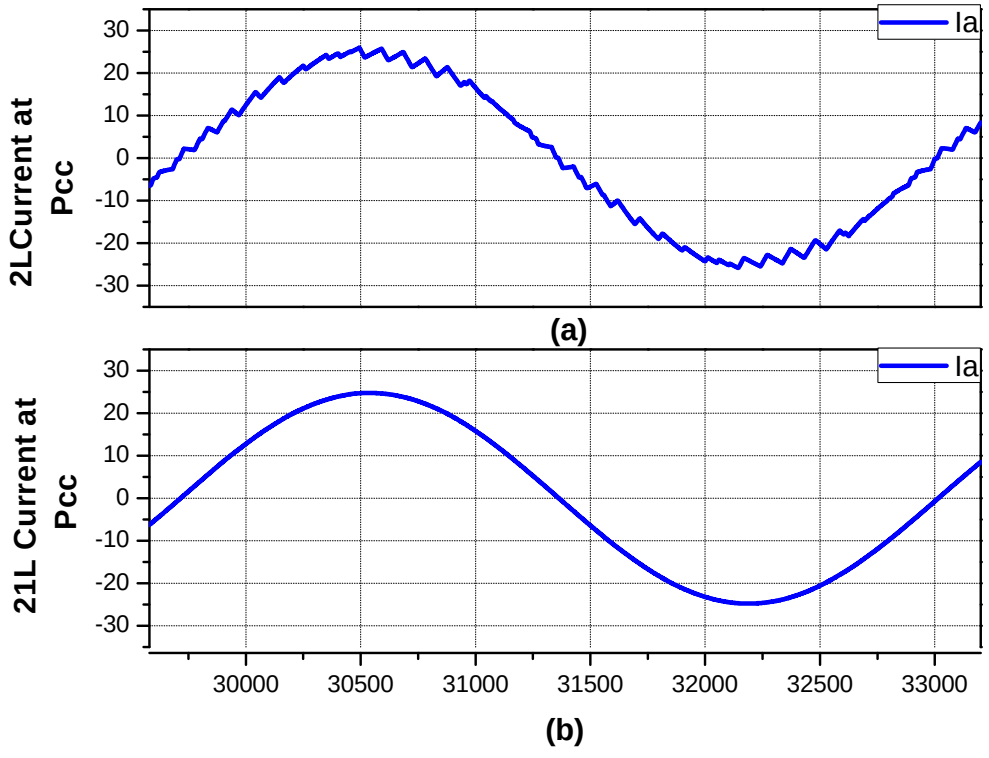

FIGURE 5.13: (a) output phase current of 2-level VSC at PCC (b) output phase current of 21-level MMC at PCC

5.4.5 Converter Output Current Harmonic Spectrum

The output current harmonic spectrum are also analyzed for both converter topologies under the same Matlab/Simulink environment by using the FFT Analysis tool box. The harmonic spectrum of 2-level VSC output current is presented in Figure 5.14 where among all harmonics the 5^{th} harmonic dominates with the highest magnitude of 1.51% of fundamental component.

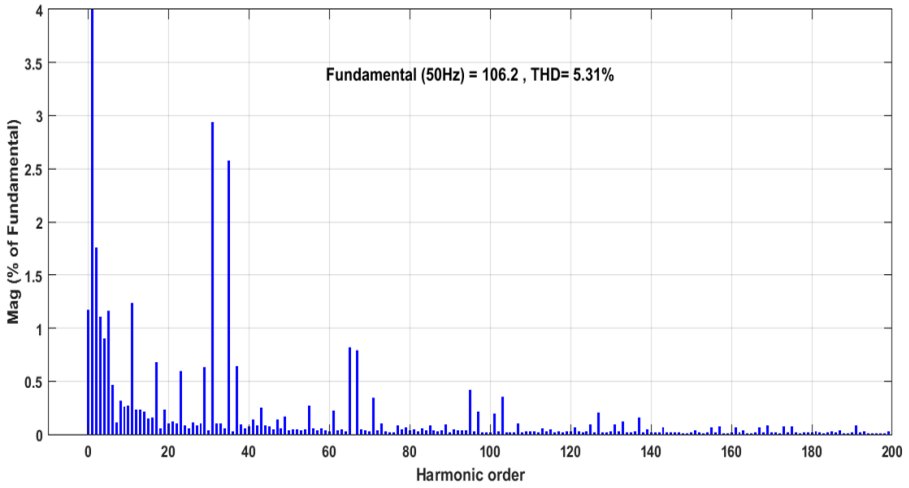

FIGURE 5.14: Output current harmonic spectrum of 2-level GTVSC

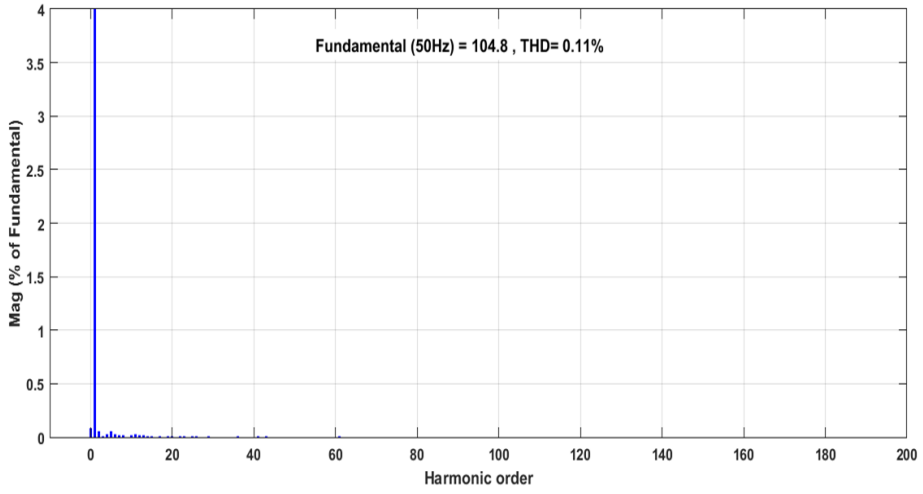

FIGURE 5.15: Output current harmonic spectrum of 21-level GTMMC

The total harmonic distortion amounts to 4.81% in the output current of two-level VSC. The total harmonic distortion amounts to 0.11% in the output phase current of 21-level MMC and it is presented by Figure 5.15. The current harmonic spectrum analysis also favors 21-level MMC and proves its superiority with respect to output current waveform of two level VSC.

5.4.6 Comparison of Total Harmonic Distortion

This section analyses the trend of total harmonic distortion when the voltage levels are increased at the converter output voltage. Figure 5.16 shows the graph in which two level VSC and multilevel MMC(for different voltage levels) are analyzed on the basis of THD present in converter output voltage waveform .

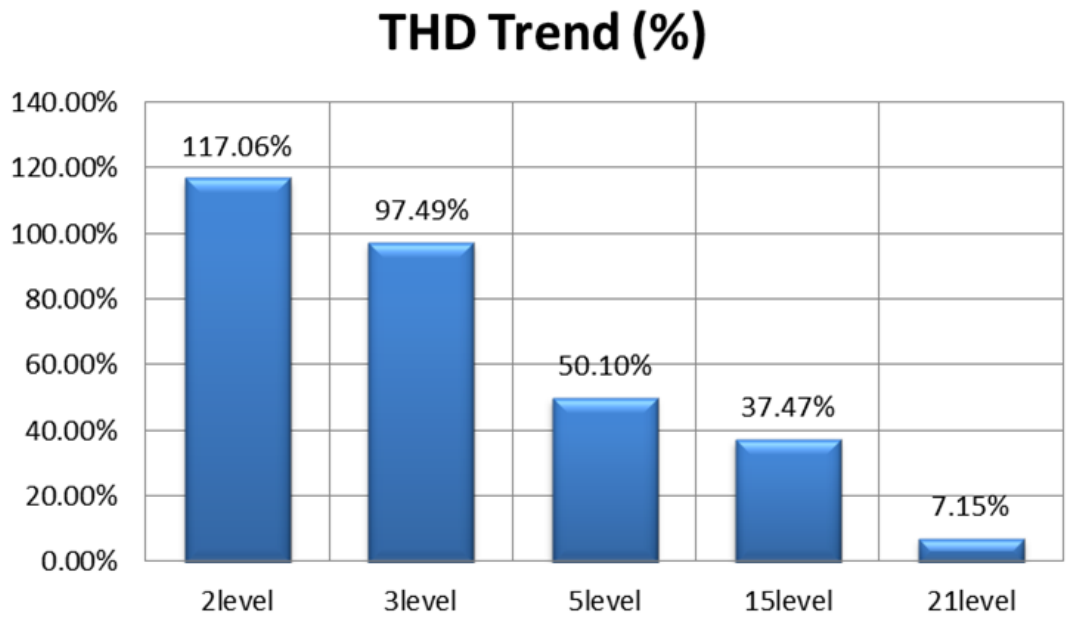

FIGURE 5.16: THD trend for different levels of converter output voltage.

This comparison is made by using open loop control where the switching signals are generated by using PWM generator block from Simscape Simpower library of Simulink. The trend of THD in this graph shows that 2-level VSC offers the highest level of total harmonic distortion ≈117%. The three-level MMC offers the THD of ≈ 97.50%.

The 5-level MMC offers ≈ 50%, 15-level MMC offers ≈ 37.50% and finally 21-level MMC was found to offer ≈ 7.15% of THD in their respective output voltage waveforms.

The THD for two-level VSC and 21-level MMC is even more reduced to 102% and 5.65% respectively, when measured with the closed loop control tuned with optimal gains using Modulus Optimum tuning criteria.

5.4.7 Comparison of Cost and Switching Losses

To withstand 100kV DC link voltage, 2-level converter requires 20 series connected IGBTs to make a converter arm valve while keeping a margin of 23% as safety margin to avoid the risk of over voltages. Therefore a net total of required IGBTs for two-level three phase VSC are $6 \times 20 = 120$.

Keeping the same safety margin for 21-level MMC, 20 half bridge submodules were used to equally share 5kV voltage from full DC link voltage of 100kV. As each half bridge submodule carries two IGBTs therefore the total IGBTs used in the design of three phase 21-level MMC were double to that of two-level VSC i.e.$6 \times 2 \times 20 = 240$.

As the number of IGBTs in MMC is increased up to double the number of IGBTs in two level VSC, conventionally it must offer more switching losses but this does not happen actually. MMC allows the switching of IGBTs at very low switching frequency almost at 3× fundamental frequency rendering very low values of total harmonic distortion in output voltage which in turn renders lower switching losses.

The switching losses corresponding to various switching frequencies are analyzed for both converter topologies by analyzing the effect of variation of switching frequency on the output voltage quality i.e. total harmonic distortion in the converter output voltage. The value of frequency modulation index is varied at 20, 15, 10, 8, 5 and 3 corresponding to each value the THD value in the output voltage waveform of two level GTVSC and 21-level GTMMC is plotted in Figure 5.17 and Figure 5.18 respectively.

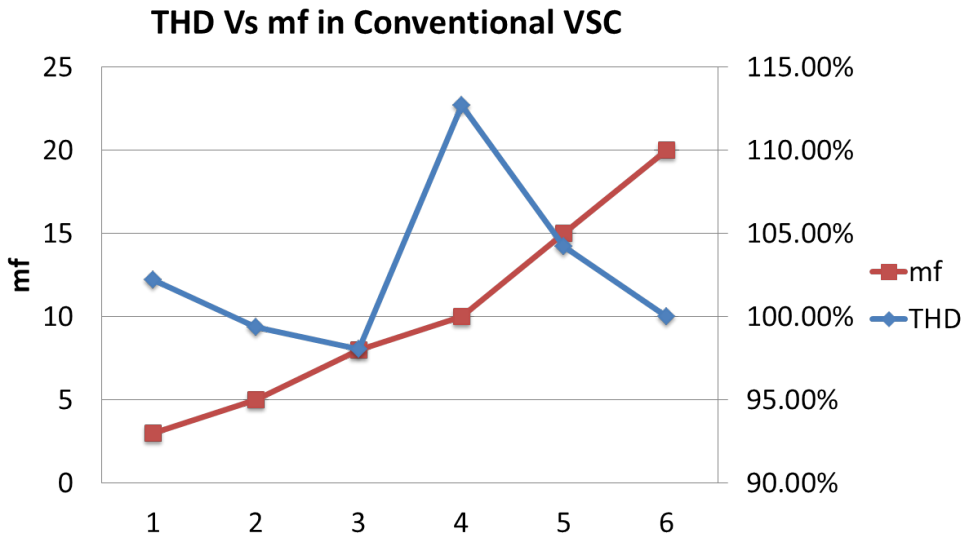

FIGURE 5.17: Effect of variations in mf on THD of 2-level GTVSC output voltage.

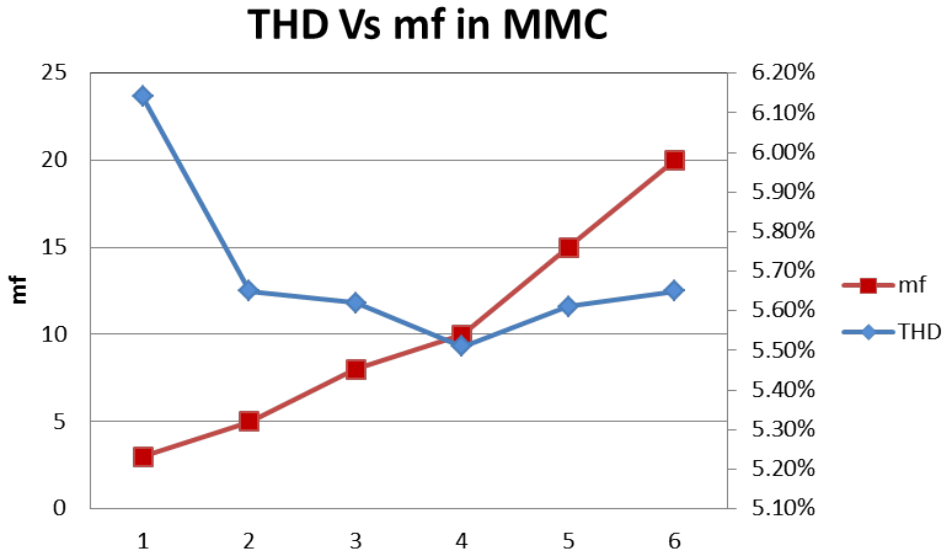

FIGURE 5.18: Effect of variations in mf on THD of 21-level GTMMC output voltage.

The quality of 2-level output voltage waveform is greatly affected by the corresponding variations of switching frequency i.e. while decreasing f_{sw} from 1kHz to 750Hz the THD increases from 100% to 104%, by further decreasing f_{sw} from 750Hz to 500Hz the THD increases from 104% to 112%. However by decreasing f_{sw} further to down to 400 decreases THD to 98%. After this point by further

decreasing f_{sw} to 5×50 and 3×50 increases THD to 99% and 104% respectively as shown in Figure 5.17.

Interestingly, when the same plot is developed for similar values of m_f for 21-level GTMMC it was found that decreasing m_f from 20 to 3 or in other words decreasing switching frequency f_{sw} from 1kHz to 150Hz could only increase the THD up to $\approx$ 0.50% which is very insignificant amount and does not effect the overall converter output voltage quality which can be seen in Figure 5.18

The analysis of both graphs shows that 2-level GTVSC is subjected to more switching losses as compared to 21-level MMC which can produce high quality output voltages with even reduced switching frequencies which in turn corresponds to reduced switching losses and high power conversion efficiency.

Although the number of IGBTs is increased by double in 21-level MMC, but as IGBTs are low voltage rated cheaper devices therefore this renders insignificant increase in the cost of 21-level MMC as compared to 2-level VSC. However the indispensable demand for AC harmonic filter significantly increases the cost in two-level VSC.

5.4.8 Comparison of Filter Requirements

As both converter topologies are being analyzed in a grid tied environment which is always a load changing environment therefore the converter output voltage is also analyzed on the basis of total harmonic distortion at various loads to analyze the maximum filter requirements. This analysis was made at various time instants i.e. at 0.3sec when the converter was injecting 10MW power, at its full capacity, to the grid and acting as a source.

At 0.5sec, when the converter power was -10MW i.e. it was acting as a load being supplied by the grid. At 0.7sec, when the converter power was +5MW i.e. it was supplying power half of its maximum rated capacity and finally at 0.9sec when the converter power was -5MW i.e. absorbing power from grid and acting as a load of

5MW. The THD corresponding to these time instants (in steady state) for both converter topologies is presented in Figure 5.19.

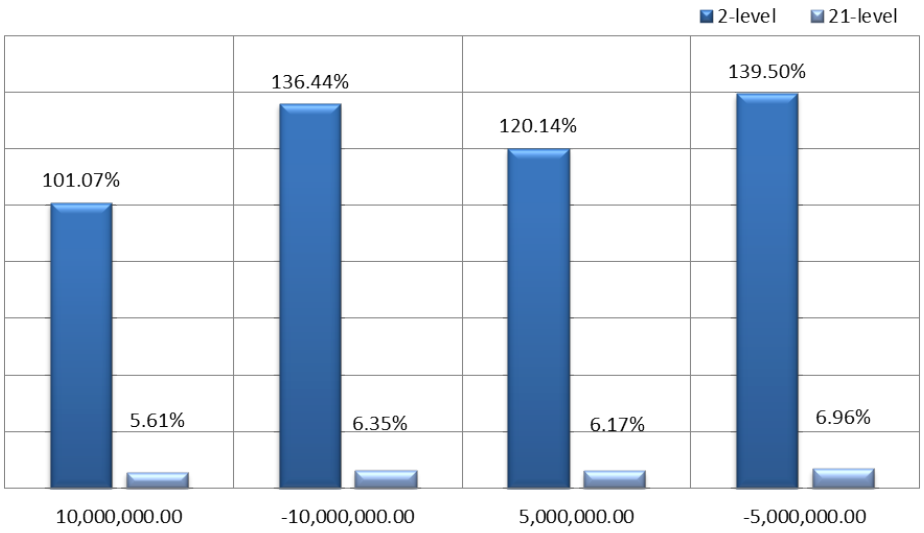

FIGURE 5.19: Effect of Load Variations on THD

In HVDC systems an AC harmonic filter is always used at the output of converter. However its size depends on the maximum susceptible harmonics whigh frequency harmonics as well as low frequency harmonics. In two level VSC as the THD values are abruptly increasing and decreasing to quite large values therefore a large size and expensive AC harmonic filter is required at the output of 2-level GTVSC.

However in 21-level GTMMC it can be viewed from Figure 5.19 that at each load change, it renders only an insignificant change in the THD of output voltage waveform. Therefore it can be proposed that the requirement of AC harmonic filters at the output is almost reduced to negligible level as compared to 2-level GTVSC.

The AC harmonic filters are most commonly passive filters which not only increase the overall cost and size of the converter station but also produce the reactive power which become another drawback for the VSC system. Because the converter is not inherently designed to absorb the reactive power therefore the use of AC harmonic filters limits the over all working performance and efficiency of the VSC system.

5.5 Case B: Comparative Analysis of Control Performance & Complexity

Under this section the control performance and complexity of 21-level GTMMC is compared with conventional standard VSC. For this purpose the transfer functions obtained in chapter 4 are used to perform frequency-domain analysis and later time-domain analysis for both converter topologies.

In the subsequent sections the Matlab/Simulink model of 21-level MMC and conventional VSC are analyzed on the basis of performance of the control loop towards various step changes in reference Active power by keeping Reactive power reference at zero value.

The converter, PCC and grid voltages, currents, active and reactive power are analyzed towards the subjected changes in active power. Towards the end of this section additional control parameters which must be considered during designing of control structure for 21-level MMC are investigated.

5.5.1 Comparison of Closed Loop Stability

The frequency domain analysis is performed to analyze stability of the converter inner current closed loop. For this, the open loop transfer functions of the current control loop of 2-level GTVSC and 21-level GTMMC as discussed in section 4.8.2.1 and section 4.8.2.1 respectively, are used to perform bode plots which analyze the stability of inner current closed loop for both converter topologies.

The bode plots are performed in Matlab by using $Bode()$ or simply $Margin()$ command. The analysis shows that for both converters the Gain Margin (G.M) is infinity whereas the Phase Margin (P.M) for 2-level GTVSC is 51.8 and for 21-level GTMMC, it is 51.9 which are almost equivalent.

These results show that the inner current closed loop is stable, and having sufficiently large phase margin signifies that inner current closed loop controller is robust against the over currents that arise due to voltage variations.

Figure 5.20 provides the comparison of stability analysis by using bode plots and concludes that the open loop inner current control of 2-level GTVSC and 21-level GTMMC have stability margins.

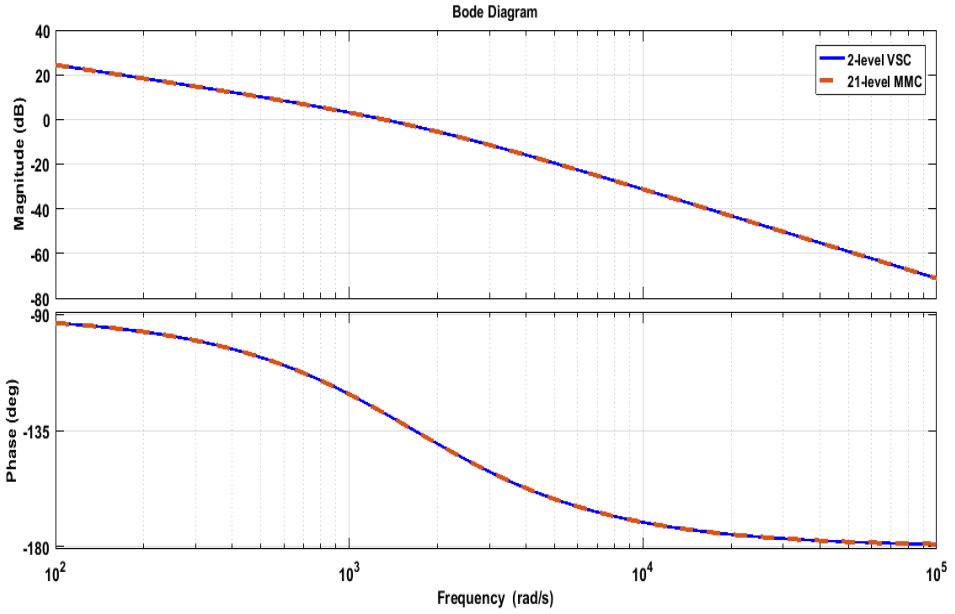

FIGURE 5.20: Frequency domain analysis of inner current control loop for 2-level GTVSC and 21-level GTMMC

Table 5.4 presents the stability margins obtained from the frequency domain analysis of open loop current control using bode plots for both of the grid connected converter topologies.

TABLE 5.4: Frequency Domain Analysis of open loop current transfer functions

Topology	Gain Margin (G.M)	Phase Margin (P.M)
2-level GTVSC	Infinity	51.8
21-level GTVSC	Infinity	51.9

5.5.2 Transient Analysis (Step Response)

The time-domain analysis is used to analyze the performance of closed loop current control when the reference signal is introduced subjected to a step change in input with respect to time. The transient and steady state response of inner current control loop are analyzed corresponding to the unit step change in the reference input by using *step*() function command in Mat lab.

Here the closed loop transfer functions of inner current control loop for both converter topologies i.e. 2-level GTVSC and 21-level GTMMC as discussed in section 4.8.2.1 and section 4.8.2.2 respectively are used to analyze the step responses which are presented in Figure 5.21.

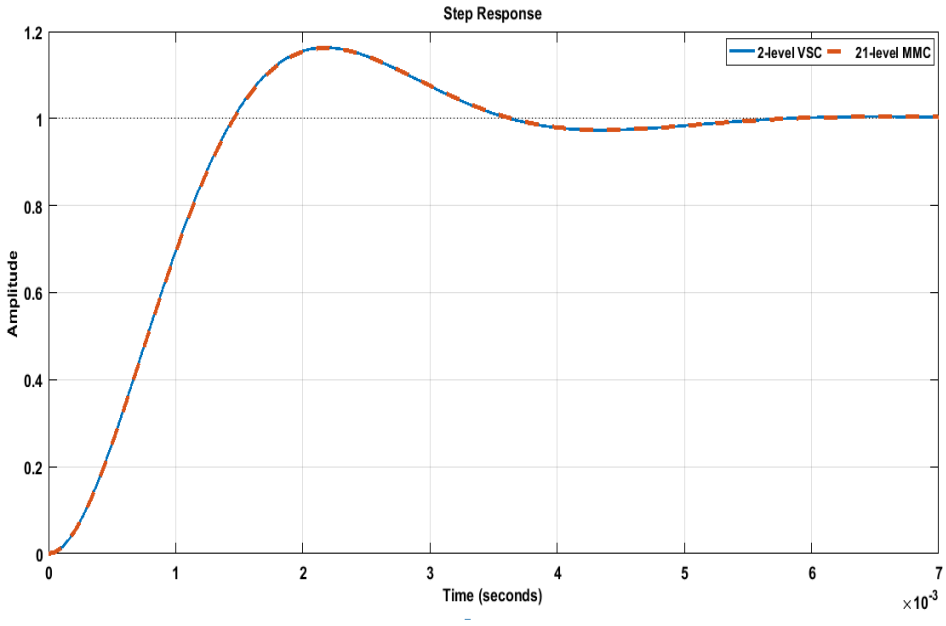

FIGURE 5.21: Step response of current controller for two-level GTVSC and 21-level GTMMC

From Figure 5.21 it is clear that both systems show the similar well damped response for current control loop tuned by Modulus optimum tuning criteria.

The peak Amplitude A_p was found to be same for both converter topologies i.e 1.6. The percent maximum overshoot (% MOS) for both systems was found with a slight difference i.e. 16.3% for conventional VSC and 16.2% for MMC for a step

input, the peak time t_p taken by VSC to reach the steady state was found to be 0.00216s where as for MMC it was 0.00221s.

The settling time (t_s) and the rise time (t_r) were same for both converter topologies i.e. 0.00485s and 0.000983s respectively. These results are summarized in Table 5.5.

TABLE 5.5: Time domain analysis of closed loop transfer functions.

System	A_p	$\%\ MOS$	t_p	t_s	t_r
2-level VSC	1.16%	16.3%	0.00216s	0.00485s	0.000983s
21-Level MMC	1.16%	16.2%	0.00221s	0.00485s	0.000983s

Table 5.5 shows that the speed of responses for current closed loop in both systems is exactly same.

Therefore it can be concluded that, 21-level GTMMC in spite of having 20 series connected floating capacitors in its each arm and additional arm inductors in each phase leg shows the same transient response as conventional GTVSC. The transient and steady state responses are found to be fast and well damped for both converter topologies.

5.5.3 Analysis of Closed Loop Control Performance in Simulink Model

In this section the Simulink model of 2-level GTVSC and 21-level GTMMC are analyzed on the basis of performance of the closed loop control. The behavior of active power controller is analyzed towards the reference active power P* step change of 10MW where as the reactive power controller is analyzed by regulating converter reactive power Q at zero during the step input changes made in active power reference P*.

5.5.3.1 Simulation Model Active Power Step Response

At time t=0 s the active and reactive power are both at zero values . The response of inner current controller is analyzed when the reference active power P* is introduced with a step change from 0 to 10MW at time t=0.2 s.

Figure 5.22 (a) represents the step response of two-level VSC active current controller whereas Figure 5.22 (b) represents the step response of 21-level MMC active current controller.

Both controllers with different converter topologies are found to perform in a similar manner towards the same input change at same time instant, which is in agreement with the analysis of step responses of the respective converter transfer functions as made in section 5.5.2.

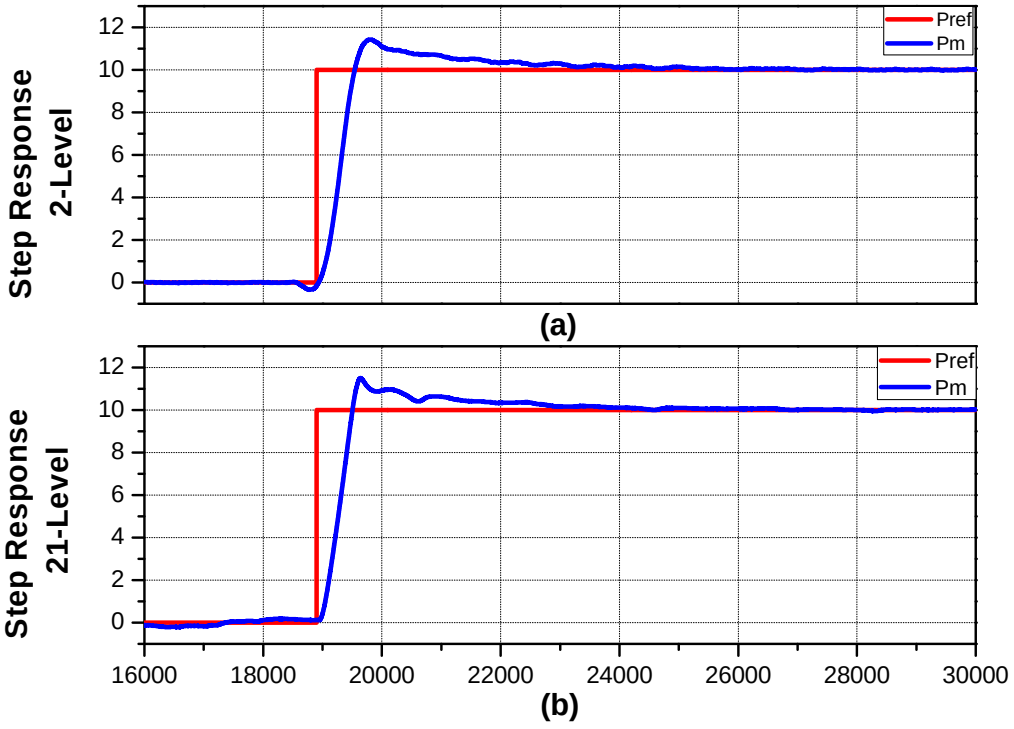

FIGURE 5.22: Step response of active power control (a)in two-level GTVSC (b) in 21-level GTMMC

5.5.3.2 Simulink Model Reactive Power Regulation

The reactive current I_q and reactive power Q of 2-level VSC and 21-level MMC are aimed to regulate at zero value reference value. In order to achieve this objective the reference reactive power Q^* command is set at zero value. The reactive current controller response is similar for both converter topologies and effectively regulates the converter reactive power Q and converter reactive current I_q back to zero after a transient was observed due the step change made in reference active power P^*.

Figure 5.23 (a) represents the reactive power regulation by reactive current controller of 2-level VSC whereas Figure 5.23 (b) represents the reactive power regulation by reactive current controller of 21-level MMC. The analysis from Figure 5.21 and Figure 5.23 represents that the control flexibility of conventional VSC is reserved in modular multilevel converter which shows the same transient and steady state response as obtained by conventional VSC.

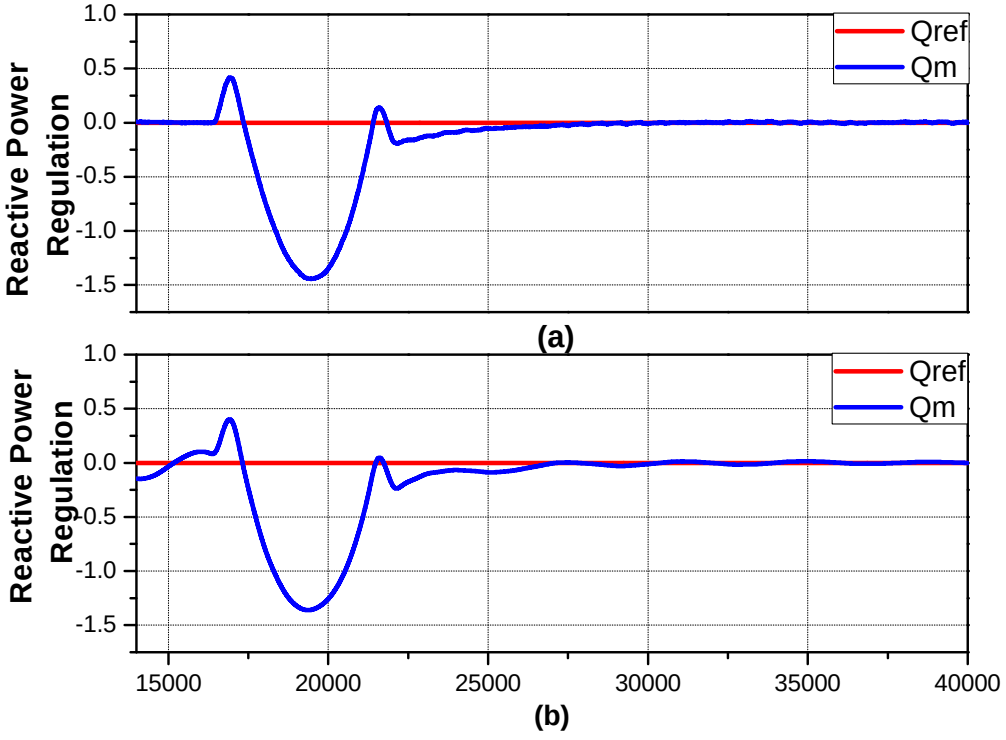

FIGURE 5.23: Regulation of reactive power (a) two-level GTVSC (b) in 21-level GTMMC

5.5.4 System Performance at Dynamic Loads

Under this section, the active power is varied at different time instants in order to analyze the flexibility of active power control towards different variations made at different time instants. The reactive power is regulated at zero through out the simulation time period. Therefore both grid connected converter topologies are subjected to these variations to investigate response of converter active/reactive current, three phase voltages and currents at PCC, grid active/reactive power and grid three phase voltages and currents. This simulation constitutes the run time from 0 to 1s.

Before proceeding further, the edges of the reference active power signals are made a little bit round by using a low pass filter with time constant τ=0.005s, so that the controller may not face any fast and abrupt changes made in reference active power which corresponds towards large overshoots in the converter instantaneous power while tracking the reference command signal. The use of low pass filter helps to evade the sharp corners of large steps in the reference signal by making the sharp corners round, due to which expected large overshoots are removed [74].

At time t=0 s, the converter active power P is set at zero initially, during this time the converter is neither acting as a source nor as a load. At time t=0.2 s, the active power reference step P^* is changed from 0 to 10MW corresponding to which the converter instantaneous power P is changed from 0 to 10MW i.e. the converter starts injecting power into PCC and acting as a source of 10MW power.

At t=0.4 s, the direction of reference active power P^* is reversed and given a step change from 10MW to -10MW, the power reversal does not endanger the converter stability and hence converter tracks the reference power with same efficiency. In this mode, it acts like a load which consumes 10MW power through PCC from grid. Further at time t=0.6 s, the reference active power command P^* is again introduced with a step change, but this time with a lower step change of +5MW to analyze the flexibility of controller at lower power variations. The converter

efficiently tracks the step reference command and now it acts like a source of 5MW.

Finally at t=0.8 s, the converter again experiences a step change of -5MW in its active power reference command P* and the controller achieves it by forcing the converter to act as a load of 5MW. During all these variations the converter reactive power Q is set to be regulated at zero VAR. As soon as the converter instantaneous reactive power Q experiences any transient during active power reversal, the reactive power controller brings it back to track its reference reactive power Q* of 0VAR and this is achieved efficiently by the reactive power controller.

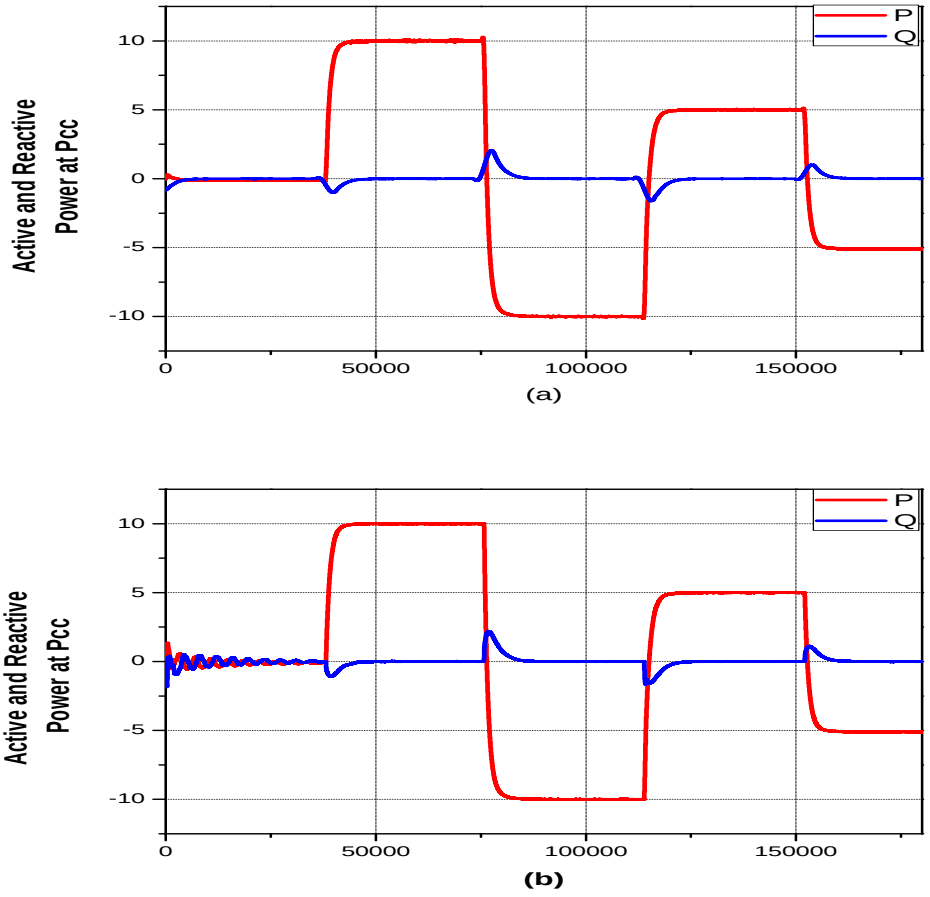

FIGURE 5.24: Active & reactive power control at different loads for(a) 2-level VSC (b) 21-level VSC

Figure 5.24 (a) shows the response of 2-level VSC whereas Figure 5.24 (b) represents the response of 21-level MMC towards the reference power step variations

while keeping the reactive power for both converter topologies equal to zero VAR. It can be analyzed from the comparison of both figures that both converter topologies perform with the same control efficiency. Therefore it is concluded that the inner current control efficiency in 21-level MMC is maintained as it was offered by standard conventional VSC.

5.5.4.1 Active/Reactive Current Control Loop Response

Corresponding to the variations subjected to the active power references for 2-level VSC and 21-level MMC, the active current I_d behaves in a similar manner as that of the active power P because of the fact that $P_{ref} = \frac{2}{3V_{sd}} i_{dref}$.

However when the reactive current experiences small transients during each active current polarity reversal, the reactive current controller efficiently regulates back the converter reactive current I_q at zero reference level that in turn corresponds towards the regulation of reactive power at 0VAR.

The phenomenon is presented in Figure 5.25 (a) and Figure 5.25 (b) where the reference command tracking of active and reactive current can be viewed for 2-level GTVSC and 21-level GTMMC respectively. Both converter topologies are observed to have the same control response towards every single variation in input reference step command.

However, the direction of d-axis and q-axis current waveforms (I_d and I_q) in 21-level GTMMC is observed to be opposite as that of the direction of d-axis and q-axis current in 2-level GTVSC. It mainly happened due to the difference in mathematical models used to realize the corresponding Simulation models in Simulink software.

In [55], the mathematical model shows additional negative sign with the transfer function of grid connected MMC and it must be the reason behind the opposite direction of dq-current in MMC with respect to the dq-current in conventional VSC.

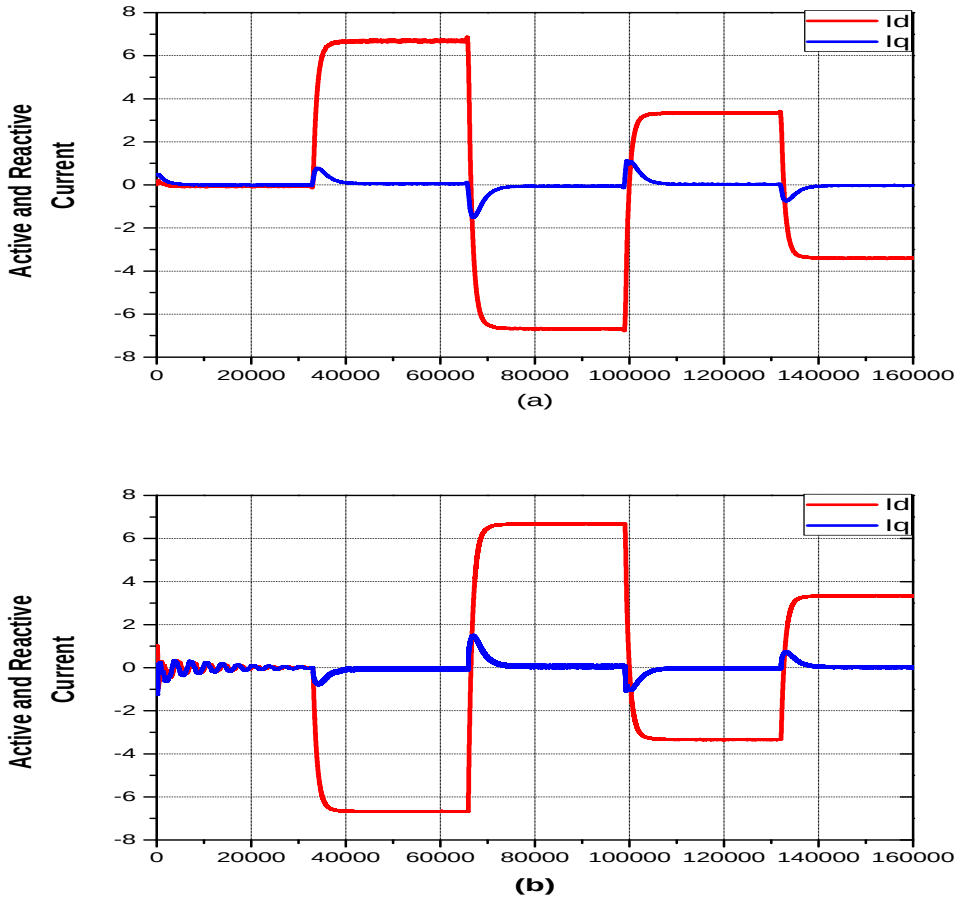

FIGURE 5.25: Converter active & reactive current at different loads (a) 2-level VSC (b) 21-level VSC

5.5.4.2 Voltage and Current at PCC

The three phase voltages and currents at point of common coupling are analyzed during the active power variation made at different time instants in the section 5.5.4.1.

The three phase voltages (V_{abc}) at point of common coupling are remained unaffected by the reference active power P^* variations however the current direction reverses corresponding to each variation (polarity as well as magnitude) made in reference active power.

The change in active power magnitude also changes magnitude of three phase currents (I_{abc}) at PCC . For large values of power the PCC currents are large

whereas for smaller magnitudes of power, the converter currents at PCC are found to be reduced at lower magnitudes.

Thus, it is concluded that the direction of flow of active power is controlled by controlling the converter current polarity. Whereas the magnitude of converter active power is controlled directly by magnitude of converter current. However the magnitude and direction of three phase voltages at PCC remain unaffected by active power variations.

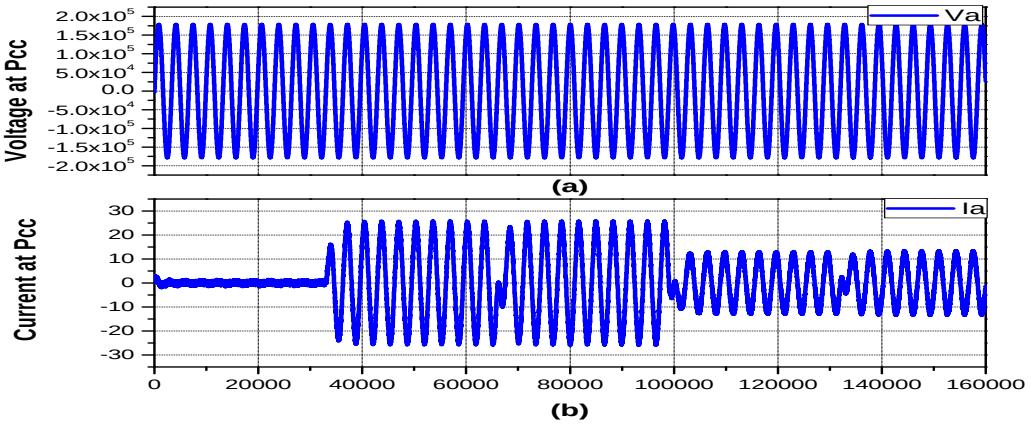

FIGURE 5.26: Phase Voltage at PCC 2-level GTVSC (b) Phase current at PCC in 2-level GTVSC

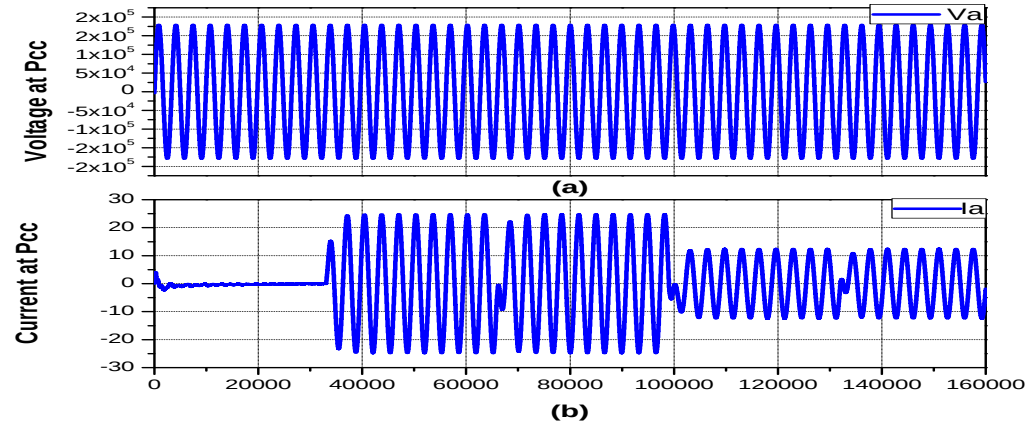

FIGURE 5.27: (a) Phase Voltage at PCC in 21-level GTMMC (b) Phase current at PCC in 21-level GTMMC

Figure 5.26 (a) shows the phase voltage of 2-level VSC at PCC while Figure 5.26 (b) shows the phase current of 2-level VSC at PCC. Figure 5.27 (a) and Figure

5.27 (b) shows the corresponding phase voltage and phase current for 21-level VSC at PCC respectively.

5.5.4.3 Grid Instantaneous Active and Reactive Power

It is interesting to note that during each step change made in reference active power P^* to control the converter instantaneous active power P at PCC, the grid instantaneous power P_g also changes accordingly during simulation of both converter models.

At time t=0 s, when the active power P is zero the grid instantaneous active power P_g = 150MW i.e. in standalone mode of operation the 150MW instantaneous power is circulating in the grid side electrical circuit.

When at time t=0.2 s, the converter reference active power is given a step change of +10MW, the grid instantaneous active power P_g is reduced by 10MW and settles down at 140MW. This can be interpreted as the 10MW power which was previously coming from grid, it is now provided by converter therefore the grid power decreases by 10MW.

At t=0.4 s, the grid power experiences a step change from 140MW to 160MW which $\Rightarrow$ the grid is providing extra 10MW power to feed converter which acting like a load now.

Similarly at time instants t=0.6 s, and t=0.8 s, the grid power changes from 160 MW to 145MW and from 145MW to 155MW corresponding to the reference active power variations of -5MW and +5MW, where converter first acts as a source of 5MW and than load of 5MW respectively.

The grid reactive power Q_g is found 310 MVAR during standalone mode however it is regulated to round about its nominal value when it experiences any transients, when the converter active power is subjected to any step change.

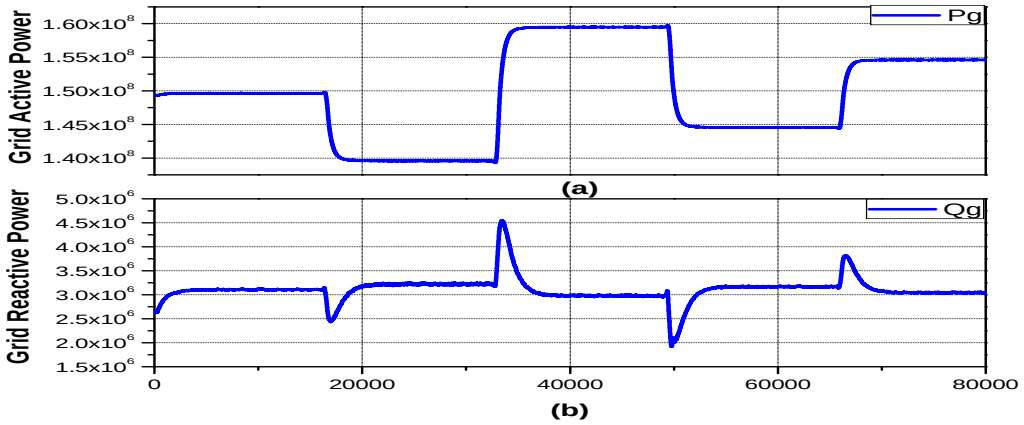

FIGURE 5.28: (a) Grid instantaneous active power variation in 2-level GTVSC (b) Grid Instantaneous reactive power regulation in 2-level GTVSC

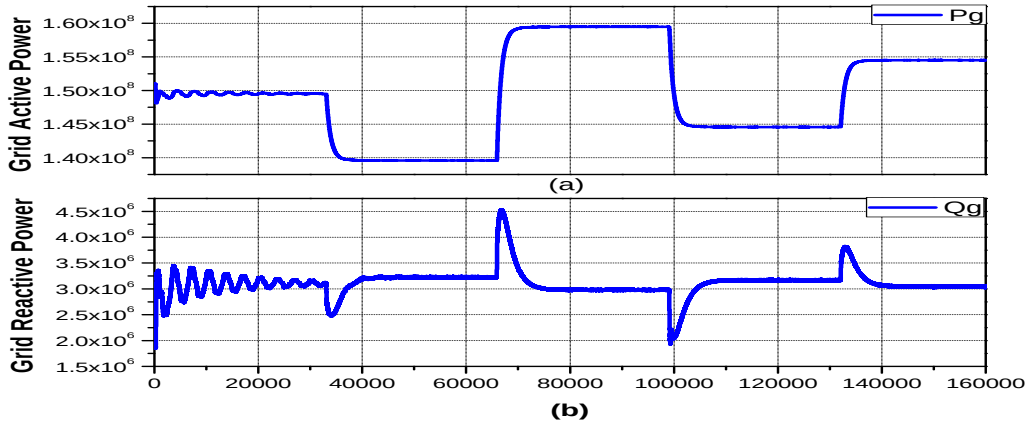

FIGURE 5.29: (a) Grid instantaneous active power variation in 21-level GTMMC (b) Grid instantaneous reactive power regulation in 21-level GTMMC

Figure 5.28 (a) and Figure 5.28 (b) represents the grid active and reactive power respectively where it can be seen that the variations in the active power of converter brings the variations in the grid instantaneous active power. This in turn causes transients in grid reactive power. The figure 5.28 relates the variations of grid active and reactive power corresponding to the variations made in active power at PCC by 2-level GTVSC.

Whereas Figure 5.29 (a) and Figure 5.29 (b) represents the grid active and reactive power variations respectively, corresponding to the variations made in active power at PCC in 21-level GTMMC.

5.5.4.4 Grid Voltage and Current

This section analyzes the impact of active power variations on the grid side voltages and currents. Figure 5.30 (a) and Figure 5.31 (a) represents the grid phase voltage for 2-level GTVSC and 21-level GTMMC respectively. It is analyzed that the active power reversal at PCC does not show any impact on grid voltages.

However in Figure 5.30 (b) and Figure 5.31 (b) it is observed that the amplitude of grid phase current varies with the variations in the magnitude of active power at PCC for both converter topologies i.e. 2-level GTVSC and 21-level GTMMC respectively. However the grid current polarities are not changed during converter power reversal at any time instant during the whole simulation period.

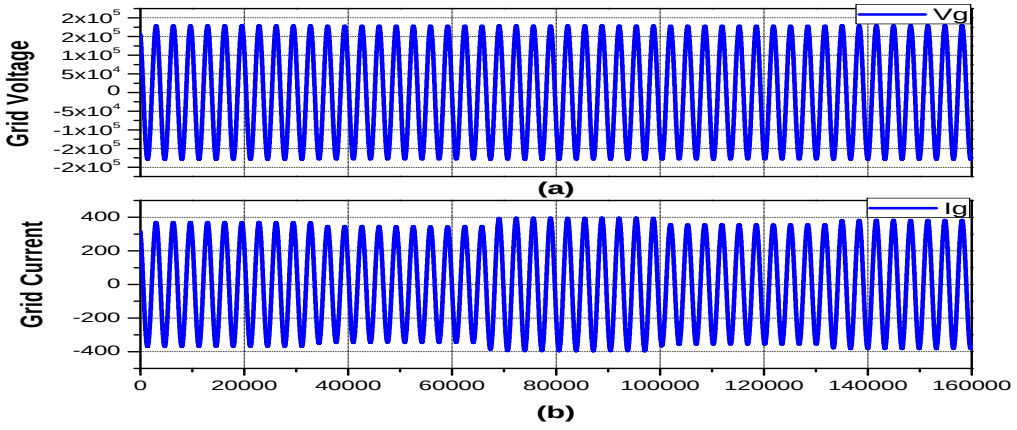

FIGURE 5.30: 2-level GTVSC (a)Grid voltage (b) Grid current

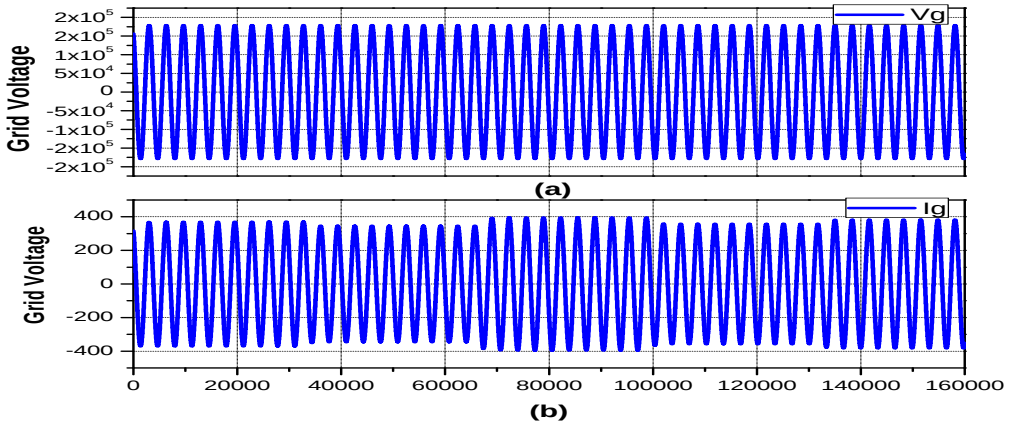

FIGURE 5.31: 21-level GTVSC (a)Grid voltage (b) Grid current

The amplitude of grid current decreases when grid power deceases in correspondence to increase in amplitude of active power. Similarly the amplitude of grid current increases when the grid power increases in correspondence to decrease in the active power at PCC.

More precisely when converter acts as a source, load draws some of the current from converter and other from grid however when converter acts as a load more current is drawn from grid i.e. to feed the converter as well as each load at its rated power.

This section analyzed the performance of 21-level GTMMC with respect to the performance of conventional VSC at PCC, on the basis of performance towards control of converter instantaneous active power when certain variations are made in reference active power.

The regulation of converter reactive power is also analyzed when the active power reversal introduces transients in reactive power of the converter. This analysis concludes that 21-level GTMMC and 2-level GTVSC are found to posses same control flexibility and performance.

However 21-level GTMMC in standalone mode of operation shows ripple which is offered by the floating capacitors joined in series connection in 21-level MMC arm. This ripple can be mitigated by using appropriate capacitor voltage balancing algorithms which adds complexity to MMC control.

5.5.5 Control Complexity Analysis

The modular multilevel converter has some constraints which offer hindrance in the design of proper control strategy. Among them the proper selection of modulation index is an important aspect.

Another element which was found greatly affecting the output performance of MMC is switching frequency. Both aspects are discussed in the following sections and elaborated with the simulation results produced during results formulations.

5.5.5.1 Modulation Index

The number of levels in the output voltage of modular multilevel converter are found to be directly related to the value of modulation index ($\hat{m}$). Lower values of modulation index abstain the appearance of maximum achievable number of voltage levels in the output of multilevel converter which in response increases the total harmonic distortion (THD %) in converter output voltage waveform.

Alongside poor voltage quality, the lower values of modulation index hinders to achieve the rated voltages which introduces greater ripple content in capacitor voltages and output power. In this way lower values of modulation index deteriorate not only the output voltage quality but also the whole system performance.

Therefore it is strongly suggested to use higher values of modulation index i.e. $\hat{m} \gtrapprox 0.8$ in modular multilevel converters to achieve efficient and high quality power conversion as well as power transmission in an HVDC system. In comparison, the output of Two-level VSC is not affected by lower values of modulation index $\hat{m}$.

The analysis was performed using 21-level GTMMC for different values of modulation index ($\hat{m}$)=$\{0.5,0.6,0.7,0.85\}$ corresponding to which output voltage of 21-level GTMMC was analyzed on the basis of converter peak output phase voltage (V_p), maximum achievable number of output voltage steps (N) and total harmonic distortion (THD) caused due to the reduction of voltage steps in converter output phase voltage.

The results of this analysis are presented in Table 5.6.

TABLE 5.6: Investigation of Effects of Variation of Modulation Index

$\hat{m}$	N	V_p	THD%
0.85	21	49.89kV	5.70%
0.7	19	44.71kV	6.85%
0.6	17	39.55kV	8.02%
0.5	15	34.53kV	8.96%

The pictorial view of Table 5.6 is presented in Figure 5.32 where;

Figure 5.32 (a) represents the output voltage waveform of 21-level GTMMC while keeping $\hat{m} = 0.85$, twenty one voltage steps are appeared at output voltage waveform with $V_p \approx 50$kV and THD = 5.70%.

Figure 5.32 (b) represents the output voltage waveform of 21-level GTMMC while keeping $\hat{m} = 0.7$, nineteen voltage steps are appeared at output voltage waveform with $V_p \approx 45$kV and THD = 6.850%.

Figure 5.32 (c) represents the output voltage waveform of 21-level GTMMC while keeping $\hat{m} = 0.6$, seventeen voltage steps are appeared at output voltage waveform with $V_p \approx 40$kV and THD = 8.02%.

Figure 5.32 (b) represents the output voltage waveform of 21-level GTMMC while keeping $\hat{m} = 0.5$, fifteen voltage steps are appeared at output voltage waveform with $V_p \approx 34$kV and THD $\approx$ 9%.

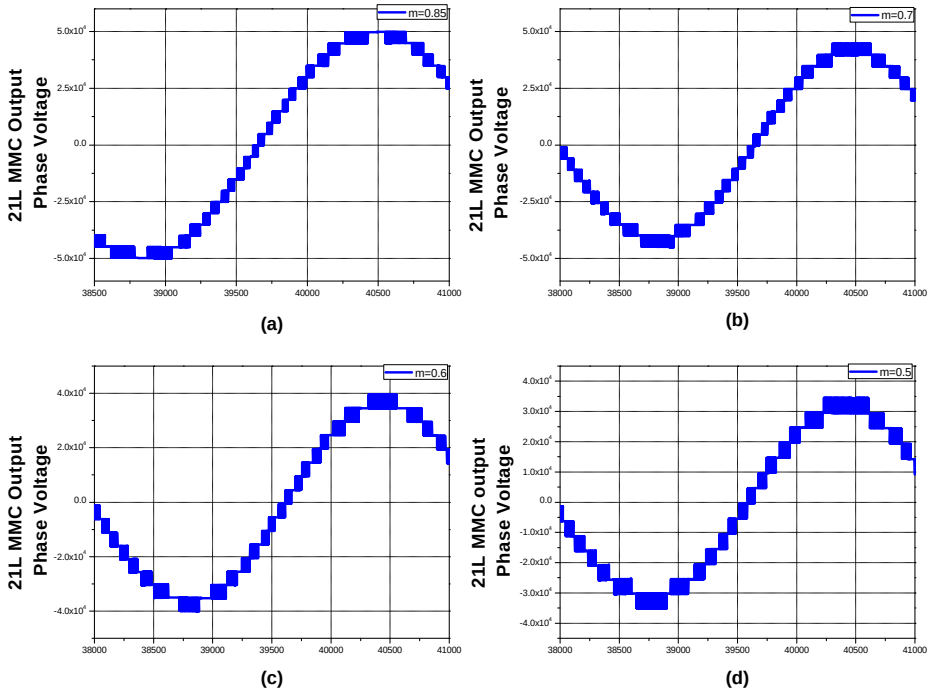

FIGURE 5.32: Effect of modulation Index on output voltage levels of 21-level MMC (a) $\hat{m} = 0.85$ (b) $\hat{m} = 0.7$ (c) $\hat{m} = 0.6$ (d) $\hat{m} = 0.5$

5.5.5.2 Switching Frequency

Switching frequency is another major element which affects the converter output voltage, as high switching frequencies help to produce voltage waveforms with low harmonic distortion or it can produce more sinusoidal output voltage waveform thus ensuring high quality power conversion and also reduces the need for filtration. Another important benefit of higher switching frequencies is realized during the analysis of case study, according to which, at higher switching frequencies the voltage across each capacitor in the series connected submodules of MMC is balanced in steady state.

As higher switching frequencies correspond to higher switching losses therefore an optimal frequency can be chosen which helps to maintain voltage balance across capacitors of each submodule per MMC arm. Figure 5.33 represents the pictorial view for behavior of twenty capacitors voltages in the upper arm phase of leg A of 21-level MMC when operated at different frequencies.

The Figure 5.33 shows that by decreasing the switching frequencies, capacitor voltages start deviating from their desired voltage values and results into the lower quality and less efficient power conversion. At switching frequency 30 times greater than fundamental frequency, the capacitor voltages are well balanced and stick to their defined voltage levels as shown in Figure 5.33 (a).

When the frequency modulation index (m_f) is reduced up to 20, the capacitor voltages do not deviate from their mean values as shown in Figure 5.33 (b), even at m_f=10, capacitor voltages are well balanced and stay with in the limit of 5kV $\pm$300v in steady state which can be seen in Figure 5.33 (c).

However when the frequency modulation index is reduced to 5 and further , the need for capacitor voltages balancing algorithm becomes indispensable because capacitor voltages start deviating from their mean values as shown in Figure 5.33 (d). The use of optimal switching frequency can provide a way out for lower switching frequency corresponding towards comparatively lower switching losses without the need for complex capacitor voltage balancing algorithms.

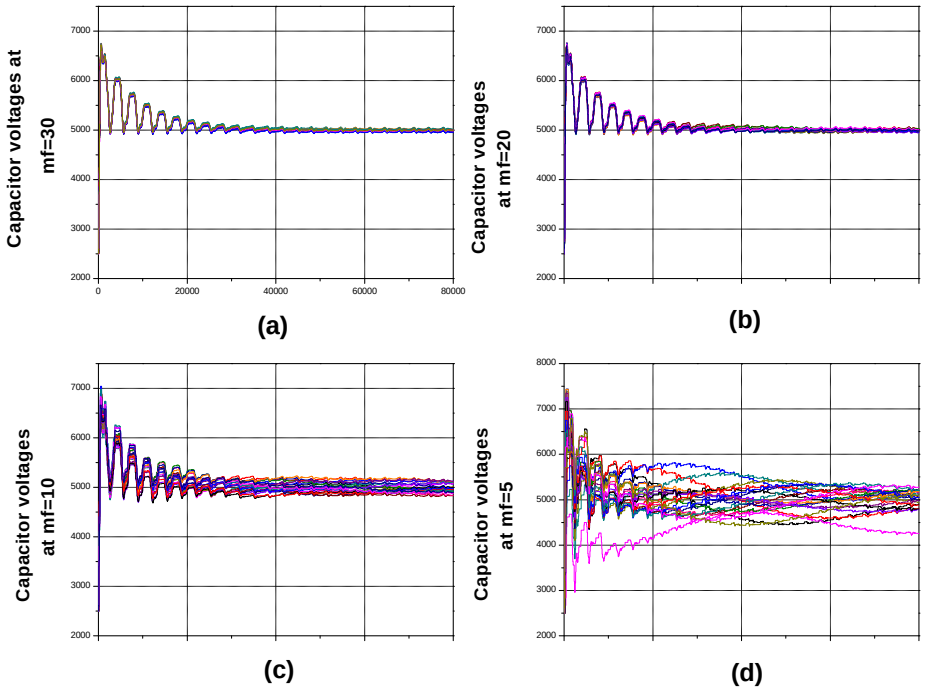

FIGURE 5.33: Effect of m_f on capacitor voltage balancing in 21-level MMC (a) m_f=30 (b) m_f=20 (c) m_f=10 (d) m_f=5

The analysis made from Figure 5.33 can be concluded that there is always a conflicting situation between lower switching frequencies ⇒ (lower switching losses) and natural balancing of capacitors′ voltage. Therefore to reduce switching losses, MMC can support reduced switching frequencies up to 3 times fundamental frequency without the demand of bulky and expensive filters required for producing high quality output voltage but at the cost of increased control complexity in the shape of demand for capacitor voltages balancing algorithms.

5.6 Chapter Summary

This chapter defines a case in which 2-level VSC and 21-level MMC are tested to make the comparative analysis on the basis of converter output voltage quality and performance with feedback control loop. Case A provides the comparative analysis

of conventional VSC and 21-level MMC on the basis of output voltage quality. Case B discusses the control system performance of both grid connected converter topologies. Different results are produced which prove the MMC superiority over conventional VSC and favors its use in high power high voltage applications. The last section of this chapter provides other control parameters which can badly affect the output of MMC if not considered properly.

TABLE 5.7: Summary of comparative analysis of two-level GTVSC and 21-level GTMMC.

Serial No.	Specification	2-L Grid tied VSC	21-L Grid tied MMC
1.	Converter Design Complexity	Converter Design requires series chains of IGBTs constituting high design complexity in HVDC	Converter design is modular and simpler therefore it offers lower design complexity in HVDC
2.	Shape of Output Voltage	Crude AC waveform with two voltage steps	Sinusoidal AC waveform with 21 voltage steps
3.	Voltage Harmonic Spectrum	The first harmonic at 33±1 with highest magnitude of 61.98% of fundamental component	The first harmonic at 660±1 with highest magnitude of 1.27% of fundamental component
4.	Dominant harmonics in Converter output voltage	h_3, h_5, h_9, h_{11}, h_{15}, h_{17}, h_{19}, h_{21} and h_{23}	h_{633}, h_{641}, h_{679}, h_{689}, h_{691} and h_{631}
5.	THD (%) in Output Voltage	102.66%	5.65%
6.	Converter Output Current Shape	AC waveform with high ripple content	Smooth sinusoidal AC waveform
7.	THD (%) in Output Current	5.31%	0.11%
8.	Converter switching losses	It requires high switching frequency thus renders high switching losses.	It allows operation at 3× fundamental frequency thus renders lower switching losses.
9.	AC harmonic filter requirements	Indispensable	Almost negligible
10.	Cost	high converter costs including bulky and expensive filters	Over all cost of the converter is greatly reduced with negligible filter requirements
11.	Control Performance	Same	Same
12.	Control Complexity	Low	High

Chapter 6

Conclusion and Future Work

This work aimed at the comprehensive study of modular multilevel converter to analyze its performance and suitability regarding its use in HVDC. Therefore in order to achieve this goal MMC is compared with conventional VSC in a grid tied system where the converter output power is controlled by using classical vector control technique. At first, the deep insight of the limitations of all the previously developed and commercialized VSC topologies in HVDC is provided, later the mathematical model for the AC side dynamics of conventional VSC and MMC are explained in view of literature, having come to the point that MMC and VSC both posses the same AC side dynamics.

Based on the mathematical model, the converter control is designed which involves the dqo transformation of system variables, grid synchronization, design of inner current closed loop control and open loop control of Active power (DPC) while reactive power is regulated at zero VAR. As per author's knowledge, the novelty of this work is to provide the detailed and comprehensive analysis of MMC by comparing it to conventional VSC (a topology which has been widely used in HVDC projects since 1997) on the basis of mathematical modeling, converter control performance and complexity, output voltage quality, converter losses, costs and filter requirements. This work encloses all the aspects for which modular multilevel converter should be considered as a promising candidate, among other VSC topologies, to be utilized in HVDC systems.

6.1 Conclusion

After analyzing the results obtained through the simulation model of both grid tied 2-level VSC and 21-level MMC, this entire work is concluded in the subsequent paragraphs as follows;

While using MMC in high voltage high power applications the need for troublesome series connection of IGBTs to make converter arm valves is eliminated which in turn abolishes converter complexity, additional circuit losses and costs. Therefore the modularity of MMC assists the series connection of submodules (even more than 200) to any number to make converter arms, in order to achieve high quality output voltage waveforms. Thus converter design structure is simple and scalable without requiring any auxiliary equipment. The 21-level MMC produces twenty one level output voltage waveform which is almost sinusoidal and this sinus behavior is achieved by easily stacking twenty submodules in series to make single converter arm.

The converter output voltage quality is increased by swifting the converter topology from 2-level VSC to 21-level MMC by using same switching frequency. The total harmonic content which was 75% in two-level VSC, reduced up to almost negligible amount of 5.65% in 21-level modular multilevel converter, thus greatly reducing the demand for bulky and expensive filters.

In 21-level MMC each switch cell is switched independently of the other, thus the requirement of simultaneous switching is eliminated which in turn eradicates the need for sophisticated gate drives to provide dynamic and static voltage balancing as was the case with conventional VSC.

The switching frequency of 21-level MMC can be reduced to 3×50Hz thus reducing switching losses almost $<1\%$ which was 1.7% with conventional VSC. The value of total harmonic distortion in 21-level MMC output voltage and current waveforms is reduced to 5.65% and 0.09% respectively which tends to reduce the requirement of AC harmonic filters which in turn makes 21-level MMC a cost effective and compact solution to be used in HVDC.

However by reducing switching frequency 3×50Hz, the amount of THD found in 21-level MMC output voltage waveform is 6.14% whereas with switching frequency 33×50Hz the amount of THD in 21-level MMC output voltage waveform is 5.65% therefore the significant reduction of switching frequency brings an insignificant increase in the THD values. Therefore it is proposed that 21-level GTMMC does not require AC harmonic filters even at lower switching frequencies of 3×fundamental frequency.

The risk of high dv/dt is eradicated by using low frequency pulse width modulation to switch each IGBT at low voltage value of 5kV which in turn reduces the hazard of electromagnetic interference (EMI) both conducted (9kHz to 30kHz) as well as radiated (30kHz to 150kHz). In contrast, there is huge risk of EMI (both conducted and radiated) in conventional VSC because of inherently present high values of dv/dt over which use of high switching frequencies act as icing on the cake and causes worst case scenario in conventional VSC. The 21-level GTMMC allows the use of lower switching frequencies and lower dv/dt thus there is no danger of EMI in 21-level MMC.

Based on the mathematical modeling of GTMMC and conventional GTVSC the the AC side dynamics of both converter topologies are analyzed to be same therefore same control strategy adopted to control the converter output power. The control system analysis shows that 21-level MMC performs with the same control flexibility as that of conventional VSC. However MMC requires additional parameters to be considered while designing the control structure for MMC. This work presented that the higher values of modulation index are crucial to produce required number of voltage steps in converter output voltage waveform. Besides if the converter is switched at lower switching frequencies to achieve lower switching losses than each floating cell capacitor voltage starts deviating from its mean value. Therefore 21-level MMC requires capacitor voltage balancing at switching frequencies $\leq$ 5×fundamental frequency.

Hence it is concluded in general that N+1-level MMC proves itself a promising candidate to be practiced in high voltage high power applications where the switching

losses, costs, power quality, scalability to higher voltage steps with higher power conversion efficiency and size of the converter are main concerns. Therefore it is concluded that, MMC provides a feasible solution which takes away all the fore mentioned hindrances but at the cost of comparatively more complex control structure which requires capacitor voltage balancing in each switching submodule.s

6.2 Future Work

The work performed in this thesis provides a base for number of future works. However to extend the use of MMC (after analyzing its highly flexible, low loss and economical design structure) in two terminal and multi terminal VSC based HVDC systems and to explore the control techniques which are robust as well as provide better dynamic responses to control the converter active and reactive power independently, are in best of the future interests.

Bibliography

[1] A. Grid, "Hvdc for beginners and beyond," 2010.

[2] A. Siemens, "High voltage direct current transmission-proven technology for power exchange," *Tech. Rep.*, 2011.

[3] C. Barker, "Hvdc for beginners and beyond," 2009.

[4] D. A. Woodford, "Hvdc transmission," *Manitoba HVDC Research Centre*, pp. 400–1619, 1998.

[5] S. Cole and R. Belmans, "Transmission of bulk power," *IEEE Industrial Electronics Magazine*, vol. 3, no. 3, 2009.

[6] K. Meah and S. Ula, "Comparative evaluation of hvdc and hvac transmission systems," in *Power Engineering Society General Meeting, 2007. IEEE.* IEEE, 2007, pp. 1–5.

[7] B. W. N. Z. Sixing Du, Apparao Dekka, *Modular Multilevel Converters: Analysis, Control, and Applications.* IEEE Press Series on Power Engineering, Jan,2018.

[8] O. E. Oni, I. E. Davidson, and K. N. Mbangula, "A review of lcc-hvdc and vsc-hvdc technologies and applications," in *Environment and Electrical Engineering (EEEIC), 2016 IEEE 16th International Conference on.* IEEE, 2016, pp. 1–7.

[9] M. P. Bahrman and B. K. Johnson, "The abcs of hvdc transmission technologies," *IEEE power and energy magazine*, vol. 5, no. 2, pp. 32–44, 2007.

[10] F. Martinez-Rodrigo, D. Ramirez, A. Rey-Boue, S. de Pablo, and L. Herrero-de Lucas, "Modular multilevel converters: Control and applications," *Energies*, vol. 10, no. 11, p. 1709, 2017.

[11] A. Dekka, B. Wu, R. L. Fuentes, M. Perez, and N. R. Zargari, "Evolution of topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 4, pp. 1631–1656, 2017.

[12] D. M. Larruskain, I. Zamora, O. Abarrategui, and A. Iturregi, "Vsc-hvdc configurations for converting ac distribution lines into dc lines," *International Journal of Electrical Power & Energy Systems*, vol. 54, pp. 589–597, 2014.

[13] B. Andersen, "Vsc transmission tutorial," in *Proc. CIGRE Study Committee B4 Meeting*, 2005.

[14] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, "Vsc-based hvdc power transmission systems: An overview," *IEEE Transactions on power electronics*, vol. 24, no. 3, pp. 592–602, 2009.

[15] E. M.-G. Olimpo Anaya-Lara, David Campos-Gaona and G. Adam., "Appendix a: Voltage source converter topologies," 2014.

[16] C. C. Bonilla and S. M. Tigga, "Design and performance comparison of two-level and multilevel converters for hvdc applications," 2011.

[17] T. M. Iversen, S. S. Gjerde, and T. Undeland, "Multilevel converters for a 10 mw, 100 kv transformer-less offshore wind generator system," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*. IEEE, 2013, pp. 1–10.

[18] P. Sanjeev and S. Jain, "Analysis of conduction and switching losses in two level inverter for low power applications," in *India Conference (INDICON), 2013 Annual IEEE*. IEEE, 2013, pp. 1–6.

[19] J. Arrillaga and J. Arrillaga, *High voltage direct current transmission*. Iet, 1998, no. 29.

[20] ABB, "Topics. hvdc fundamentals," 2017, [Online; accessed 11-Feb-2019].

[21] S. Allebrod, R. Hamerski, and R. Marquardt, "New transformerless, scalable modular multilevel converters for hvdc-transmission," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE.* IEEE, 2008, pp. 174–179.

[22] C.-C. Liu, S. McArthur, and S.-J. Lee, *Smart grid handbook, 3 volume set.* John Wiley & Sons, 2016, vol. 1.

[23] J. Arrillaga, Y. H. Liu, and N. R. Watson, *Flexible power transmission: the HVDC options.* John Wiley & Sons, 2007.

[24] C. Davidson and D. Trainer, "Innovative concepts for hybrid multi-level converters for hvdc power transmission," 2010.

[25] J. Chen, D. Jiang, and Q. Li, "Attenuation of conducted emi for three-level inverters through pwm," *CPSS Transactions on Power Electronics and Applications*, vol. 3, no. 2, pp. 134–145, 2018.

[26] A. Yazdani and R. Iravani, *Voltage-sourced converters in power systems: modeling, control, and applications.* John Wiley & Sons, 2010.

[27] K. Sharifabadi, L. Harnefors, H.-P. Nee, S. Norrga, and R. Teodorescu, *Design, control, and application of modular multilevel converters for HVDC transmission systems.* John Wiley & Sons, 2016.

[28] H. Zhang, "Investigation and mitigation of the adverse effects of pwm adjustable speed drives," 1998.

[29] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on industrial electronics*, vol. 49, no. 4, pp. 724–738, 2002.

[30] J. M. Kharade and N. G. Savagave, "A review of hvdc converter topologies," *International Journal of Innovative Research in Science, Engineering and Technology*, vol. 6, no. 2, pp. 1822–1830, 2017.

[31] J. Kharade and N. G. Savagave, "A review of hvdc converter topologies," *International Journal of Innovative Research in Science, Engineering and Technology*, vol. 6, no. 2, pp. 1822–1830, 2017.

[32] B. J. Pawar and V. J. Gond, "Modular multilevel converters: A review on topologies, modulation, modeling and control schemes," in *Electronics, Communication and Aerospace Technology (ICECA), 2017 International conference of*, vol. 1. IEEE, 2017, pp. 431–440.

[33] R. Marquardt, "Modular multilevel converter: An universal concept for hvdc-networks and extended dc-bus-applications," in *Power Electronics Conference (IPEC), 2010 International*. IEEE, 2010, pp. 502–507.

[34] M. Barnes and A. Beddard, "Voltage source converter hvdc links–the state of the art and issues going forward," *Energy Procedia*, vol. 24, pp. 108–122, 2012.

[35] M. P. Kazmierkowski and L. Malesani, "Current control techniques for three-phase voltage-source pwm converters: A survey," *IEEE Transactions on industrial electronics*, vol. 45, no. 5, pp. 691–703, 1998.

[36] R. Naderi and A. Rahmati, "Phase-shifted carrier pwm technique for general cascaded inverters," *IEEE Transactions on power electronics*, vol. 23, no. 3, pp. 1257–1269, 2008.

[37] M. Moranchel, F. Huerta, I. Sanz, E. Bueno, and F. J. Rodríguez, "A comparison of modulation techniques for modular multilevel converters," *Energies*, vol. 9, no. 12, p. 1091, 2016.

[38] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Pulse width modulation scheme for the modular multilevel converter," in *Power Electronics and Applications, 2009. EPE'09. 13th European Conference on*. IEEE, 2009, pp. 1–10.

[39] F. Deng and Z. Chen, "Elimination of dc-link current ripple for modular multilevel converters with capacitor voltage-balancing pulse-shifted carrier

pwm," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 284–296, 2015.

[40] Maryaum Saeed Ifarad, "Multilevel Converters for Medium/High-Power Applications," https://courses.edx.org/courses/course-v1:GTx+DL0028M+3T2017/course/, 2018, [Online; accessed 20-Jan-2019].

[41] R. Darus, G. Konstantinou, J. Pou, S. Ceballos, and V. G. Agelidis, "Comparison of phase-shifted and level-shifted pwm in the modular multilevel converter," in *Power Electronics Conference (IPEC-Hiroshima 2014–ECCE-ASIA), 2014 International*, 2014, pp. 3764–3770.

[42] E. Solas, G. Abad, J. A. Barrena, S. Aurtenetxea, A. Carcar, and Ludwik, "Modular multilevel converter with different submodule conceptspart i: Capacitor voltage balancing method," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 10, pp. 4525–4535, 2013.

[43] J. Mei, K. Shen, B. Xiao, L. M. Tolbert, and J. Zheng, "A new selective loop bias mapping phase disposition pwm with dynamic voltage balance capability for modular multilevel converter," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 2, pp. 798–807, 2014.

[44] N.-Y. Dai, M.-C. Wong, Y.-H. Chen, and Y.-D. Han, "A 3-d generalized direct pwm algorithm for multilevel converters," *IEEE Power Electronics Letters*, vol. 3, no. 3, pp. 85–88, 2005.

[45] P. M. Meshram and V. B. Borghate, "A simplified nearest level control (nlc) voltage balancing method for modular multilevel converter (mmc)," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 450–462, 2015.

[46] P. Hu and D. Jiang, "A level-increased nearest level modulation method for modular multilevel converters," *IEEE transactions on Power Electronics*, vol. 30, no. 4, pp. 1836–1842, 2015.

[47] P. Sahu and V. Acharya, "Thd analysis of a vsc based hvdc transmission using multi-level converters and two-level converters," *International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering*, pp. 6098–6105, 2013.

[48] H. A. Pereira, V. F. Mendes, L. Harnefors, and R. Teodorescu, "Comparison of 2l-vsc and mmc-based hvdc converters: Grid frequency support considering reduced wind power plants models," *Electric Power Components and Systems*, vol. 45, no. 18, pp. 2007–2016, 2017.

[49] T. Honade, S. Udapure, S. Timande, S. Rodge, V. Burde, and S. Gudadhe, "Comparative study between two and three level converter for electric application," *International Journal of Advances in Engineering & Technology*, vol. 9, no. 2, p. 210, 2016.

[50] B. Chuco and E. Watanabe, "A comparative study of dynamic performance of hvdc system based on conventional vsc and mmc-vsc," in *Bulk Power System Dynamics and Control (iREP)-VIII (iREP), 2010 iREP Symposium*. IEEE, 2010, pp. 1–6.

[51] A. Ahmed, *Power Electronics for Technology*. Prentice Hall, 1999.

[52] P. Giroux, G. Sybille, C. Osorio, and S. Chandrachood, "Detailed model of a 100-kw grid-connected pv array," 2014.

[53] Wikipedia contributors, "Delta-wye transformer — Wikipedia, the free encyclopedia," https://en.wikipedia.org/w/index.php?title=Delta-wye_transformer&oldid=854273629, 2018, [Online; accessed 5-February-2019].

[54] W. Theodore *et al.*, *Electrical machines, drives and power systems, 6/E*, 2007.

[55] E. N. Abildgaard and M. Molinas, "Modelling and control of the modular multilevel converter (mmc)," *Energy Procedia*, vol. 20, pp. 227–236, 2012.

[56] H. Saad, S. Dennetière, J. Mahseredjian, P. Delarue, X. Guillaud, J. Peralta, and S. Nguefeu, "Modular multilevel converter models for electromagnetic

transients," *IEEE Transactions on Power Delivery*, vol. 29, no. 3, pp. 1481–1489, 2014.

[57] Wikipedia contributors, "Hvdc converter — Wikipedia, the free encyclopedia," https://en.wikipedia.org/w/index.php?title=HVDC_converter&oldid=881627638, 2019, [Online; accessed 5-February-2019].

[58] J. Freytes, S. Akkari, J. Dai, F. Gruson, P. Rault, and X. Guillaud, "Small-signal state-space modeling of an hvdc link with modular multilevel converters," in *Control and Modeling for Power Electronics (COMPEL), 2016 IEEE 17th Workshop on*. IEEE, 2016, pp. 1–8.

[59] G. M. Tina and G. Celsa, "A matlab/simulink model of a grid connected single-phase inverter," in *Power Engineering Conference (UPEC), 2015 50th International Universities*. IEEE, 2015, pp. 1–6.

[60] T. Kalitjuka, "Control of voltage source converters for power system applications," Master's thesis, Institutt for elkraftteknikk, 2011.

[61] Wikipedia contributors, "Direct-quadrature-zero transformation — Wikipedia, The Free Encyclopedia", year =."

[62] S. Ruihua, Z. Chao, L. Ruomei, and Z. Xiaoxin, "Vscs based hvdc and its control strategy," in *Transmission and Distribution Conference and Exhibition: Asia and Pacific, 2005 IEEE/PES*. IEEE, 2005, pp. 1–6.

[63] C. Bajracharya, "Control of vsc-hvdc for wind power," Master's thesis, Institutt for elkraftteknikk, 2008.

[64] C. Bajracharya, M. Molinas, J. A. Suul, T. M. Undeland *et al.*, "Understanding of tuning techniques of converter controllers for vsc-hvdc," in *Nordic Workshop on Power and Industrial Electronics (NORPIE/2008), June 9-11, 2008, Espoo, Finland*. Helsinki University of Technology, 2008.

[65] K. J. Åström, T. Hägglund, and K. J. Astrom, "Advanced pid control," 2006.

[66] J. L. Dominguez-Garcia, F. Bianchi, and O. Gomis, "Power control of voltage source converter for distributed generation," 2011.

[67] R. Zaimeddine and T. Undeland, "Direct power control strategies of a grid-connected three-level voltage source converter vsi-npc," in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*. IEEE, 2011, pp. 1–7.

[68] S. Sanchez, G. Bergna, and E. Tedeschi, "Tuning of control loops for grid-connected modular multilevel converters under a simplified port representation for large system studies," in *Ecological Vehicles and Renewable Energies (EVER), 2017 Twelfth International Conference on*. IEEE, 2017, pp. 1–8.

[69] Á. J. Rezek, C. A. Coelho, J. M. E. Vicente, J. A. Cortez, and P. R. Laurentino, "The modulus optimum (mo) method applied to voltage regulation systems: modeling, tuning and implementation," in *Proc. International Conference on Power System Transients, IPST*, vol. 1, 2001, pp. 24–28.

[70] J. W. Umland and M. Safiuddin, "Magnitude and symmetric optimum criterion for the design of linear control systems: what is it and how does it compare with the others?" *IEEE Transactions on Industry Applications*, vol. 26, no. 3, pp. 489–497, 1990.

[71] Z. Xu, S. Gao, and S. Yang, "Phase-shifted pulse-width-modulation scheme for modular multilevel converters," in *Industrial Technology (ICIT), 2016 IEEE International Conference on*. IEEE, 2016, pp. 360–365.

[72] E. Hossain, M. R. Tür, S. Padmanaban, S. Ay, and I. Khan, "Analysis and mitigation of power quality issues in distributed generation systems using custom power devices," *IEEE Access*, vol. 6, pp. 16 816–16 833, 2018.

[73] I. F II, "Ieee recommended practices and requirements for harmonic control in electrical power systems," *New York, NY, USA*, 1993.

[74] J. Espinoza-Jurado, E. Dávila, J. Rivera, J. J. Raygoza-Panduro, and S. Ortega, "Robust control of the air to fuel ratio in spark ignition engines with delayed measurements from a uego sensor," *Mathematical Problems in Engineering*, 2015.